

2010 IEEE CPMT Symposium Japan

**Tokyo, Japan
24 - 26 August 2010**



**IEEE Catalog Number: CFP10PWJ-PRT
ISBN: 978-1-4244-7593-3**

TABLE OF CONTENTS

SESSION 1: ADVANCED PACKAGE (AP-1)

Module Miniaturization by ultra thin Package Stacking ,	1
<i>Thomas Löher, David Schütze, Andreas Ostmann, Rolf Aschenbrenner</i>	
Development of Super Thin TSV PoP	5
<i>Flynn Carson, Kazuo Ishibashi, Seung Wook Yoon, Pandi Chelvam Marimuthu, Dzafir Shariff</i>	
A Wafer-level System Integration Technology for Flexible Pseudo-SOC Incorporates MemS-cmos Heterogeneous Devices	9
<i>Hiroshi Yamada, Yutaka Onozuka, Atsuko Iida, Kazuhiko Itaya, Hideyuki Funaki, Kazuhiro Takahashi, Hiroshi Toshiyoshi</i>	
Silicon TSV Interposer with Embedded Capacitors for High Performance VLSI Packaging	13
<i>Nagesh Vodrahall</i>	

SESSION 2: ADVANCED PACKAGE (AP-2)

Alternative Process and Support Material for Embedded Fine-pad-pitch LSI Package	17
<i>Hideya Murai, Kentaro Mori, Masaya Kawano, Shintaro Yamamichi</i>	
Preparation of Ferroelectric Capacitor Films Onto the Releasable Substrate and Its Application to Nano-transfer Method	21
<i>Masaaki Ichiki, Keita Imura, Toshifumi Hosono, Keisuke Kuraki, Fumiaki Tomioka, Tadatomo Suga, Ryutaro Maeda, Toshihiro Itoh</i>	
Embedded Wafer Level Ball Grid Array (eWLB) Technology for System Integration	24
<i>Klaus Pressel, Gottfried Beer, Thorsten Meyer, Maciej Wojniwski, Markus Fink, Gerals Ofner, Bernd Römer</i>	
High Density Substrate Solution for Complex High Pin Count Flip-Chip Applications	28
<i>Vern Solberg, Vage Oganessian</i>	

SESSION 3: BOARD LEVEL RELIABILITY (BR-1)

Invited : Mechanical and Material Reliability in Board Level Solder Joints	N/A
<i>Masazumi Amagai</i>	
Effect of Mild Aging on Package Drop Performance for Lead Free Solders	32
<i>SeokHo Na, SeWoong Cha, WonJoon Kang, TaeSeong Kim, TaeKyung Hwang, JinYoung Khim</i>	
Next Generation Substrate for High Density and Thin Package	37
<i>Toru Furuta</i>	
PoP Prototyping by Determination of Matter Transport Effects	41
<i>Lutz Meinshausen, Kirsten Weide-Zaage, Wei Feng, Hélène Frémont</i>	

SESSION 4: BOARD LEVEL RELIABILITY (BR-2)

Modeling of Board Level Solder Joint Reliability under Mechanical Drop Test with the Consideration of Plastic Strain Hardening of Lead-free Solder	45
<i>Z. J. Xu, T. Jiang, F. B. Song, Jeffery C. C. Lo, S. W. Ricky Le</i>	
Effect of Solders, Underfills and Substrates on Reliability of Flip-Chip Bonding of Low-k Semiconductor Chips	49
<i>Kenji Terada, Takayuki Nejime, Takafumi Ooyoshi, Kaoru Kobayashi, Kimihiro Yamanaka</i>	
Health Monitoring Method for Load Assessment in Reliability Design of Printed Circuit Board	53
<i>Kenji Hirohata, Katsumi Hisano, Yosuke Hisakuni, Takahiro Omori, Minoru Mukai</i>	
Effects of the Crystallographic Orientation of Sn Grain During Electromigration Test	57
<i>Kiju Lee, Keun-Soo Kim, Kimihiro Yamanaka, Yutaka Tsukada, Soichi Kuritani, Mimoru Ueshima, Katsuaki Suganuma</i>	

SESSION 5: ELECTRICAL DESIGN (ED-1)

Design Trade-Off for Resonance Reduction of Multiple Power Planes in Super Ball Grid Array (SBGA) Package	61
<i>GaWon Kim, SeungJae Lee, JiHeon Yu, Ozgur Misman, KiCheol Bae, TaeKi Kim, Sangwoong Lee, JinYoung Kim</i>	
Fast Power Integrity Estimation Method by Use of LSI Power-pin Model	65
<i>Takashi Harada, Masashi Ogawa, Manabu Kusumot</i>	
Modeling and Analysis of Differential Signal Through Silicon Via (TSV) in 3D IC	69
<i>Joohee Kim, Jun So Pak, Jonghyun Cho, Junho Lee, Hyungdong Lee, Kunwoo Park, JoungHo Kim</i>	
A Stopband Enhanced EBG Power/ground Plane based on Via Location Design	73
<i>Chuen-De Wang, Tzong-Lin Wu</i>	

SESSION 6: ELECTRICAL DESIGN (DE-2)

TSV Mutual Inductance Effect on Impedance of 3D Stacked On-Chip PDN with Multi-TSV Connections	77
<i>Jun So Pak, Jonghyun Cho, Joohee Kim, Junho Lee, Hyungdong Lee, Kunwoo Park, JoungHo Kim</i>	
Through Co-Design to Optimize Power Delivery Distribution System Using Embedded Discrete Decoupling Capacitor	81
<i>Chen-Chao Wang, Hung-Hsiang Cheng, Chi-Tsung Chiu, Chih-Pin Hung, Chih-Wen Kuo, Toshihide Kitazawa</i>	
Impulse Responses of On-chip Power Supply Networks with Varying Conditions	85
<i>Yutaka Uematsu, Hideki Osaka, Masayoshi Yagyu,</i>	

SESSION 7: INTERCONNECT (IC)

Fine Pitch Cu Wire Bonding – As Good As Gold	89
<i>Bernd K. Appelt, William T. Chen, Andy Tseng, Yi-Shao Lai</i>	
Wire Bonding with Pd-Coated Copper Wire	93
<i>Horst Clauberg, Bob Chylak, Nelson Wong, Johnny YeungInd</i>	
Study of EMC for Cu Bonding Wire Application	97
<i>Hidetoshi Seki, Chen Ping, Hiroshi Nakatake, Shin-ichi Zenbutsu, Shingo Itoh</i>	
Process Design of Self-Replication for Micro Bump Formation	100
<i>Kiyokazu Yasuda</i>	

SESSION 8: OPTICAL VS. ELECTRICAL TRANSMISSION (OE-1)

Invited : Potential of Wavelength-Division-Multiplexing Optical-Interconnects for Next-Generation System in Packaging	N/A
<i>Shogo Ura, Kenji Kintaka</i>	
Study on Novel Concept of Transmission Signal Assisted with Evanescent Wave Energy	104
<i>Kaoru Hashimoto, Kazuo Kohno, Yutaka Akiyama, Hisashi Kikuchi, Kanji Otsuka</i>	
A Feasibility Study of Proximity Interconnect Technology Utilizing Transmission Line Coupling	108
<i>Daisuke Iguchi, Yutaka Akiyama, Fumiaki Fujii, Kanji Otsuka</i>	
Analysis of On-Board Antenna Modules for the Millimeter-Wave Intra-Connect system	112
<i>Sho Ohashi, Takahiro Takeda, Hirofumi Kawamura, Yasuhiro Okada, Masahiro Uno, Yoshiyuki Akiyama, Kenichi Kawasaki</i>	

SESSION 9: 3D INTEGRATION (3D-1)

Development of High Accuracy Wafer Thinning and Pickup Technology for Thin Wafer(die)	116
<i>Chuichi Miyazaki, Haruo Shimamoto, Toshihide Uematsu, Yoshiyuki Abe, Kosuke Kitaichi, Tadaihiro Morifuji, Shoji Yasunaga</i>	
Development of High Speed Copper CMP Slurry for TSV Application Based on Friction Analysis	120
<i>Jin Amanokura, Hiroshi Ono, Kyoko Hombo</i>	
Evaluation of Surface Microroughness for Surface Activated Bonding	124
<i>Kei Tsukamoto, Eiji Higurashi, Tadatomo Suga</i>	

Guard-Ring Effect for Through Silicon Via (TSV) Noise Coupling Reduction	128
<i>Jonghyun Cho, Kihyun Yoon, Jun So Pak, Joohee Kim, Junho Lee, Hyungdong Le2, Kunwoo Park, Jounggho Kim</i>	

SESSION 10: 3D INTEGRATION (3D-2)

Development of Multi-Stack Process on Wafer-on-Wafer (WOW)	132
<i>Koji Fujimoto, Nobuhide Maeda, Hideki Kitada, Youngsuk Kim, Akihito Kawai, Kazuhisa Arai, Tomoji Nakamura, Kousuke Suzuki, Takayuki Ohba</i>	
Room-temperature Si-Si and Si-SiN Wafer Bonding	136
<i>Ryuichi Kondou, Chenxi Wang, Tadatomu Suga</i>	
Thermal Stress Analysis of the 3D Die Stacks with Low-Volume Interconnections	140
<i>Sayuri Kohara, Katsuyuki Sakuma, Yoshikazu Takahashi, Tohoyiro Aoki, Kumiaki Sueoka, Keiji Matsumoto, Paul S. Andry, Cornelia K. Tsang, Edmund J. Sprogis, John U. Knickerbocker, Yasumitsu Orii</i>	
Wafer And/or Chip Bonding Adhesives for 3D Package	144
<i>Toshihisa Nonaka, Koichi Fujimaru, Akira Shimada, Noboru Asahi, Yoshiko Tatsuta, Hiroyuki Niwa, Yasuko Tachibana</i>	

SESSION 11: MECHANICAL DESIGN (MD-1)

Review on the High Temperature Warpage Measurement Using Shadow Moiré	148
<i>Yong Goo Um, Jin Young Khim</i>	
Warpage Mechanism of Single-sided Molded Package Studied with Viscoelastic Analysis	152
<i>Yusuke Komoto</i>	
Vibration Test Durability on Large BGA Assemblies: Evaluation of Reinforcement Techniques,	156
<i>Matthieu Berthou3, Hua Lu, Pascal Retailleau, Helene Frémont, Alexandrine Guédon-Gracia, Catherine Jephos-Davennel, Christopher Bailey</i>	
The Development of Cleaving - DBG + CMP Process	160
<i>Shinya Takyu, Mika Kiritani, Tetsuya Kuroswa, Noriko Shimizu</i>	

SESSION 12: MECHANICAL DESIGN (MD2)

Thermal Stress Analysis of FCBGA During Cooling Under Reflow Process	164
<i>Chihiro J. Uchibori, Michael Le</i>	
Assembly-Stress-Mechanism in Pad Areas of Flip Chip Package on High-k/Metal gate Transistors	168
<i>Yukitoshi Ota, Fumito Itoh, Kazuhiro Ishikawa, Kiyomi Hagihara, Takeshi Matsumoto, Teppei Iwase, Yutaka Itoh, Hiroshige Hirano</i>	

SESSION 13: THERMAL DESIGN (TD-1)

Heat Spreader Technology for Silicon Chip	172
<i>Tomoyuki Kosakabe, Masataka Mochizuki, Koichi Mashiko, Yuji Saito, Fumitoshi Kiyooka, Yasuhiro Horiuchi, Gerald Cabusao, Thang Nguyen</i>	
A Study of Thermal Performance for Chip-in-Substrate type LED Package Structure	176
<i>Yen-Fu Su, Tuan-Yu Hung, Shin-Yueh Yang, Kuo-Ning Chiang</i>	

SESSION 14: THERMAL DESIGN (TD-2)

Study on the Application of Thermal Interface Materials for Integration of HP-LEDs	180
<i>Jun Wu, Meilin Zhuang, Shuzhi Li, Weiqiao Yang, Jianhua Zhang</i>	
Structure Function Based Thermal Resistance & Thermal Capacitance Measurement for Semiconductor Packages	185
<i>Yafei Luo</i>	
Data Center Energy Conservation Utilizing Heat Pipe Based Ice Storage System	190
<i>Gerald Cabusao, Masataka Mochizuki, Koichi Mashiko, Tetsuya Kobayashi, Randeep Singh, Thang Nguyen, Xiao Ping Wu</i>	

SESSION 15: MATERIAL (ML-1)

Invited : Recent Advance in Anisotropic Conductive Adhesives (ACAs) Materials and Processing Technology	194
<i>Kyung-Wook Paik</i>	
Micro- Solder Precoat Technology by Precoat by Powder Sheet method	198
<i>Kaichi Tsuruta, Takeo Kuramoto, Takeo Saitou, Manabu Muraoka</i>	

SESSION 16: MATERIAL (ML-2)

Preparation of Active Layer of Solar Cells Device by F8T2 Blending with PCBM	202
<i>Han-Sheng Huang , Po-Yi Lu , Cho-Liang Chung, Shen-Li Fu</i>	
A Novel Polymer Technology for Underfill	206
<i>Osamu Suzuki, Toshiyuki Sato, Pawel Czubarow Tomasz Waechol, Dave Son</i>	
Transparent Encapsulating Resin for Automotive Applications	210
<i>Hisataka Ito, Hiroshi Noro, Shinya Oota</i>	
High Reliability Epoxy Encapsulating Compound for Power Module	214
<i>Yuya Kitagawa, Satomi Yano, Hironori Kobayashi, Aya Mizushima</i>	

SESSION 17: MATERIAL (ML-3)

Phase Transformation of Metallic Nanoparticle Deposites for the Electrodes of Flexible Electronics	218
<i>Tzu-Hsuan Kao, Jenn-Ming Song, Jian-Yih Wang, In-Gann Chen</i>	
A New, Cost-effective Coreless Substrate Technology	222
<i>Bernd K. Appelt, Bruce Su, Alex S.F. Huang, Yi-Shao Lai</i>	
Build-up Electrical Insulation Material with Low-Dielectric Tangent, Low-CTE and Low-Surface Roughness	226
<i>Isao Suzuki, Toshiaki Tanaka, Akihiro Uenishi, Takayuki Kobayashi, Junnosuke Murakami</i>	
Electroless Ni/Pd/Au Plating for Semiconductor Package Substrates -Effect of Gold Plating Combinations on Gold Wire Bonding Reliability-	230
<i>Yoshinori Ejiri, Takehisa Sakurai, Yoshinori, Arayama, Yoshiaki Tsubomatsu, Shuuichi Hatakeyama, Shigeharu Arike, Yukihsa Hiroyama, Kiyoshi Hasegawa</i>	

SESSION 18: OPTOELECTRONICS (OE-2)

Invited : Multichannel Optical Modules with an SF Optical Connector Interface	234
<i>Hiromasa Tanobe, Shuichiro Asakawa, Masaru Kobayashi, Junya Kobayashi</i>	
High-bandwidth Optical MCM: FPGA with Optical I/O on Waveguide-integrated SLC	238
<i>Masao Tokunari, Jean Benoit Héroux, Shigeru Nakagawa</i>	

SESSION 19: OPTOELECTRONICS (OE-3)

4-ch × 10-Gb/s Chip-to-chip Optical Interconnections with Optoelectronic Packages and Optical Waveguide Separated from PCB	242
<i>Yutaka Takagi, Atsushi Suzuki, Toshikazu Horio, Takeshi Ohno, Toshifumi Kojima, Toshikatsu Takada, Satoshi Iio, Kazushige Obayashi, Masahiko Okuyama</i>	
1060-nm 10-Gb/s X12-channel Parallel-optical Modules for Optical Interconnects	246
<i>Toshinori Uemura, Yoza Ishikawa, Yoshinobu Nekado, Atsushi Izawa, Masakazu Yoshihara, Hideyuki Nasu</i>	
High Throughput On-board Parallel Optical Modules Using Multi-chip Visual Alignment Technique	250
<i>Kenichro Yashiki, Takara Sugimoto, Ichiro Ogura, Kazuhiro Kurata</i>	
Relationship Between Alignment Errors of Optical Components and Power Consumption in Ptoelectronic Devices	254
<i>Hironobu Morita, Minoru Watanabe</i>	

SESSION 20 OPTOELECTRONICS (OE-4)

Polymeric Multi/demultiplexers Using Light-induced Self-written Waveguides for Cost-effective Optical Interconnection..... 258
Tatsuya Yamashita, Akari Kawasaki, Manabu Kagami, Takashi Yasuda, Hideki Goto

Soft-Lithographic Fabrication of Polymer Parallel Optical Waveguides with Graded-Index Cores for Board-Level Optical Interconnections 262
Takaaki Ishigure, Yosuke Nitta, Yusuke Sugimori

Optical Waveguide Materials with High Thermal Reliability and Their Applications for High-density Optical Interconnections 266
Tomoaki Shibata, Tatsuya Makino, Atsushi Takahashi, Yasunobu Matsuoka, Tosahiki Sugawara

Author Index