

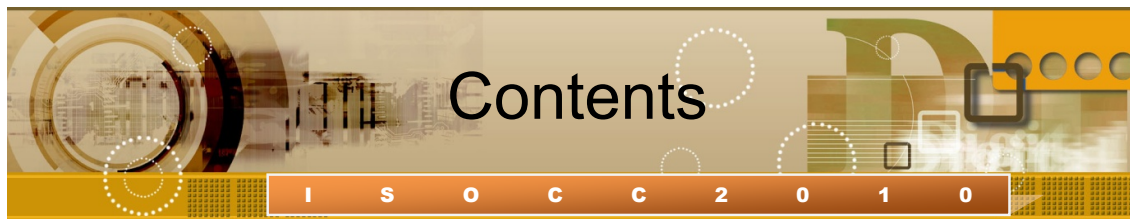
# **2010 International SoC Design Conference**

**(ISOCC 2010)**

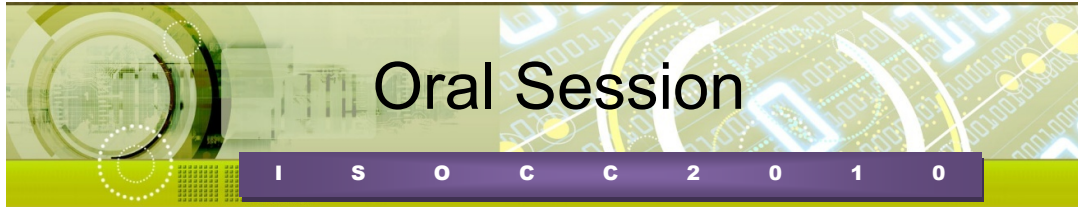
**Incheon, South Korea  
22 – 23 November 2010**



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**Session 1**

**Noise Management and Reliability Enhancement Techniques for Gigascale SoC**

14:15 – 15:45 Monday, November 22, 2010 Room 104

Special Session

Organizer: Volkan Kursun (Hong Kong University of Science and Technology, Hong Kong)

Chair: Volkan Kursun (Hong Kong University of Science and Technology, Hong Kong)

**Overview**

Various noise and reliability enhancement techniques are presented in this session. A methodology for the analysis and mitigation of noise in large scale heterogeneous SoC is described in the first paper. A new power gating technique applicable to memory circuits for implementing a low leakage data retention sleep mode with enhanced noise margins is proposed in the second paper. The noise mitigating effect of forward body bias in MTCMOS circuits is discussed in the third paper. Design of ultra wideband transceiver and receiver circuits for electrostatic discharge protection are presented in the fourth paper. Tradeoffs between longer battery lifetime and higher noise margins in communications circuits used for wireless devices are reviewed in the fifth paper. Various techniques for the attenuation of narrow-band interference in spread-spectrum wireless communications systems are discussed. Finally, techniques to enhance the reliability of circuits subject to electrical fast transient events are described in the sixth paper of the session.

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 Stony Brook University, USA ..... 1

**[S1-2] Power Gated SRAM Circuits with Data Retention Capability and High Immunity to Noise: A Comparison for Reliability in Low Leakage Sleep Mode**  
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<sup>(1)</sup> University of California, Riverside, USA  
<sup>(2)</sup> Peking University, China  
<sup>(3)</sup> CitrusCom Semiconductor, China  
<sup>(4)</sup> Fairchild Semiconductor, USA  
<sup>(5)</sup> SMIC, China  
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Michael A. Soderstrand  
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14:15 – 15:30 Monday, November 22, 2010 Room 102

Special Session

Organizer: Tae-Chan Kim (Samsung Electronics, Korea)

Chair: Tae-Chan Kim (Samsung Electronics, Korea)

**Overview**

Digital photos and videos have become more and more popular in our daily life. Therefore, Digital camera products, especially general digital cameras such as DSLRs, digital still cameras, cell phones and webcams, and in addition other applications such as surveillance, automotive, medical, etc., have grown explosively. Such trend incentivizes the development of image sensors with smaller pixel, lower power and higher speed as well as better image quality. Recently, 3-D camera technologies such as stereo type and depth cameras are being widely developed and high-sensitive cameras using white pixel, near IR pixel, wide dynamic range and low-noise techniques are also gaining great popularity. To reflect the trend, this session presents these up-to-dated technologies on image sensor and image signal processor (ISP). A total of 5 papers include analog circuit design for CMOS image sensor and image processing techniques for enhancement of image quality. In paper [S2-1], CMOS Image Sensor (CIS) for VGA is presented. It has 11-bit column parallel single-slope ADCs which offers a significantly lower noise. In paper [S2-2], a novel image noise reduction filter is developed in wavelet domain. The correlations of intensity and anisotropy of wavelet coefficients in different sub-bands and scales are utilized as features to separate signal from random noise by dynamic thresholding. In paper [S2-3], a weighted adaptive image defogging method by extracting features in the RGB color channels is presented. It can overcome the problem of local color distortion,

which is known to be the limitations of existing defogging techniques. In paper [S2-4], new framework is proposed for upsampling the resolution of depth maps that jointly uses Gaussians of spatial and depth differences of low resolution depth map. Finally paper [S2-5] presents an efficient image fusion of the visible range (VR) and infrared range (IR) images for image enhancement in digital still camera.

<b>[S2-1]</b> A VGA CMOS Image Sensor with 11-bit column parallel single-slope ADCs Nayeon Cho <sup>(1)</sup> , Bongsub Song <sup>(1)</sup> , Kwangsoo Kim <sup>(1)</sup> , Jinwook Burm <sup>(1)</sup> and Sang-Wook Han <sup>(2)</sup> <sup>(1)</sup> Sogang University, Korea <sup>(2)</sup> Samsung Electronics, Korea .....	25
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14:15 – 15:15 Monday, November 22, 2010 Room 110

Regular Session

Chair: Byeong Kil Lee (University of Texas, San Antonio, USA)

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**Session 5** **Behavioral and System-Level Synthesis**

17:00 – 18:00 Monday, November 22, 2010 Room 104

Special Session

Organizer: Hiroyuki Tomiyama (Ritsumeikan University, Japan)

Chair: Hiroyuki Tomiyama (Ritsumeikan University, Japan)

**Overview**

Automatic synthesis from abstract models/descriptions is the key for designing complex SoCs in short time. This special session presents several state-of-the-art methodologies on behavioral and system-level synthesis. The topics include high-level synthesis from C and MATLAB/Simulink, processor synthesis and MPSoC design space exploration.

- [S5-1]** Towards Practical High-Level Synthesis From Large Behavioral Descriptions  
Yuko Hara-Azumi<sup>(1)(2)(3)</sup>, Toshinobu Matsuba<sup>(2)</sup>, Hiroyuki Tomiyama<sup>(3)</sup>, Shinya Honda<sup>(2)</sup>, Hiroaki Takada<sup>(2)</sup> and Nikil Dutt<sup>(1)</sup>  
<sup>(1)</sup>University of California, Irvine, USA

( <sup>2</sup> )Nagoya University, Japan	
( <sup>3</sup> )Ritsumeikan University, Japan	71
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Yoshinori Takeuchi, Keishi Sakanushi and Masaharu Imai	
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Seiya Shibata <sup>(1)(2)</sup> , Shinya Honda <sup>(1)</sup> , Hiroyuki Tomiyama <sup>(3)</sup> and Hiroaki Takada <sup>(1)</sup>	
( <sup>1</sup> )Nagoya University, Japan	
( <sup>2</sup> )Japan Society for the Promotion of Science, Japan	
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Dai Araki <sup>(1)</sup> , Atsushi Nakamura <sup>(1)</sup> , Masayuki Miyama <sup>(2)</sup>	
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( <sup>2</sup> )Kanazawa University, Japan	83

## Session 6

### Methodology and Design for Multimedia and Communication SoCs

17:00 – 18:30 Monday, November 22, 2010

Room 102

Special Session

Organizer: Yeong-Kang Lai (National Chung Hsing University, Taiwan)

Chair: Yeong-Kang Lai (National Chung Hsing University, Taiwan)

### Overview

With the recent advances in VLSI technology, the SoC design for multimedia and communication applications appears possible. Several key technologies will be introduced in this special session. The technology scope covers the high definition multi-view video encoder, the hybrid full system simulation platform, the high definition camera and camcorder system, the MIMO-OFDM System, the synthesizable AXI protocol checker, and the multi-standard video decoder. In addition, these papers also employ two architecture approaches to implement the multimedia and communication algorithms. One is to use dedicated architectures. The architectures offer a high performance processing capability, but take considerable time and effort to fabricate and test. Thus, they have less flexibility. The other is to use reconfigurable/programmable architectures. Their main advantages are function flexibility and multiprocessing capability. However, the performance is not enough high due to complex architectures. In this special session, we will also introduce these two design methodologies for SoC design.

<b>[S6-1] System Scheduling Analysis for High Definition Multiview Video Encoder</b>	
Pei-Kuei Tsung, Li-Fu Ding, Wei-Yin Chen, Tzu-Der Chuang, Shao-Yi Chien and Liang-Gee Chen	
National Taiwan University, Taiwan	87

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Regular Session

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## Session 8

## Communication &amp; Multimedia SoCs

17:00 – 18:15 Monday, November 22, 2010 Room 110

Regular Session

Chair: Sang Hoon Hong (Kyung Hee University, Korea)

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 Chang-Ha Jeon<sup>(1)</sup>, Jae-Kyung Lee<sup>(1)</sup>, Dong-Hyun Seo<sup>(1)</sup>, Jeong-Hun Kim<sup>(1)</sup>, Jin-Gyun Chung<sup>(1)</sup> and Chul-Dong Lee<sup>(2)</sup>  
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## Session 9

## New Horizons in SoC and ASIC Design

09:45 – 11:00 Tuesday, November 23, 2010 Room 104

Special Session

Organizer: Volkan Kursun (Hong Kong University of Science and Technology, Hong Kong)

Chair: Volkan Kursun (Hong Kong University of Science and Technology, Hong Kong)

**Overview**

Novel techniques for enhanced performance and power efficiency in application specific integrated circuits (ASICs) and systems-on-chips are presented in this session. Potential power and speed advantages and adoptability challenges of pulsed latches in ASICs are discussed in the first paper. The idea of using selectively patterned masks and different types of tiles to lower the area and delay of structured ASICs is explored in the second paper. Seven-transistor static memory cells are presented in the third paper for providing enhanced data stability with a UMC 80nm

multi-threshold-voltage CMOS technology. A detailed analysis of rare events with statistical blockade approach and Monte Carlo simulation is presented in the fourth paper. Finally, a quantitative design methodology for capacitive interpolated flash analog to digital converters is presented in the fifth paper of the session.

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<sup>(1)</sup> University of California, Riverside, USA	
<sup>(2)</sup> Fairchild Semiconductor, Inc., USA	
<sup>(3)</sup> Peking University, Beijing, China.....	166

## Session 10

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09:45 – 11:15 Tuesday, November 23, 2010

Room 102

Regular Session

Chair: Byeong Kil Lee (University of Texas, San Antonio, USA)

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**Session 11**

**Analog and Mixed-Signal Circuits 1**

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Regular Session

Chair: Gil Cho Ahn (Sogang University, Korea)

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**Session 12**

**SoC Testing & Signal Integrity**

09:45 – 11:00 Tuesday, November 23, 2010 Room 110  
Regular Session

Chair: Tae Hee Han (Sungkyunkwan University, Korea)

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## Session 13

### Low Power Design for Electronic System

13:45 – 15:00 Tuesday, November 23, 2010

Room 104

Special Session

Organizer: Satoshi Goto (Waseda University, Japan)

Chair: Satoshi Goto (Waseda University, Japan)

Co-Chair: Jong-Wha Chong (Hanyang University, Japan)

### Overview

The growing classes of personal multimedia devices ( mobile phone or digital camera) as well as imaging systems and multimedia communication systems, that demand real-time processing and compression techniques with low power consumption, becomes a driving force for developing low power electronic system. This special session focuses on advanced low power technologies from system level to device level. Since the different kinds of applications results in diversity in video contents, the techniques are designed according to pursue the best trade-off between the power consumption and processing performance. Algorithm together with hardware implementation schemes have to be selectively introduced.

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BongKi Lee, Jaehwan Kim, Yeuncheul Jeung and Jongwha Chong

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## Session 14

### Emerging CMOS Device and Circuit Technologies

13:45 – 15:15 Tuesday, November 23, 2010

Room 102

Special Session

Organizer: Volkan Kursun (Hong Kong University of Science and Technology, Hong Kong)

Chair: Volkan Kursun (Hong Kong University of Science and Technology, Hong Kong)

### Overview

Technology scaling challenges, novel nanodevices, and nanomaterials are presented in this session. Feasibility of one-dimensional nanomaterials as a building block of electronic and optoelectronic devices is explored in the first paper. Large scale assembly of inorganic one-dimensional materials forming a variety of functional electronic and optoelectronic devices, such as field-effect transistors, Schottky diodes, and photodiodes is demonstrated. A tunneling magnetoresistance device is introduced and potential applications of this new spintronic device in SoC design are discussed in the second paper. Technology and circuit level challenges for scaling multi-gate transistors into sub-22 nm regime are discussed in the third paper. Electrical characteristics of P-type carbon nanotube MOSFETs are explored in the fourth paper. Optimum 16nm P-type carbon nanotube device profiles are presented for achieving high-speed, area efficient, and manufacturable integrated circuits. Finally, behavior of drain extended n-channel MOSFETs and various other nanoscale devices under electrostatic discharge stress are evaluated in the fifth and sixth papers, respectively.

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Yun-ze Long, Johnny C. Ho, Zhiyong Fan

Hong Kong University, Hong Kong..... 248

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Yiran Chen<sup>(1)</sup>, Hai Li<sup>(2)</sup>, Xiaobin Wang<sup>(3)</sup> and Jongsun Park<sup>(4)</sup><sup>(1)</sup>University of Pittsburgh, Pittsburgh, USA<sup>(2)</sup>Polytechnic Institute of New York University, Brooklyn, USA<sup>(3)</sup>Seagate Technology, USA<sup>(4)</sup>Korea University, Korea..... 252

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## Session 15

### Analog and Mixed-Signal Circuits 2

13:45 – 15:00 Tuesday, November 23, 2010

Room 107

Regular Session

Chair: Kang-Yoon Lee (Konkuk University, Korea)

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**Session 16**

**SoC Design Methodology 1**

13:45 – 15:00 Tuesday, November 23, 2010 Room 110

Regular Session

Chair: Yungseon Eo (Hanyang University, Korea)

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**Session 17**

**Design for Noise Tolerance, Error Correction and Energy Efficiency in CMOS VLSI Circuits and Systems**

15:30 – 16:45 Tuesday, November 23, 2010 Room 104

Special Session

Organizer: Kiat Seng YEO (Nanyang Technological University, Singapore)

Chair: Kiat Seng YEO (Nanyang Technological University, Singapore)

**Overview**

As technology nodes approach the sub-100nm regime, statistical behaviors such as noise, parametric variations, defects, dopant concentrations and tunneling effects, just to name a few, are

becoming more prominent. As a result, the nature of digital computation is shifting from deterministic to probabilistic VLSI design. This special session focuses on the challenges associated with the probabilistic nature and the reliability issues of scaled CMOS devices. The selected papers will cover from providing reliable computation in the presence of strong interference to building energy efficient digital blocks with probabilistic-based or hardware redundant methodologies. Paper [S17-1] proposes a new Differential Cascode Voltage Switch based Markov Random Field (MRF) logic design method, which offers substantial noise immunity improvement over the normal MRF logic circuits. Paper [S17-2] presents a feedback monitor scheme to significantly increase the reliability of SRAM cells. Paper [S17-3] describes a novel termination mechanism for LDPC-BCH decoding which leads to reduced parallelism, power and area consumption. Paper [S17-4] demonstrates a unique circuit technique to design a 32-bit error-tolerant adder. Unlike traditional circuit designs, the proposed adder can simultaneously give high speed and low power with good accuracy. Finally paper [S17-5] shows a Random Number Generator (RNG) with excellent statistical quality and low power consumption. The chip, which consists of a serial-to-parallel shift register, a 32-bit register and a pseudo random number generator module, is realized using a 180-nm CMOS process from Global Foundries.

- [S17-1] Design of Probabilistic-Based Markov Random Field Logic Gates in 65nm CMOS Technology**  
 Zhenghao Lu<sup>(1)</sup>, Xiao Peng Yu<sup>(2)</sup> and Kiat Seng Yeo<sup>(3)</sup>  
<sup>(1)</sup>Soochow University, China  
<sup>(2)</sup>Zhejiang University, China  
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 Ning Zhu, Wang Ling Goh, Gang Wang and Kiat Seng Yeo  
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- [S17-5] A Random Number Generator for Low Power Cryptographic Application**  
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### Overview

While digital circuits and systems have enjoyed benefits of scaling, analog circuits have not enjoyed the same benefits. Rather, ever-shrinking signal range and supply voltage, lower device gain, poor matching, and increased substrate noise all are conspiring to make analog design extremely challenging. This special session focuses on the challenges associated with high performance mixed-signal circuit design for mobile applications in deep-sub micron CMOS technologies. The selected papers cover a low power ultra-wideband RF transmitter, a high performance audio DAC, a high speed low-power data converter, a PLL-based clock generator, and power management units. Paper [S18-1] proposes an ultra-wideband (UWB) transmitter which adopts an automatic self-calibration technique to reduce sideband tones, achieving high performance and manufacturability with high-production yield. Paper [S18-2] presents a stereo audio DAC with ground-centered class-D headphone drivers adopting built-in self-calibration to minimize static power dissipation caused by DC offset voltage. Paper [S18-3] describes a 7b 1GS/s CMOS folding ADC which utilizes simple bootstrapped sampling switch and track-and-hold circuit, sequential amplifier settling method and low-power thermometer-to-binary encoder. Paper [S18-4] demonstrates a clock generator in a 32nm CMOS process with ultra-low power consumption and the operating capability under 1-V supply voltage. By adopting automatic frequency control and adaptive bandwidth architecture, the robustness over PVT is further enhanced. Paper [S18-5] shows a dual-mode DC-DC converter with automatic mode change control which reduces the inductor peak current during the transition between the pulse frequency modulation (PFM) and the pulse width modulation (PWM). Finally paper [S18-6] presents a temperature sensor which detects from  $-25^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  with  $1^{\circ}\text{C}$  resolution using the SAR type algorithm and software calibration.

#### [S18-1] An Ultra-Wideband Transmitter with Automatic Self-Calibration of Sideband

##### Rejection up to 9 GHz in 65nm CMOS

Byoungjoong Kang, Jounghyun Yim, Taewan Kim, Heeseon Shin, Sangsoo Ko, Won Ko, Inhyo Ryu, Sung-Gi Yang, Wooseung Choo and Byeong-Ha Park

Samsung Electronics, Korea ..... 332

#### [S18-2] A Self-Calibration 103-dB SNR Stereo Audio DAC with True-GND Class-D

##### Headphone Drivers in 45nm CMOS

Yong-Hee Lee, Chun-Kyun Seok, Bong-Joo Kim, Seung-Bin You, Wang-Seup Yeum, Ho-Jin Park and Byeong-Ha Park

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**Session 19**

**RF & Display**

15:30 – 16:45 Tuesday, November 23, 2010

Room 107

Regular Session

Chair: Sang-Woong Yoon (Kyung Hee University, Korea)

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Session 20

**SoC Design Methodology 2**

15:30 – 16:45 Tuesday, November 23, 2010 Room 110

Regular Session

Chair: Soonhoi Ha (Seoul National University, Korea)

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<sup>(1)</sup>Xi'an Jiaotong-Liverpool University, China  
<sup>(2)</sup>Bangalore, India  
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