

**2007 5th IEEE/ACM/IFIP
International Conference on
Hardware/Software Codesign
and System Synthesis**

(CODES+ISSS 2007)

**Salzburg, Austria
30 September – 3 October 2007**



**IEEE Catalog Number: CFP07COD-PRT
ISBN: 978-1-59593-824-4**

Table of Contents

ESWEEK 2007 Technical Sponsors

Sunday, September 30th

Tutorials

- **Beyond Gaming: Programming the PLAYSTATION3 Cell Architecture for Cost-Effective Parallel Processing** 1
Rodric Rabbah (*IBM Watson Research Center*)
- **Compiling Code Accelerators for FPGAs** 2
Walid. A. Najjar (*University of California, Riverside*)

Monday, October 1st • 10:30–12:30

Session 1A: System-Level Design Methods for MPSoC

Session Chair: Todor Stefanov, Session Co-chair: Sungchan Kim

- **Simultaneous Synthesis of Buses, Data Mapping and Memory Allocation for MPSoC** 3
Brett H. Meyer, Donald E. Thomas (*Carnegie Mellon University*)
- **A Framework for Rapid System-level Exploration, Synthesis, and Programming of Multimedia MP-SoCs** 9
Mark Thompson (*University of Amsterdam*), Hristo Nikolov, Todor Stefanov (*Leiden University*),
Andy D. Pimentel, Cagkan Erbas, Simon Polstra (*University of Amsterdam*),
Ed F. Deprettere (*Leiden University*)
- **Predictable Execution Adaptivity through Embedding Dynamic Reconfigurability into Static MPSoC Schedules** 15
Chengmo Yang, Alex Orailoglu (*University of California, San Diego*)

Session 1B: Specification Language and Model Transformations to Support Synthesis and Design

Session Chair: Robert P. Dick, Session Co-chair: John Darringer

- **Synchronization after Design Refinements with Sensitive Delay Elements** 21
Tarvo Raudvere, Ingo Sander, Axel Jantsch (*Royal Institute of Technology*)
- **Embedded Software Development on Top of Transaction-Level Models** 27
Wolfgang Klingauf, Robert Günzel, Christian Schröder (*Technical University of Braunschweig*)
- **Pointer Re-coding for Creating Definitive MPSoC Models** 33
Pramod Chandraiah, Rainer Dömer (*University of California, Irvine*)

Monday, October 1st • 13:30–15:30

Session 2A: Embedded Systems

Session Chair: Catherine Gebotys, Session Co-chair: Fadi Kurdahi

- **Dynamic Security Domain Scaling on Symmetric Multiprocessors for Future High-End Embedded Systems** 39
Hiroaki Inoue (*NEC Corporation*), Akihisa Ikeno (*NEC Informatec Systems, Ltd.*),
Tsuyoshi Abe, Junji Sakai, Masato Edahiro (*NEC Corporation*)
- **Secure FPGA Circuits Using Controlled Placement and Routing** 45
Pengyuan Yu, Patrick Schaumont (*Virginia Tech*)
- **A Smart Random Code Injection to Mask Power Analysis Based Side Channel Attacks** 51
Jude Angelo Ambrose, Roshan G. Ragel, Sri Parameswaran (*University of New South Wales*)
- **Ensuring Secure Program Execution in Multiprocessor Embedded Systems: A Case Study** 57
Krutartha Patel, Sridevan Parameswaran, Seng Lin Shee (*The University of New South Wales*)

Session 2B: Heterogeneous Computing Platform Simulation and Debug

Session Chair: Franco Fummi, Session Co-chair: Ahmed Jerraya

- **Combined Approach to System Level Performance Analysis of Embedded Systems** 63
Simon Künzli (*Siemens Building Technologies*), Arne Hamann (*TU Braunschweig*),
Rolf Ernst (*TU Braunschweig*), Lothar Thiele (*ETH Zurich*)
- **Event-based Re-training of Statistical Contention Models for Heterogeneous Multiprocessors** 69
Alex Bobrek (*Carnegie Mellon University*), JoAnn M. Paul (*Virginia Tech*),
Donald E. Thomas (*Carnegie Mellon University*)
- **HySim: A Fast Simulation Framework for Embedded Software Development** 75
Stefan Kraemer, Lei Gao, Jan Weinstock, Rainer Leupers, Gerd Ascheid, Heinrich Meyr
(*RWTH Aachen University*),
- **A Computational Reflection Mechanism to Support Platform Debugging in SystemC** 81
Bruno Albertini, Sandro Rigo, Guido Araujo (*UNICAMP*),
Cristiano Araujo, Edna Barros, Williams Azevedo (*Federal University of Pernambuco*),

Monday, October 1st • 16:00–17:30

Session 3A: Static and Dynamic Techniques for Partitioning and Scheduling

Session Chair: Jianwen Zhu, Session Co-chair: Paul Pop

- **Energy Efficient Co-scheduling in Dynamically Reconfigurable Systems** 87
Pao-Ann Hsiung, Pin-Hsien Lu, Chih-Wen Liu (*National Chung Cheng University*)
- **Thread Warping: A Framework for Dynamic Synthesis of Thread Accelerators** 93
Greg Stitt (*University of Florida*), Frank Vahid (*University of California, Riverside*)
- **HW/SW Co-Design for Esterel Processing** 99
Sascha Gädtke, Claus Traulsen, Reinhard von Hanxleden (*Christian-Albrechts-Universität zu Kiel*)

Session 3B: Low Power Design and Thermal Control

Session Chair: Joerg Henkel, Session Co-chair: Naehyuck Chang

- **Power Deregulation: Eliminating Off-Chip Voltage Regulation Circuitry From Embedded Systems** 105
Seunghoon Kim (*LG Electronics*), Robert P. Dick, Russ Joseph (*Northwestern University*)

- **Temperature-Aware Processor Frequency Assignment for MPSoCs Using Convex Optimization** 111
Srinivasan Murali (*LSI, EPFL & Stanford University*), Almir Mutapcic (*Stanford University*), David Atenza (*EPFL*), Rajesh Gupta (*University of California at San Diego*), Stephen Boyd (*Stanford University*), Giovanni De Micheli (*LSI, EPFL*)
- **Three-Dimensional Multiprocessor System-on-Chip Thermal Optimization** 117
Chong Sun, Li Shang (*Queen's University*), Robert P. Dick (*Northwestern University*)

Tuesday, October 2nd • 10:30–12:00

Keynote

Moderated by Jurgen Teich

- **Complexity Challenges Towards 4th Generation Communication Solutions** 123
Hermann Eul (*Infineon Technologies AG*)

Special Session I

Session Organizers: Radu Marculescu

- **Fresh Air: The Emerging Landscape of Design for Networked Embedded Systems** 124
Radu Marculescu (*Carnegie Mellon University*), Borivoje Nikolic, Alberto Sangiovanni-Vincentelli (*University of California*)

Tuesday, October 2nd • 13:30–15:30

Session 4A: Embedded Software

Session Chair: Joseph Buck, Session Co-chair: Rolf Ernst

- **Locality Optimization in Wireless Applications** 125
Javed Absar, Min Li, Praveen Raghavan, Andy Lambrechts, Murali Jayapala, Arnout Vandecappelle, Francky Catthoor (*IMEC*)
- **A Code-Generator Generator for Multi-Output Instructions** 131
Hanno Scharwaechter, Rainer Leupers, Gerd Ascheid, Heinrich Meyr (*RWTH Aachen University*), Jonghee M. Youn, Yunheung Paek (*Seoul National University*)
- **Influence of Procedure Cloning on WCET Prediction** 137
Paul Lokuciejewski, Heiko Falk, Martin Schwarzer (*University of Dortmund*), Peter Marwedel (*Embedded Systems Groups*), Henrik Theiling (*AbsInt Angewandte Informatik*)
- **Compile-Time Decided Instruction Cache Locking Using Worst-Case Execution Paths** 143
Heiko Falk, Sascha Plazar (*University of Dortmund*), Henrik Theiling (*AbsInt Angewandte Informatik*)

Session 4B: Advances in NoC Optimization

Session Chair: Twan Basten, Session Co-chair: Srinivasan Murali

- **Channel Trees: Reducing Latency by Sharing Time Slots in Time-Multiplexed Networks on Chip** 149
Andreas Hansson (*Eindhoven University of Technology*), Martijn Coenen, Kees Goossens (*NXP Semiconductors*)
- **Performance and Resource Optimization of NoC Router Architecture for Master and Slave IP Cores** 155
Glenn Leary, Krishna Mehta, Karam S. Chatha (*Arizona State University*)
- **Incremental Run-time Application Mapping for Homogeneous NoCs with Multiple Voltage Levels** 161
Chen-Ling Chou, Radu Marculescu (*Carnegie Mellon University*)
- **A Data Protection Unit for NoC-based Architectures** 167
Leandro Fiorin (*University of Lugano*), Gianluca Palermo (*Politecnico di Milano*), Slobodan Lukovic (*University of Lugano*), Cristina Silvano (*Politecnico di Milano*)

Tuesday, October 2nd • 16:00–17:30

Session 5A: System-Level Performance Analysis

Session Chair: Robert A. Walker, Session Co-chair: Hiroyuki Tomiyama

- **Complex Task Activation Schemes in System Level Performance Analysis** 173
Wolfgang Haid, Lothar Thiele (*Swiss Federal Institute of Technology*)
- **Improved Response Time Analysis of Tasks Scheduled under Preemptive Round-Robin** 179
Razvan Racu, Li Li, Rafik Henia, Arne Hamann, Rolf Ernst (*Technical University of Braunschweig*)
- **Probabilistic Performance Risk Analysis at System-Level**..... 185
Alexander Viehl, Markus Schwarz, Oliver Bringmann (*FZI Forschungszentrum Informatik*),
Wolfgang Rosenstiel (*FZI Forschungszentrum Informatik & Universität of Tübingen*)

Session 5B: Case Studies and Emerging Techniques

Session Chair: Reinaldo Bergamaschi, Session Co-chair: Rainer Dorsch

- **ESL Design and HW/SW Co-verification of High-end Software Defined Radio Platforms** 191
C. H. Ng, J. W. Weijers, M. Glassee, T. Schuster, B. Bougard, L. Van der Perre (*IMEC*)
- **Smart Driver for Power Reduction in Next Generation Bistable Electrophoretic Display Technology** 197
Michael A. Baker, Aviral Shrivastava, Karam S. Chatha (*Arizona State University*)
- **On the Impact of Manufacturing Process Variations on the Lifetime of Sensor Networks** 203
Siddharth Garg, Diana Marculescu (*Carnegie Mellon University*)

Wednesday, October 3rd • 10:30–12:00

Special Session II: Practical Approaches to System-level Performance Analysis

Session Organizer: Adam Donlin

- **Performance Modeling for Early Analysis of Multi-Core Systems** 209
Reinaldo Bergamaschi, Indira Nair, Gero Dittmann (*IBM T. J. Watson Research Center*),
Hiren Patel (*Virginia Polytechnic Institute and State University*),
Geert Janssen (*IBM T. J. Watson Research Center*), Nagu Dhanwada (*IBM EDA*),
Alper Buyuktosunoglu, Emrah Acar, Gi-Joon Nam, Dorothy Kucar, Pradip Bose, John Darringer
(*IBM T. J. Watson Research Center*), Guoling Han (*University of California*)
- **Bridging Gap between Simulation and Spreadsheet Study** 215
Antoine Perrin, Frank Ghenassia (*STMicroelectronics*)
- **Performance Analysis and Design Space Exploration for High-End Biomedical Applications: Challenges and Solutions** 217
Iyad Al Khatib (*Royal Institute of Technology*), Davide Bertozzi (*University of Ferrara*),
Axel Jantsch (*Royal Institute of Technology*), Luca Benini (*University of Bologna*)

Wednesday, October 3rd • 13:30–15:00

Session 6A: System-Level Synthesis

Session Chair: Christian Haubelt, Session Co-chair: Donatella Sciuto

- **A Low Power VLIW Processor Generation Method by Means of Extracting Non-redundant Activation Conditions** 227
Hirofumi Iwato, Keishi Sakanushi, Yoshinori Takeuchi, Masaharu Imai (*Osaka University*)

- **Scheduling and Voltage Scaling for Energy/Reliability Trade-offs in Fault-Tolerant Time-Triggered Embedded Systems**233
Paul Pop, Kåre Harbo Poulsen (*Technical University of Denmark*),
Viacheslav Izosimov, Petru Eles (*Linköping University*)
- **Reliable Multiprocessor System-On-Chip Synthesis**239
Changyun Zhu (*Queen's University*), Zhenyu (Peter) Gu, Robert P. Dick (*Northwestern University*),
Li Shang (*Queen's University*)

Session 6B: Embedded Systems Architecture

Session Chair: Wayne Wolf, Session Co-chair: Bruce Jacob

- **Aggressive Snoop Reduction for Synchronized Producer-Consumer Communication in Energy-Efficient Embedded Multi-Processors**.....245
Chenjie Yu, Peter Petrov (*University of Maryland*)
- **Predator: A Predictable SDRAM Memory Controller**251
Benny Akesson (*Technische Universiteit Eindhoven*),
Kees Goossens (*NXP Semiconductors Research & Delft University of Technology*),
Markus Ringhofer (*Graz University of Technology*)
- **Performance Improvement of Block Based NAND Flash Translation Layer**257
Siddharth Choudhuri, Tony Givargis (*University of California, Irvine*)

Wednesday, October 3rd • 16:00–17:30

Panel

- **Automotive Networks—Are New Busses and Gateways the Answer or Just Another Challenge?**263
Rolf Ernst (*Technische Universität Braunschweig*), Gernot Spiegelberg (*Siemens VDO Automotive AG*),
Thomas Weber (*DaimlerChrysler AG*), Herman Kopetz (*Technische Universität Wien*),
Alberto Sangiovanni-Vincentelli (*University of California at Berkeley*), Marek Jersak (*Symtavision GmbH*)

Author Index.....264