

2011 12th International Symposium on Quality Electronic Design

(ISQED 2011)

**Santa Clara, California, USA
14-16 March 2011**



**IEEE Catalog Number: CFP11250-PRT
ISBN: 978-1-61284-913-3**

TABLE OF CONTENTS
INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN

SESSION 1A: Device Aging: Analysis and Design

Chair: Hamid Mahmoodi
Co-Chair: Srinivas Bodapati

1A.1: Analysis and Mitigation of NBTI Aging in Register File: An End-To-End Approach	1
Saurabh Kothawade, Koushik Chakraborty, Sanghamitra RoyUtah State University, USA	
1A.2: Reducing Impact of Degradation on Analog Circuits by Chopper Stabilization and Autozeroing	8
Shailesh More, Florian Chouard, Doris Schmitt-LandsiedelTechnical University of Munich, Germany Michael Fulde Infineon Technologies AG, Villach, Austria	
1A.3: Circuit-Level Delay Modeling Considering both TDDB and NBTI.....	14
Hong Luo, Xiaoming Chen, Yu Wang, Yuchun Ma, Huazhong YangTsinghua Univ., China Jyothi Velamala, Yu CaoArizona State Univ., USA Vikas Chandra..... ARM R&D, USA	
1A.4: Modeling of Random Telegraph Noise under Circuit Operation -- Simulation and Measurement of RTN-Induced Delay Fluctuation	22
Kyosuke Ito, Takashi Matsumoto, Shinichi Nishizawa, Hiroki Sunagawa..... Kyoto University, Japan Kazutoshi Kobayashi..... Kyoto Institute of Technology, Japan Hidetoshi Onodera Kyoto University, JST, CREST, Japan	
1A.5: Modeling and Analyzing NBTI in the Presence of Process Variation.....	28
Taniya Siddiqua, Sudhanva Gurusurthi, Mircea Stan..... University of Virginia, USA	

SESSION 1B: Analog and 3D Integrated Circuits

Chair: Martin Wong
Co-Chair: Vamsi Srikantam

1B.1: A Novel Detailed Routing Algorithm with Exact Matching Constraint for Analog and Mixed Signal Circuits.....	36
Qiang Gao, Hailong Yao, Qiang Zhou, Yici Cai..... Tsinghua University, China	
1B.2: Signal Integrity Analysis and Optimization for 3D ICs.....	42
Chang Liu, Taigon Song, Sung Kyu Lim Georgia Institute of Technology, USA	
1B.3: 3DICE: 3D IC Cost Evaluation Based on Fast Tier Number Estimation	50
Cheng-Chi Chan, Yen-Ting Yu, Iris Hui-Ru Jiang National Chiao Tung University, Taiwan	

1B.4: Accurate Analysis of Substrate Sensitivity of Active Transistors in an Analog Circuit	56
Satoshi Takaya, Yoji Bando, Makoto Nagata Kobe University, Japan	
Toru Ohkawa, Toshiharu Takaramoto, Toshio Yamada, Masaaki Souda, Shigetaka Kumashiro, Tohru MogamiMIRAI-Selete, Japan	
1B.5: Full-Chip Analysis of Unintentional Forward Biased Diodes	62
Amir Grinshpon, Adam Segoli Schubert..... Freescale Semiconductor, USA	
Ziyang Lu..... Mentor Graphics, USA	

SESSION 1C: Low Power Circuits, Sensors, and Memories

Chair: Syed Alam

Co-Chair: Mark Budnik

1C.1: A 12.4μm² 133.4μW 4.56mV/$^{\circ}$C Resolution Digital On-Chip Thermal Sensing Circuit in 45nm CMOS Utilizing Sub-Threshold Operation.....	67
Basab Datta and Wayne Burleson University of Massachusetts - Amherst, USA	
1C.2: Effective Algorithm for Integrating Clock Gating and Power Gating to Reduce Dynamic and Active Leakage Power Simultaneously.....	74
Li Li, Ken Choi, Haiqing Nan Illinois Institute of Technology, USA	
1C.3: Transient and Fine-Grained Voltage Adaptation for Variation Resilience in VLSI Interconnects.....	80
Kyu-Nam Shim and Jiang Hu Texas A&M University, USA	
1C.4: A 128kb High Density Portless SRAM Using Hierarchical Bitlines and Thyristor Sense Amplifiers	87
Michael Wieckowski, Gregory Chen, Daeyeon Kim, David Blaauw, Dennis Sylvester University of Michigan, USA	
1C.5: Temperature Aware Energy Management for Real-Time Scheduling	91
Nikhil Gupta and Rabi Mahapatra Texas A&M University, USA	

SESSION 2A: Lithography and 3D Integration

Chair: Siddharth Garg

Co-Chair: Rajan Beera

2A.1: Coupling Timing Objectives with Optical Proximity Correction for Improved Timing Yield	97
Shayak Banerjee, Kanak Agarwal, Sani Nassif, James Culp, Lars Liebmann..... IBM Corp., USA	
Shayak Banerjee, Michael Orshansky..... University of Texas - Austin, USA	
2A.2: Self-Aligned Double Patterning (SADP) Layout Decomposition.....	103
Minoo Mirsaeeedi University of Waterloo, Canada	
J. Andres Torres..... Mentor Graphics Corp., USA	
Mohab Anis The American University in Cairo, Egypt	
2A.3: DFM: Impact Analysis in a High Performance Design	110
Stalin SM, Amit Brahme, Venkatraman Ramakrishnan, Ajoy Mandal Texas Instruments Pvt. Ltd., India	
2A.4: Metrics for Characterizing Machine Learning-Based Hotspot Detection Methods.....	116
Jen-Yi Wu, Malgorzata Marek-Sadowska..... University of California - Santa Barbara, USA	
Fedor Pikus Mentor Graphics Corporation, USA	
2A.5: Analysis of TSV-to-TSV Coupling with High-Impedance Termination in 3D ICs.....	122
Taigon Song, Chang Liu, Dae Hyun Kim, Sung Kyu Lim Georgia Institute of Technology, USA	
Jonghyun Cho, Joohee Kim, Jun So Pak, Seungyoung Ahn, Joungho Kim KAIST, Korea	
Kihyun Yoon Silicon Image, USA	
2A.6: 3D Stacked IC Layout Considering Bond Pad Density and Doubling for Manufacturing Yield Improvement.....	129
Ding-Ming Kwai and Chang-Tzu Lin Industrial Technology Research Institute, Taiwan	

SESSION 2B: New Ideas in Digital Design Automation

Chair: James Lei

Co-Chair: Jin He

2B.1: Compact Circuit Modeling of RF Characteristics of 1-D Nanostructures (Invited - abstract)	135
Cary Y. Yang Santa Clara University, USA	
2B.2: SCPlace: A Statistical Slack-Assignment Based Constructive Placer	136
Evriklis Kounalakis and Christos Sotiriou FORTH-ICS, Heraklion, Greece; and University of Crete, Greece	
2B.3: Application-Specific Network-on-Chip Synthesis: Cluster Generation and Network Component Insertion	144
Wei Zhong, Song Chen, Takeshi Yoshimura, Satoshi Goto Waseda University, Japan Bei Yu, Sheqin Dong Tsinghua University, China.	
2B.4: Novel and Efficient Min Cut based Voltage Assignment In Gate Level	150
Tao Lin, Sheqin Dong, Yuchun Ma, Ou He Tsinghua University, China Song Chen, Satoshi Goto Waseda University, Japan	
2B.5: Multi-Objective Optimization Techniques for VLSI Circuits	156
Fatemeh Kashfi, Safar Hatami, Massoud Pedram University of Southern California, USA	

SESSION 2C: System Frameworks and Tools

Chair: Makram Mansour

Co-Chair: Sudeep Pasricha

2C.1: A Design Time Simulator for Computer Architects	164
Sangeetha Sudhakarishnan, Francisco J. Mesa Martinez, Jose Renau University of California - Santa Cruz, USA	
2C.2: Constraint Generation for Software-Based Post-Silicon Bug Masking with Scalable Resynthesis Technique for Constraint Optimization	174
Chia-Wei Chang, Chien-Nan Jimmy Liu National Central University, Taiwan Hong-Zu Chou, Jie-Hong Roland Jiang, Chiu-Han Hsiao, Sy-Yen Kuo . National Taiwan University, Taiwan Kai-Hui Chang Avery Design Systems, Inc., USA	
2C.3: POSEIDON: A Framework for Application-Specific Network-on-Chip Synthesis for Heterogeneous Chip Multiprocessors	182
Soohyun Kwon, Jeonghun Cho Kyungpook National University, Korea Sudeep Pasricha Colorado State University, USA	
2C.4: A Complete Framework of Simultaneous Functional Unit and Register Binding with Skew Scheduling	189
Mineo Kaneko Japan Advanced Institute of Science and Technology, Japan	
2C.5: Virtual Hellfire Hypervisor: Extending Hellfire Framework for Embedded Virtualization Support	196
Alexandra Aguiar and Fabiano Hessel PUCRS, Brazil	
2C.6: A Low Overhead Fault Tolerant Routing Scheme for 3D Networks-on-Chip	204
Sudeep Pasricha and Yong Zou..... Colorado State University, USA	

SESSION 3A: Variation and Noise-Aware Design

Chair: Payman Zarkesh-Ha

Co-Chair: Riaz Nasseer

3A.1: Integrated Circuit-Architectural Framework for PSN Aware Floorplanning in Microprocessors	212
Mandar Padmawar AES Corporation, USA Sanghamitra Roy, Koushik Chakraborty..... Utah State University, USA	

3A.2: 0.45-V Operating V_t-Variation Tolerant 9T/18T Dual-Port SRAM	219
Hiroki Noguchi, Shunsuke Okumura, Tomoya Takagi, Koji Kugata, Hiroshi Kawaguchi Kobe University, Japan	
Masahiko YoshimotoKobe University, JST CREST, Japan	
3A.3: Power-Supply-Network Design in 3D Integrated Systems	223
Michael B Healy and Sung Kyu Lim Georgia Institute of Technology, USA	
3A.4: An Automated Design Methodology for Yield Aware Analog Circuit Synthesis in Submicron Technology	229
Sabyasachi Deyati and Pradip Mandal..... Indian Institute of Technology - Kharagpur, India	
3A.5: Process Variation Sensitivity of the Rotary Traveling Wave Oscillator	236
Ying Teng and Baris Taskin Drexel University, USA	

SESSION 3B: Physical Design Issues in Custom Circuits and FPGAs

Chair: Martin Wong

Co-Chair: Vamsi Srikantam

3B.1: Enhancement of Incremental Design for FPGAs Using Circuit Similarity	243
Xiaoyu Shi, Dahua Zeng, Yu Hu, Guohui Lin, Osmar Zaiane..... University of Alberta, Canada	
3B.2: On Discovery of “Missing” Physical Design Rules via Diagnosis of Soft-Faults	251
Aswin Sreedhar and Sandip Kundu.....University of Massachusetts at Amherst, USA	
3B.3: Mixed Non-Rectangular Block Packing for Non-Manhattan Layout Architectures	257
Meng-Chen Wu, Hung-Ming Chen, Jing-Yang Jou National Chiao Tung University, Taiwan	
3B.4: Optimizing Simulated Annealing on GPU: A Case Study with IC Floorplanning	263
Yiding Han, Sanghamitra Roy, Koushik Chakraborty Utah State University, USA	
3B.5: Floorplanning for High Utilization of Heterogeneous FPGAs	270
Nan Liu, Song Chen, Takeshi Yoshimura..... Waseda University, Japan	

SESSION 3C: Verification, Validation and Test

Chair: Sreejit Chakravarty

Co-Chair: Srivatsa Vasudevan

3C.1: Efficient Directed Test Generation for Validation of Multicore Architectures	276
Xiaoke Qin and Prabhat Mishra..... University of Florida, USA	
3C.2: Global Transaction Ordering in Network-on-Chips for Post-Silicon Validation	284
Amir Masoud Gharehbaghi and Masahiro Fujita University of Tokyo, Japan	
3C.3: On Evaluating Signal Selection Algorithms for Post-Silicon Debug	290
Eddie Hung and Steven J. E. Wilton University of British Columbia, Canada	
3C.4: Debugging and Optimizing High Performance Superscalar Out-of-order Processors Using Formal Verification Techniques	297
Bijan Alizadeh.....University of Tehran, Iran	
Masahiro Fujita..... University of Tokyo, Japan	
3C.5: RF BIST for ADPLL-based Polar Transmitters with Wide-Band DCO Gain Calibration	303
Leyi Yin and Peng Li Texas A&M University, USA	

SESSION 3P: Poster Session & Mixer

Chair: Keith Bowman

3P.1: A 90 nm Low-Power Successive Approximation Register for A/D Conversions	311
Mohamed Shaker and Magdy Bayoumi University of Louisiana at Lafayette, USA	
3P.2: A Low Noise CMOS Interface Circuit for Capacitive Liquid Crystal Chemical and Biological Sensor	316
Alireza Hassanzadeh and Robert G. Lindquist..... University of Alabama in Huntsville, USA	

3P.3: Block-Basis On-Line BIST Architecture for Embedded SRAM using Wordline and Bitcell Voltage Optimal Control	322
Masahiro Yoshikawa, Shunsuke Okumura, Yohei Nakata, Yuki Kagiya, Hiroshi Kawaguchi, Masahiko Yoshimoto..... Kobe University, Japan	
3P.4: pH Sensing with Temperature Compensation in a Molecular Biosensor for Drugs Detection	326
Daniela De Venuto Politecnico di Bari, Italy Sandro Carrara, Andrea Cavallini, Giovanni De Micheli..... EPFL, Switzerland	
3P.5: CMOS Diodes Operating Beyond Avalanche Frequency	332
Talal Al-Attar..... Santa Clara University, USA	
3P.6: Entropy-Reduced Hashing for Physical IP Management	338
Sandeep Koranne, John Ferguson, Bikram Garg, Manish Khanna..... Mentor Graphics, USA & India	
3P.7: A Physical Model for Tunable Patch Antennas	343
Benjamin Horwath and Talal Al-Attar Santa Clara University, USA	
3P.8: Model Analysis of Multi-Finger MOSFET Layout in Ring Oscillator Design	347
Bo Jiang and Tian Xia University of Vermont, USA	
3P.9: Crosstalk Aware Coupled Line Delay Tree Construction for On-chip Interconnects	353
Tuhina Samanta, Sanoara Khatun, Hafizur Rahaman Bengal Engineering and Science University, India Parthasarathi Dasgupta..... Indian Institute of Management - Calcutta, India	
3P.10: A Layer Prediction Method for Minimum Cost Three Dimensional Integrated Circuits	359
Tsu-Yun Hsueh, Hsiang-Hui Yang, Wei-Chieh Wu, Mely Chen Chi Chung Yuan Christian University, Taiwan	
3P.11: Delay Optimization Considering Power Saving in Dynamic CMOS Circuits	364
Kumar Yelamarthi..... Central Michigan University, USA Henry Chen Wright State University, USA	
3P.12: Capacitor Free Phase Locked Loop Design in 45nm	370
Anisha Seli, Hoa Nguyen, Lili He, Morris Jones San Jose State University, USA	
3P.13: Model Based Double Patterning Lithography (DPL) and Simulated Annealing (SA)	376
Rance Rodrigues and Sandip Kundu University of Massachusetts at Amherst, USA	
3P.14: Comparative BTI Reliability Analysis of SRAM Cell Designs in Nano-Scale CMOS Technology	384
Shreyas Kumar Krishnappa and Hamid Mahmoodi..... San Francisco State University, USA	
3P.15: Design Method of NOR-Type Comparison Circuit in CAM with Ground Bounce Noise Considerations	390
Changmin Jung LS Industrial Systems Co., Ltd., Korea Sanghyeon Baeg..... Hanyang Univeristy - ERICA, Korea ShiJie Wen, Richard Wong..... Cisco Systems Inc., USA	
3P.17: A 12-Bit CMOS Current Steering D/A Converter with a Fully Differential Voltage Output	398
Guoyuan Fu, H. Alan Mantooh, Jia Di University of Arkansas, USA	
3P.18: Fast Optimization of Nano-CMOS Mixed-Signal Circuits Through Accurate Metamodeling	405
Oleg Garitselov, Saraju Mohanty, Elias Kougianos University of North Texas, USA	
3P.19: CMP Monitoring and Prediction Based Metal Fill	411
Philippe Morey-Chaisemartin, Eric Beisser Xyalis, France Jean-Claude Marin, Lidwine Chaize, Pascal Guyader, Julien Rosa..... STmicroelectronics, France	
3P.20: Non-Gaussian Uncertainty Propagation in Statistical Circuit Simulation	417
Qian Ying Tang and Costas Spanos University of California - Berkeley, USA	
3P.21: New Category of Ultra-Thin Notchless 6T SRAM Cell Layout Topologies for Sub-22nm	425
Randy Mann and Benton Calhoun University of Virginia, USA	

3P.22: A Sensitivity-aware Methodology to Improve Cell Layouts for DFM Guidelines.....	431
Savithri Sundareswaran, Robert Maziasz, Vladimir Rozenfeld, Mikhail Sotnikov, Mukhanov Konstantin Freescale Inc., USA & Russia	
3P.23: Lithography-Aware Layout Modification Considering Performance Impact	437
Hongbo Zhang, Yuelin Du, Martin D. F. Wong University of Illinois Urbana-Champaign, USA Kai-Yuan Chao Intel Corp., USA	
3P.24: Tracking Hardware Evolution	442
Jose Augusto Nacif, Thiago Sousa Silva, Luiz Filipe Vieira, Claudionor Jose Coelho Jr., Antonio Otavio Fernandes Universidade Federal de Minas Gerais, Brazil Jose Augusto Nacif Universidade Federal de Viçosa, Brazil Alex Borges Vieira Universidade Federal de Juiz de Fora, Brazil	
3P.25: An Accurate and Scalable MOSFET Aging Model for Circuit Simulation	448
Bogdan Tudor, Joddy Wang, Zhaoping Chen, Robin Tan, Weidong Liu, Frank Lee Synopsys, Inc., USA	
3P.26: Fast Variational Static IR-Drop Analysis on the Graphical Processing Unit	452
Rasit Topaloglu Global Foundries, USA	
3P.27: Efficient Nanoscale VLSI Standard Cell Library Characterization Using a Novel Delay Model.....	458
Sandeep Miryala, Baljit Kaur, Bulusu Anand, Sanjeev Manhas IIT Roorkee, India	
3P.28: Occurrence Probability Analysis of a Path at the Architectural Level	464
Dheepakkumaran Jayaraman and Spyros Tragoudas Southern Illinois University - Carbondale, USA	
3P.29: Automatic Post-layout Flow Validation Tool for Deep Sub-Micron Process Design Kits	469
Pinping Sun, Cole Zemke, Wayne Woods, Nick Perez, Hailing Wang, Essam Mina, Barbara DeWitt IBM, USA	
3P.30: Switching Constraint-driven Thermal and Reliability Analysis of Nanometer Designs	473
Sri Krishna moorthy, Vishak Venkatraman, Yuri Apanovich, Thomas Burd, Anand Daga Advanced Micro Devices, USA	
3P.31: Separation of Communication and Computation in SystemC/TLM Modeling: A Feature-Oriented Approach	481
Jun Ye, Qingping Tan, Tun Li National University of Defense Technology, China	
3P.32: Integrated Scheduling, Allocation and Binding in High Level Synthesis using Multi Structure Genetic Algorithm Based Design Space Exploration System.....	486
Anirban Sengupta and Reza Sedaghat Ryerson University, Canada	
3P.33: Exploring Performance-Power Tradeoffs in Providing Reliability for NoC-Based MPSoCs	495
Hui Zhao, Mahmut Kandemir, Mary Jane Irwin Pennsylvania State University, USA	
3P.34: Stratus: Free Design of Highly Parametrized VLSI Modules Interoperable with Commercial Tools	502
Sophie Belloeil-Dupuis, Roselyne Chotin-Avot, Habib Mehrez University Paris VI, France	

SESSION 4A: Variation, Reliability, and Test

Chair: Fedor Pikus

Co-Chair: Narendra Devta-Prasanna

4A.1: Variation-Aware Stochastic Extraction with Large Parameter Dimensionality: Review and Comparison of State of the Art Intrusive and Non-intrusive Techniques (Invited)	508
Tarek El-Moselhy and Lucia Daniel Massachusetts Institute of Technology, USA	
4A.2: Digitally Programmable SRAM Timing for Nano-Scale Technologies	518
Adam Neale and Manoj Sachdev University of Waterloo, Canada	
4A.3: Layout-aware Mismatch Modeling for CMOS Current Sources with D/A Converter Analysis.....	525
Bo Liu, Qing Dong, Bo Yang, Jing Li, Shigetoshi Nakatake University of Kitakyushu, Japan	

4A.4: Using NMOS Transistors as Switches for Accuracy and Area-efficiency in Large-scale Addressable Test Array	533
Weiwei Pan, Jie Ren, Yongjun Zheng, Zheng Shi, Xiaolang Yan..... Zhejiang University, China	
4A.5: A Simple Array-Based Test Structure for the AC Variability Characterization of MOSFETs	539
Karthik Balakrishnan, Duane Boning.....Massachusetts Institute of Technology, USA	
Keith Jenkins..... IBM T.J. Watson Research Center, USA	

SESSION 4B: Package and Processor Co-Design for Reliability and Signal/Power Integrity

Chair: Lalitha Immaneni
Co-Chair: Kamesh Gadepally

4B.1: Reliability - A Highly Important Product Attribute for the World's Poorest Consumers (Invited)	545
Joseph Fjelstad..... Verdant Electronics, USA	
4B.2: Cost-Effective Optimization of Serial Link System for Signal Integrity and Power Integrity	548
Raj Kumar Nagpal, Rakesh Malik..... STMicroelectronics Pvt. Ltd, India	
Jai Narayan Tripathi.....IIT Bombay,India	
4B.3: Package-Chip Co-Design to Increase Flip-Chip C4 Reliability	553
Sheldon Logan and Matthew Guthaus.....University of California - Santa Cruz, USA	
4B.4: Maximizing Hotspot Temperature: Wavelet based Modelling of Heating and Cooling Profile of Functional Workloads	559
Sudarshan Srinivasan, Kunal P Ganeshpure, Sandip Kundu...University of Massachusetts Amherst, USA	

SESSION 4C: System Design Considerations

Chair: Rajesh Berigei
Co-Chair: Houman Homayoun

4C.2: Process Variation Aware System-level Load Assignment for Total Energy Minimization using Stochastic Ordering	566
Shahin Golshan, Eli Bozorgzadeh.....University of California - Irvine, USA	
Love Singhal..... Synopsys, Inc., USA	
4C.3: A Low Cost Approach to Calibrate On-Chip Thermal Sensors	572
Krishna Bharath, Chunhua Yao, Nam Sung Kim, Parameswaran Ramanathan, Kewal Saluja.....University of Wisconsin - Madison, USA	
4C.4: Maximizing Throughput of Temperature-Constrained Multi-Core Systems with 3D-Stacked Cache Memory	577
Kyungsu Kang, Jongpil Jung, Chong-Min Kyung.....KAIST, Korea	
Sungjoo Yoo..... POSTECH, Korea	

SESSION 5A: Error-Resilient Design

Chair: Riaz Naseer
Co-Chair: Srinivas Bodapati

5A.1: Design and Analysis of Metastable-Hardened and Soft-Error Tolerant High-Performance, Low-Power Flip-Flops	583
David Li, David Rennie, Pierce Chuang, David Nairn, Manoj Sachdev..... University of Waterloo, Canada	
5A.2: ERAVC: Enhanced Reliability Aware NoC Router	591
M. h Neishaburi and Zeljko Zilic.....McGill University, Canada	
5A.3: SEU Tolerant SRAM Cell	597
Sudipta Sarkar, Anubhav Adak, Virendra Singh.....Indian Institute of Science - Bangalore, India	
Kewal Saluja.....University of Wisconsin - Madison, USA	
Masahiro Fujita.....University of Tokyo, Japan	

5A.4: Soft Error Reduction through Gate Input Dependent Weighted Sizing in Combinational Circuits	603
Warin Sootkaneung and Kewal K Saluja.....	University of Wisconsin - Madison, USA
5A.5: Low Power Latch Design in Near Sub-Threshold Region to Improve Reliability for Soft Error ..	611
Sandeep Sriram, Haiqing Nan, Ken Choi.....	Illinois Institute of Technology, USA
5A.6: BCH Code Based Multiple Bit Error Correction in Finite Field Multiplier Circuits	615
Mahesh Poolakkaparambil, Abusaleh Jabir.....	Oxford Brookes University, UK
Jimson Mathew, Dhiraj Pradhan.....	University of Bristol, UK
Saraju Mohanty.....	University of North Texas, USA

SESSION 5B: Routing, Signal Integrity, and Timing Closure

Chair: Martin Wong

Co-Chair: Vamsi Srikantam

5B.1: A Novel Fine-Grain Track Routing Approach for Routability and Crosstalk Optimization	621
Zhongdong Qi, Qiang Zhou, Yanming Jia, Yici Cai, Hailong Yao.....	Tsinghua University, China
Zhuoyuan Li.....	Magma Design Automation Inc., USA
5B.2: Redundant Via Insertion under Timing Constraints	627
Chi-Wen Pan and Yu-Min Lee.....	National Chiao-Tung University, Taiwan
5B.3: A New ECO Technology For Functional Changes and Removing Timing Violations	634
Jui-Hung Hung, Yao-Kai Yeh, Yung-Sheng Tseng, Tsai-Ming Hsieh.....	Chung Yuan Christian University,
5B.4: The Effect of SRNR on Timing Characteristics of Signal Busses	639
Bassel Soudan	University of Sharjah, UAE
5B.5: Gridless Wire Ordering, Sizing and Spacing with Critical Area Minimization	646
Yu-Wei Lee, Yen-Hung Lin, Yih-Lang Li.....	National Chiao-Tung University, Taiwan
5B.6: Clock Planning for Multi-Voltage and Multi-Mode Designs	654
Chang-Cheng Tsai, Tzu-Hen Lin, Shin-Han Tsai, Hung-Ming Chen	
.....	National Chiao Tung University, Taiwan
Tzu-Hen Lin.....	National Taiwan University, Taiwan

SESSION 5C: Power Delivery and Estimation

Chair: Mark Budnik

Co-Chair: Syed Alam

5C.1: Fast Power Delivery Network Analyzer	659
Bosun Hwang, Jongeun Koo, Chanseok Hwang, Younghoi Cheon,	
Sooyoung Ahn, Jongbae Lee, Moonhyun Yoo	Samsung Electronics, Korea
5C.2: Efficient Checking of Power Delivery Integrity for Power Gating	663
Zhiyu Zeng, Peng Li	Texas A&M University, USA
Zhuo Feng	Michigan Technological University, USA
5C.3: An Efficient Statistical Chip-Level Total Power Estimation Method Considering Process Variations with Spatial Correlation	671
Zhigang Hao, Guoyong Shi	Shanghai Jiao Tong University, China
Zhigang Hao, Sheldon X.-D. Tan	University of California - Riverside, USA
5C.4: Statistical Full-Chip Dynamic Power Estimation Considering Spatial Correlations	677
Zhigang Hao, Guoyong Shi	Shanghai Jiao Tong University, China
Zhigang Hao, Ruijing Shen, Sheldon X.-D. Tan	University of California - Riverside, USA
Bao Liu	University of Texas at San Antonio, USA
Yici Cai	Tsinghua University, China
5C.5: Stepped Supply Voltage Switching for Energy Constrained Systems	683
Sudhanshu Khanna, Kyle Craig, Yousef Shakhshsheer, Saad Arrabi,	
John Lach, Benton Calhoun	University of Virginia, USA

5C.6: Minimum Energy CMOS Design with Dual Subthreshold Supply and Multiple Logic-Level Gates.....	689
Kyungseok Kim and Vishwani Agrawal	Auburn University, USA

SESSION 6A: Design Methodologies for CMOS and Beyond

Chair: Saraju Mohanty
Co-Chair: Rasit Topaloglu

6A.1: Design of Ultra-low-leakage Logic Gates and Flip-flops in High-performance FinFET Technology (Invited).....	695
Ajay Bhoj and Niraj Jha	Princeton University, USA
6A.2: Timing Yield Estimation of Carbon Nanotube-based Digital Circuits in the Presence of Nanotube Density Variation and Metallic-Nanotubes.....	703
Behnam Ghavami, Mohsen Raji, Hossein Pedram	Amirkabir University of Technology, Iran
6A.3: Measuring Within-Die Spatial Variation Profile through Power Supply Current Measurements.....	711
Jim Plusquellic.....	University of New Mexico, USA
Dhruva Acharyya.....	Verigy Ltd., USA
Kanak Agarwal	IBM Corp., USA
6A.4: Analysis of Within-Die Process Variation in 65nm FPGAs.....	716
Tim Tuan, Austin Lesea, Chris Kingsley, Steve Trimberger	Xilinx Inc., USA
6A.5: Estimating the Probability Density Function of Critical Path Delay via Partial Least Squares Dimension Reduction.....	721
Yu Ben and Costas Spanos	University of California - Berkeley, USA

SESSION 6B: Advanced Devices and Manufacturing Technologies

Chair: Paul Tong
Co-Chair: Bao Liu

6B.1: Complementary Nano-Electro-Mechanical Switch for Ultra-Low-Power Applications: Design and Modeling.....	728
Khawla Alzoubi.....	Tafila Technical University, Jordan
Daniel G. Saab, Sijing Han.....	Case Western Reserve University, USA
Massood Tabib-Azar	University of Utah, USA
6B.2: Interconnection Aspects of Spin Torque Devices: Delay, Energy-Per-Bit, and Circuit Size Modeling.....	736
Shaloo Rakheja and Azad Naeemi.....	Georgia Institute of Technology, USA
6B.3: Scaled LTPS TFTs for Low-Cost Low-Power Applications	745
Soo Youn Kim, Selin Baytok, Kaushik Roy.....	Purdue University, USA
6B.4: Mitigating TSV-induced Substrate Noise in 3-D ICs using GND Plugs	751
Nauman Khan, Soha Hassoun	Tufts University, USA
Syed Alam	Everspin Technologies Inc., USA
6B.5: Device and Circuit Implications of Double-Patterning - A Designer's Perspective	757
Rasit Onur Topaloglu	Global Foundries, USA

SESSION 6C: New Ideas in Analog Design Automation

Chair: Masahiro Fujita
Co-Chair: Shireesh Verma

6C.1: Automatic Generation of Saturation Constraints and Performance Expressions for Geometric Programming Based Analog Circuit Sizing	761
Supriyo Maji, Samiran Dam, Pradip Mandal.....	Indian Institute of Technology – Kharagpur, India

6C.2: Constructive AIG Optimization Considering Input Weights	769
Thiago Figueiró, Renato Perez Ribas, André Reis..... Universidade Federal do Rio Grande do Sul, Brazil	
6C.3: Integrated Hierarchical Synthesis of Analog/RF Circuits with Accurate Performance Mapping	777
Kuo-Hsuan MengUniversity of Illinois Urbana-Champaign, USA	
Po-Cheng Pan, Hung-Ming Chen..... National Chiao Tung University, Taiwan	
6C.4: A Fully Pipelined Implementation of Monte Carlo Based SSTA on FPGAs	785
Hiroshi Yuasa, Hiroshi Tsutsui, Hiroyuki Ochi, Takashi Sato Kyoto University, Japan	
6C.5: Multi-mode Redundancy Removal	791
Stephen Plaza Janelia Farm Research Campus, USA	
Prashant Saxena, Thomas Shiple, Pei-Hsin Ho Synopsys, USA	