

**2011 IEEE 19th Annual
International Symposium on Field-
Programmable Custom Computing
Machines**

(FCCM 2011)

**Salt Lake City, Utah, USA
1 – 3 May 2011**



IEEE Catalog Number: CFP11054-PRT
ISBN: 978-1-61284-277-6

IEEE International Symposium on Field-Programmable Custom Computing Machines

FCCM 2011

Table of Contents

Message from the General and Program Chairs	x
Organizing Committee	xii
Program Committee	xiii
Additional Reviewers	xv
Preconference Workshop Summary	xvi
Panel Session Summary	xvii
Sponsors	xviii

Reconfigurable Computing

A Sparse Matrix Personality for the Convey HC-1	1
<i>Krishna K. Nagar and Jason D. Bakos</i>	
Modeling Dynamically Reconfigurable Systems for Simulation-Based	
Functional Verification	9
<i>Lingkan Gong and Oliver Diessel</i>	
Mixed Precision Processing in Reconfigurable Systems	17
<i>Gary C.T. Chow, K.W. Kwok, Wayne Luk, and Philip Leong</i>	
Dynamic Communication in a Coarse Grained Reconfigurable Array	25
<i>Robin Panda and Scott Hauck</i>	
Run-Time Resource Allocation for Simultaneous Multi-tasking in Multi-core	
Reconfigurable Processors	29
<i>Waheed Ahmed, Muhammad Shafique, Lars Bauer, Manuel Hammerich, Jörg Henkel, and Juergen Becker</i>	
An Autonomous Vector/Scalar Floating Point Coprocessor for FPGAs	33
<i>Jainik Kathiara and Miriam Leeser</i>	

Hecto-Scale Frame Rate Face Detection System for SVGA Source on FPGA Board	37
<i>Zheng Ding, Feng Zhao, Tinghui Wang, Wei Shu, and Min-You Wu</i>	

Comparing Implementations of Applications on Different Architectures

An FPGA Implementation of Information Theoretic Visual-Saliency System and Its Optimization	41
<i>Sungmin Bae, Yong Cheol Peter Cho, Sungho Park, Kevin M. Irick, Yongseok Jin, and Vijaykrishnan Narayanan</i>	
Scalable, High Performance Fourier Domain Optical Coherence Tomography: Why FPGAs and Not GPGPUs	49
<i>Jian Li, Marinko V. Sarunic, and Lesley Shannon</i>	
Architecture, Design, and Experimental Evaluation of a Lightfield Descriptor Depth Buffer Algorithm on Reconfigurable Logic and on a GPU	57
<i>Matina Lakka, Grigoris Chrysos, Ioannis Papaefstathiou, and Apostolos Dallas</i>	
Implementation and Performance Analysis of SEAL Encryption on FPGA, GPU and Multi-core Processors	65
<i>Kostas Theoharoulis, Charalampos Antoniadis, Nikolaos Bellas, and Christos D. Antonopoulos</i>	

Applications I

FPGA Communication Framework	69
<i>Peter Lieber and Brad Hutchings</i>	
Efficient Calculation of Pairwise Nonbonded Forces	73
<i>Matt Chiu, Md. Ashfaquzzaman Khan, and Martin C. Herbordt</i>	
High Performance IP Lookup on FPGA with Combined Length-Infix Pipelined Search	77
<i>Yi-Hua E. Yang, Oguzhan Erdem, and Viktor K. Prasanna</i>	
A Scalable Multi-FPGA Platform for Complex Networking Applications	81
<i>Sascha Mühlbach and Andreas Koch</i>	
An FPGA-Based Optical IOH Architecture for Embedded System	85
<i>Liu Ling, Zhuang Jincan, Zhu Qianying, Zhu Shunyu, Zhang Zhiyuan, Zhang Xinxin, Cao Lu, Yu Zhihong, Wu Xiangbin, and Liu Dong</i>	
On Comparing Financial Option Price Solvers on FPGA	89
<i>Qiwei Jin, Wayne Luk, and David B. Thomas</i>	
Low-Latency FPGA Based Financial Data Feed Handler	93
<i>Robin Pottathuparambil, Jack Coyne, Jeffrey Allred, William Lynch, and Vincent Natoli</i>	

Design and Implementation of an FPGA-Based Real-Time Face Recognition System	97
<i>Janarbek Matai, Ali Irturk, and Ryan Kastner</i>	
FPGA-Based Solid-State Drive Prototyping Platform	101
<i>Yu Cai, Erich F. Haratsch, Mark McCartney, and Ken Mai</i>	
Accelerating Statistical LOR Estimation for a High-Resolution PET Scanner Using FPGA Devices and a High Level Synthesis Tool	105
<i>Zhong-Ho Chen, Alvin W.Y. Su, Ming-Ting Sun, and Scott Hauck</i>	
SYSCORE: A Coarse Grained Reconfigurable Array Architecture for Low Energy Biosignal Processing	109
<i>Kunjan Patel, Séamas McGettrick, and Chris J. Bleakley</i>	
High-Throughput, Lossless Data Compression on FPGAs	113
<i>Bharat Sukhwani, Bulent Abali, Bernard Brezzo, and Sameh Asaad</i>	

Tools

HMFflow: Accelerating FPGA Compilation with Hard Macros for Rapid Prototyping	117
<i>Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent Nelson, and Brad Hutchings</i>	
Automatic HDL-Based Generation of Homogeneous Hard Macros for FPGAs	125
<i>Sebastian Korf, Dario Cozzi, Markus Koester, Jens Hagemeyer, Mario Porrmann, Ulrich Rückert, and Marco D. Santambrogio</i>	
Using Functional Programming to Generate an LDPC Forward Error Corrector	133
<i>Andy Gill, Tristan Bull, Dan DePardo, Andrew Farmer, Ed Komp, and Erik Perrins</i>	

Reconfigurable Computing in the Cloud

Reconfigurable Data Processing for Clouds	141
<i>Anil Madhavapeddy and Satnam Singh</i>	

Architecture and Systems

TMbox: A Flexible and Reconfigurable 16-Core Hybrid Transactional Memory System	146
<i>Nehir Sonmez, Oriol Arcas, Otto Pflucker, Osman S. Unsal, Adrián Cristal, Ibrahim Hur, Satnam Singh, and Mateo Valero</i>	
The PowerPC 405 Memory Sentinel and Injection System	154
<i>Mark Bucciero, John Paul Walters, Roger Moussalli, Shanyuan Gao, and Matthew French</i>	

Checkpoint/Restart and Beyond: Resilient High Performance Computing with FPGAs	162
---	-----

Andrew G. Schmidt, Bin Huang, Ron Sass, and Matthew French

FUSE: Front-End User Framework for O/S Abstraction of Hardware Accelerators	170
--	-----

Aws Ismail and Lesley Shannon

High-Level Synthesis

Multilevel Granularity Parallelism Synthesis on FPGAs	178
---	-----

*Alexandros Papakonstantinou, Yun Liang, John A. Stratton, Karthik Gururaj,
Deming Chen, Wen-Mei W. Hwu, and Jason Cong*

Synthesis of Platform Architectures from OpenCL Programs	186
--	-----

Muhsen Owaida, Nikolaos Bellas, Konstantis Daloukas, and Christos D. Antonopoulos

Programming Real-Time Autofocus on a Massively Parallel Reconfigurable Architecture Using Occam-pi	194
---	-----

Zain-ul-Abdin, Anders Ahlander, and Bertil Svensson

Towards Synthesis-Free JIT Compilation to Commodity FPGAs	202
---	-----

Davor Capalija and Tarek S. Abdelrahman

Automated Placement for Parallelized FPGA FFTs	206
--	-----

Suraj Gowda, Aaron Parsons, Robert Jarnot, and Dan Werthimer

Reducing the Energy Cost of Irregular Code Bases in Soft Processor Systems	210
--	-----

*Manish Arora, Jack Sampson, Nathan Goulding-Hotta, Jonathan Babb,
Ganesh Venkatesh, Michael Bedford Taylor, and Steven Swanson*

Extending Force-Directed Scheduling with Explicit Parallel and Timed Constructs for High-Level Synthesis	214
---	-----

Rohit Sinha and Hiren D. Patel

Applications II

String Matching in Hardware Using the FM-Index	218
--	-----

Edward Fernandez, Walid Najjar, and Stefano Lonardi

Accelerating Phylogeny-Aware Short DNA Read Alignment with FPGAs	226
--	-----

Nikolaos Alachiotis, Simon A. Berger, and Alexandros Stamatakis

Scalable Streaming-Array of Simple Soft-Processors for Stencil Computations with Constant Memory-Bandwidth	234
---	-----

Kentaro Sano, Yoshiaki Hatsuda, and Satoru Yamamoto

Memory-Efficient IPv4/v6 Lookup on FPGAs Using Distance-Bounded Path Compression	242
---	-----

Hoang Le, Weirong Jiang, and Viktor K. Prasanna

Posters

A Key Size Configurable High Speed RSA Coprocessor	250
<i>E. Castillo, J. Castillo, J. Cano, P. Huerta, and J.I. Martínez</i>	
A Model for Peak Matrix Performance on FPGAs	251
<i>Colin Y. Lin, Hayden K.-H. So, and Philip H.W. Leong</i>	
Reconsideration of Computing Paradigms and a Novel Reconfigurable Architecture	252
<i>Ming Yan, Ziyu Yang, Sikun Li, and Liu Yang</i>	
Hybrid Data Structure for IP Lookup in Virtual Routers Using FPGAs	253
<i>Oguzhan Erdem, Hoang Le, Viktor Prasanna, and Cüneyt F. Bazlamaççi</i>	
FPGA Architecture of Generalized Laguerre-Volterra MIMO Model for Neural Population Spiking Activities	254
<i>Will X.Y. Li, Ray C.C. Cheung, Wei Zhang, Rosa H.M. Chan, Dong Song, and Theodore W. Berger</i>	
Implementation and Performance Comparison of the Motion Compensation Kernel of the AVS Video Decoder on FPGA, GPU and Multicore Processors	255
<i>M. Owaida, N. Bellas, C.D. Antonopoulos, K. Daloukas, Ch. Antoniadis, K. Krommydas, and G. Tsoumplekas</i>	
Author Index	256