

2011 VII Southern Conference on Programmable Logic

(SPL 2011)

**Cordoba, Argentina
13 – 15 April 2011**



IEEE Catalog Number: CFP1121B-PRT
ISBN: 978-1-4244-8847-6

Table of Contents

Poster Session 1

A DDR3 Memory Based Time Interleaving FPGA Implementation For ISDB-T Standard <i>Edgardo Marchi, Marcos Cervetto, Marcelo Tenorio</i>	1
FPGA implementation of two very low complexity LDPC decoders <i>Jorge Castiñeira, Miguel Rabini, Claudio González, Carlos Gayoso, Leonardo Arnone</i>	7
N-Continuous OFDM Signal Analysis of FPGA-Based Transmissions <i>Enrique Lizarraga, Victor Sauchelli, Gabriel Maggio</i>	13
High speed acquisition and storage platform for SDR applications development <i>Jorge Cogo, Javier García, Pedro Roncagliolo, Carlos Muravchik</i>	19
Framer Design, Verification and Prototyping for G.709 Optical Transport Networks <i>Jorge Finochietto, Román Arenas, Ulises Morales, Ramiro Lopez</i>	25
A Novel Low-Latency Parallel Architecture for Digital PLL with Application to Ultra-High Speed Carrier Recovery Systems <i>Pablo Gianni, Hugo Carrer, Graciela Corral-Briones, Mario Hueda</i>	31
Hardware Primitives for Packet Flow Processing Architectures <i>Jorge Finochietto, Carlos Zerbini, Santiago Paz</i>	37

Oral Session: Embedded Soft Processors

Customizable Security-Aware Cache for FPGA-based Soft Processors <i>Maciej Kurek, Ioannis Ilkos, Wayne Luk</i>	45
Custom FPGA-based Micro-architecture for Streaming Computing <i>Jose Alves, Pedro Diniz</i>	51
Known-Blocking. Synchronization method for reliable processor using TMR and DPR in SRAM FPGAs <i>Aitor Morillo, Armando Astarloa, Jesus Lázaro, Unai Bidarte, Jaime Jimenez</i>	57

Poster Session 2

An Unified Approach for Convolution-Based Image Filtering on Reconfigurable Systems <i>Camilo Sánchez Ferreira, Jones Yudi Mori, Carlos Llanos, Pedro Berger, Daniel Muñoz</i>	63
An example of rapid design of Power electronics control with FPGA in MATLAB/Simulink <i>Juan Tettamanti, Alejandro Latini, Miguel Aguirre</i>	69
Design of a FPGA based position PI servo controller for a DC motor with dry friction <i>Luis Castaño Londoño, Gustavo Osorio</i>	75
An extensible code generation framework for heterogeneous architectures based on IP-XACT <i>Thomas Perry, Richard Walke, Khaled Benkrid</i>	81
Power Estimations vs. Power Measurements in Cyclone III Devices <i>Juan Oliver, Eduardo Boemo</i>	87
Balanced Bipartitioning of a Multiweighted Hypergraph for Heterogeneous FPGAs <i>Sagnik Mukhopadhyay, Pritha Banerjee, Susmita Sur-Kolay</i>	91
Ultra Wideband Digital Receiver Implemented on FPGA for Mobile Robot Indoor Self-Localization <i>Marcelo Segura, Cristian Sisterna, Martin Guzzo, Gustavo Ensinck, Carlos Gil</i>	97

Oral Session: Modelling, Simulation and Emulation Applications

FPGA-Based Random Pulse Generator For Emulation of a Neutron Detector System in a Nuclear Reactor <i>Franco Ferrucci, Claudio Verrastro, Gloria Ríos, Daniel Estryk</i>	103
Experiences applying framework-based functional verification to a design for programmable logic <i>Oscar Goñi, Martín Vazquez, Gustavo Sutter, Elías Todorovich</i>	109
Python as a Hardware Description Language: A Case Study <i>Jose I. Villar, Jorge Juan Chico, Manuel Jesus Bellido, Julian Viejo, David Guerrero Martos, Jan Decaluwe</i>	117
Synthesis of Robust Controllers for GALS FPGA from Multi-Burst Graph Specification <i>Duarte Oliveira, Eduardo Lussari</i>	123

Oral Session: Image and Video Processing

A H.264/AVC Quarter-Pixel Motion Estimation Refinement Architecture Targeting High Resolution Videos <i>Marcel Corrêa, Mateus Schoenknetch, Luciano Agostini</i>	131
Multichannel SDRAM Controller Design for H.264/AVC Video Decoder <i>Alexsandro Bonatto, André Soares, Altamiro Susin</i>	137
Architecture driven memory allocation for FPGA Based Real-Time Video Processing Systems <i>Benny Thörnberg, Mattias O'Nils, Najeem Lawal</i>	143

Oral Session: High-Speed Design Techniques

An Euler Solver Accelerator in FPGA for Computational Fluid Dynamics Applications <i>Diego Sanchez-Roman, Gustavo Sutter, Sergio Lopez-Buedo, Ivan Gonzalez, Francisco Gomez-Arribas, Javier Aracil</i>	149
The MPRACE Framework: An Open Source Stack for Communication with custom FPGA-based Accelerators <i>Guillermo Marcus, Wenxue Gao, Andreas Kugel, Reinhard Maenner</i>	155
FPGA Implementation of an Ultra-High Speed ADC Interface <i>Cristian Sisterna, Marcelo Segura, Martin Guzzo, Gustavo Ensinck, Carlos Gil</i>	161

Poster Session 3:

FPGA implementation of a Dynamic-Clamp system. <i>Walter Bast, Damián Dellavale, Fabian Bonetto</i>	167
Hardware Particle Swarm Optimization with Passive Congregation for Embedded Applications <i>Daniel Munoz, Carlos Llanos, Leandro dos Santos Coelho, Mauricio Ayala Rincón</i>	173
Spanning Forests In Constant Time Using FPGAS Applied To Network Design Problems <i>Tiago Silva, Marcilyanne Moreira Gois, Paulo Matias, Aldexandre Delbem, Eduardo Marques, Vanderlei Bonato</i>	179
FPGA Implementation of a Chaotic Oscillator Using RK4 Method <i>Luciana De Micco, Hilda Larrondo</i>	185
Security-Centric FPGA CAD Tools to Balance Dual-Rail Routing in WDDL Designs <i>Amouri Emna, Zied Marrakchi, Habib Mehrez</i>	191
Intelligent FPGA based system for shape recognition <i>Emerson Pedrino, Orides Morandin Jr., Valentin Roda, Edilson Kato</i>	197
A Novel Method for Secure IP Deployment in Embedded Systems <i>Sunil Malipatlolla, Sorin Alexander Huss</i>	203

Oral Session: Dynamic/Runtime Reconfiguration

A reconfigurable GF(2^m) elliptic curve cryptographic coprocessor <i>Miguel Morales-Sandoval, Claudia Feregrino-Uribe, Ignacio Alredo-Badillo, Rene Cumplido</i>	
209	
Using partial reconfigurability to aid in debugging of FPGA designs <i>Andreas Ehliar, Jacob Siverskog</i>	215
Soft Error in FPGA-Implemented Asynchronous Circuits <i>Weidong Kuang, Yu Bai</i>	221
A Dynamic Buffer Resize Technique for Networks-on-Chip on FPGA <i>Mário Véstias, Horácio Neto</i>	227

Oral Session: Telecommunications and DSP Applications

A High Data Rate BPSK Receiver Implementation in FPGA for High Dynamics Applications <i>Juan Maya, Nicolás Casco, Pedro Roncagliolo, Javier García</i>	233
Implementation of a configuration server for a hardware SNTP synchronization platform based on FPGA <i>Juan Quiros, Julian Viejo, Alejandro Millan, Alejandro Muñoz, Jose I. Villar, David Guerrero Martos</i>	239
Fast Parallel Audio Fingerprinting Implementation in Reconfigurable Hardware and GPUs <i>José Ignacio Martínez, Jaime Vitola Oyaga, Cesar Pedraza Bonilla, Adriana Sanabria Borbón</i>	245

Oral Session: Computer Arithmetic

A FPGA IEEE-754-2008 Decimal64 Floating-Point Adder/Subtractor <i>Carlos Minchola, Martín Vazquez, Gustavo Sutter</i>	251
Iterative Decimal Multiplication using Binary Arithmetic <i>Mário Véstias, Horácio Neto</i>	257
A Suitable FPGA Implementation of Floating-Point Matrix Inversion based on Gauss-Jordan Elimination <i>Janier Arias, Ricardo Pezzuol Jacobi, Carlos Llanos, Mauricio Ayala Rincón</i>	263

Tutorial Session

FPGA and ASIC convergence <i>Carlos Valderrama, Julio Dondo Gazzano, Paulo Da Cunha Possa, Laurent Jojczyk</i>	269
---	-----