

# **2011 IEEE International Conference on IC Design & Technology**

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## Session A: I/O Circuits and ESD Protection

### Transient-to-Digital Converter to Detect Electrical Fast Transient (EFT) Disturbance for System Protection Design \$\$\$

Cheng-Cheng Yen<sup>1</sup>, Wan-Yen Lin<sup>1</sup>, Ming-Dou Ker<sup>1,2</sup>, Ching-Ling Tsai<sup>3</sup>, Shih-Fan Chen<sup>3</sup>, Tung-Yang Chen<sup>3</sup>

<sup>1</sup>Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

<sup>2</sup>Department of Electronics Engineering, I-Shou University, Kaohsiung, Taiwan

<sup>3</sup>Himax Technologies Inc., Taiwan

### ESD RF Protections in Advanced CMOS Technologies and its Parasitic Capacitance Evaluation \$\$)

Ph. Galy<sup>1</sup>, J. Jimenez<sup>1</sup>, P. Meuris<sup>2</sup>, W. Schoenmaker<sup>2</sup>, O. Dupuis<sup>2</sup>

<sup>1</sup>STMicroelectronics, Crolles, France

<sup>2</sup>MAGWEL NV, Leuven, Belgium

### Design of Low-Leakage Power-Rail ESD Clamp Circuit with MOM Capacitor and STSCR in a 65-nm CMOS Process \$\$-

Po-Yen Chiu<sup>1</sup>, Ming-Dou Ker<sup>1,2</sup>

<sup>1</sup>Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

<sup>2</sup>Dept. of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan

## Session B: Advanced Transistor/Material

### Invited Paper: Low power UTBOX and Back Plane (BP) FDSOI technology for 32nm node and below \$%

C. Fenouillet-Beranger<sup>1,2</sup>, P. Perreau<sup>1,2</sup>, L. Tosti<sup>2</sup>, O. Thomas<sup>2</sup>, J-P. Noel<sup>2</sup>, T. Benoist<sup>1</sup>, O. Weber<sup>2</sup>, F. Andrieu<sup>2</sup>, A. Bajolet<sup>1</sup>, S. Haendler<sup>1</sup>, M. Cassé<sup>2</sup>, X. Garros<sup>2</sup>, K.K. Bourdelle<sup>3</sup>, F. Boedt<sup>3</sup>, O. Faynot<sup>2</sup>, F. Boeuf<sup>1</sup>

<sup>1</sup>STMicroelectronics, Crolles, France

<sup>2</sup>CEA/LETI-Minatec, Grenoble, France

<sup>3</sup>SOITEC, Parc Technologique des Fontaines, Bernin, France

### Electrical Characteristic Fluctuation of 16 nm MOSFETs Induced by Random Dopants and Interface Traps \$%+

Yung-Yueh Chiu<sup>1</sup>, Fu-Hai Li<sup>1</sup>, Hui-Wen Cheng<sup>1</sup>, Yiming Li<sup>2</sup>

<sup>1</sup>Institute of Communications Engineering, National Chiao-Tung University, Hsinchu, Taiwan.

<sup>2</sup>Department of Electrical Engineering and Institute of Communications Engineering, National Chiao-Tung University, Hsinchu, Taiwan

### Invited Paper: Excellent Silicon Thickness Uniformity on Ultra-Thin SOI for controlling Vt variation of FDSOI \$&%

W. Schwarzenbach, X. Cauchy, F. Boedt, O. Bonnin, E. Butaud, C. Girard, B.-Y. Nguyen, C. Mazure, C. Maleville

SOITEC, Parc Technologique des Fontaines – Bernin – Crolles – France

### Variability Analysis of UTB SOI Subthreshold SRAM Considering Line-Edge Roughness, Work Function Variation and Temperature Sensitivity \$&(

Vita Pi-Ho Hu, Ming-Long Fan, Pin Su, Ching-Te Chuang

Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

### Invited Paper: 3D Integrable Nanowire FET Sensor with Intrinsic Sensitivity Boost \$&

Chi On Chui, Jorge Kina, Kyeong-Sik Shin

Department of Electrical Engineering, University of California, Los Angeles, CA, USA

### On The Magnitude of Random Telegraph Noise in Ultra-Scaled MOSFETs '\$' &

K.P. Cheung, J.P. Campbell

Semiconductor Electronics Division, NIST, Gaithersburg, MD, USA

## Session C: DFM/DFT/DFR/DFY

### [Invited Paper: Timing Error Prevention using Elastic Clocking](#) '\$' \*

*Kwanyeob Chae, Chang-Ho Lee, Saibal Mukhopadhyay*  
Georgia Institute of Technology, Atlanta, GA, USA

### [Time and Workload Dependent Device Variability in Circuit Simulations](#) '\$(\$

*D. Rodopoulos, S. Mahato, V. Valduga de Almeida Camargo, B. Kaczer, F. Catthoor, S. Cosemans, G. Groeseneken, A. Papanicolaou, D. Soudris*  
IMEC, Leuven, Belgium

### [Invited Paper: An On-Chip Waveform Capturer for Diagnosing Off-Chip Power Delivery](#) '\$()

*Kumpei Yoshikawa<sup>1</sup>, Takushi Hashida<sup>1</sup>, Makoto Nagata<sup>1,2</sup>*

<sup>1</sup>Graduate School of System Informatics, Kobe University, Nada-ku, Kobe, Japan

<sup>2</sup>CREST, JST, Japan

### [Interconnect Test for Core-based Designs with Known Circuit Characteristics and Test Patterns](#) '\$(-

*Tung-Hua Yeh<sup>1</sup>, Sying-Jyan Wang<sup>1</sup>, Katherine Shu-Min Li<sup>2</sup>*

<sup>1</sup>Department of Computer Science and Engineering, National Chung-Hsing University Taichung, Taiwan

<sup>2</sup>Department of Computer Science and Engineering, National Sun-Yat Sen University Kaohsiung, Taiwan

### [Invited Paper: Architectural-Level Error-Tolerant Techniques for Low Supply Voltage Cache Operation](#) '\$)'

*Shih-Lien Lu, Alaa Alameldeen, Keith Bowman, Zeshan Chishti, Chris Wilkerson, Wei Wu*  
Intel Labs, Hillsboro Oregon, USA

## Session D: 3D Integration

### [Invited Paper: Special Considerations for 3DIC Circuit Design and Modeling](#) '\$),

*Sally Liu, Yung-Chow Peng, Fu-Lung Hsueh*

Taiwan Semiconductor Manufacturing Company, Hsinchu Science Park, Hsinchu, Taiwan, ROC

### [A Single TSV-rail 3D Quasi Delay Insensitive Asynchronous Signaling](#) '\$\* %

*M. Belleville, E. Beigne, A. Valentian*

CEA, LETI, MINATEC Campus, Grenoble, France

### [Invited Paper: Smart Stacking™ Technology: an Industrial Solution for 3D Layer Stacking](#) '\$\*)

*C. Lagahe Blanchard<sup>1</sup>, I. Radu<sup>1</sup>, M. Sadaka<sup>2</sup>, K. Landry<sup>1</sup>*

<sup>1</sup>SOITEC, Parc Technologique des Fontaines, Bernin, Crolles Cedex, France

<sup>2</sup>SOITEC USA Inc., Austin, Texas, USA

### [TSV Number Minimization Using Alternative Paths](#) '\$\*,

*Chun-Hua Cheng, Chih-Hsien Kuo, Shih-Hsu Huang*

Department of Electronic Engineering, Chung Yuan Christian University, Chung Li, Taiwan, R.O.C.

### [Invited Paper: Through Silicon Via Technology using Tungsten Metallization](#) '\$+&

*G. Parès<sup>1</sup>, N. Bresson<sup>2</sup>, S. Minoret<sup>1</sup>, V. Lapras<sup>1</sup>, P. Brianceau<sup>1</sup>, J.F. Lugand<sup>1</sup>, R. Anciant<sup>1</sup>, N. Sillon<sup>1</sup>*

<sup>1</sup>CEA/LETI – Minatec, France

<sup>2</sup>SOITEC France

## Session E: CAD

### [Statistical Delay Calculation with Multiple Input Simultaneous Switching](#) '\$++

*Qin Tang, Amir Zjajo, Michel Berkelaar and Nick van der Meijs*

Circuits and Systems Group, Delft University of Technology, The Netherlands

**Balanced Truncation of a Stable Non-Minimal Deep-Submicron CMOS Interconnect** \$, %

*Amir Zjajo, Qin Tang, Michel Berkelaar, Nick van der Meijs*

Circuits and Systems Group, Delft University of Technology, The Netherlands

**Enabling TLM-2.0 Interface on QEMU and SystemC-based Virtual Platform** \$, )

*Tse-Chen Yeh, Zin-Yuan Lin, Ming-Chao Chiang*

Department of Computer Science and Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan

**A Fast Custom Network Topology Generation with Floorplanning for NoC-based Systems** \$, -

*Katherine Shu-Min Li, Shu-Yu Chen, Liang-Bi Chen, Rwei-Ting Gu*

Department of Computer Science and Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

## Session F: Advanced Memory Device

**Invited Paper: Evolution of Embedded Flash Memory Technology for MCU** \$- '

*Hideto Hidaka*

Renesas Electronics Corp. Itami, Hyogo, Japan

**Impacts of Intrinsic Device Variations on the Stability of FinFET Subthreshold SRAMs** \$- +

*Yin-Nien Chen, Chien-Yu Hsieh, Ming-Long Fan, Vita Pi-Ho Hu, Pin Su and Ching-Te Chuang*

Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan

**Invited Paper: Low-Cost Embedded Flash Memory Technology** %\$%

*Wein-Town Sun<sup>1</sup>, Cheng-Jye Liu<sup>1</sup>, Chun-Yuan Lo<sup>1</sup>, Yun-Jen Ting<sup>1</sup>, Ying-Je Chen<sup>1</sup>, Tai-Yi Wu<sup>1</sup>, Eng-Huat Toh<sup>2</sup>, Xiao-Hong Yuan<sup>2</sup>, Ko-Li Low<sup>2</sup>, Qiu Han<sup>2</sup>, Young-Seon You<sup>2</sup>, Ying-Keung Leung<sup>2</sup>, Swee-Tuck Woo<sup>2</sup>*

<sup>1</sup>eMemory Technology Inc., Hsinchu County, Taiwan

<sup>2</sup>GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore

## Session G: Reliability/Plasma Induced Damage

**Invited Paper: Crystallization Technique of Epitaxial HfO<sub>2</sub> Thin Films on Si Substrates and their Potential for Advanced High-k Gate Stack Technology** %\$\*

*Shinji Migita, Hiroyuki Ota*

Nanodevice Innovation Research Center, National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, Japan

**A New Prediction Model for Effects of Plasma-Induced Damage on Parameter Variations in Advanced LSIs** %/\$

*Koji Eriguchi, Yoshinori Takao, Kouichi Ono*

Kyoto University, Yoshida-Honmachi, Sakyo-ku, Kyoto, Japan

**Invited Paper: Impact of La on the Bias-Temperature Instability of the HfSiO High-k N-MOSFET** %/\$

*D. S. Ang<sup>1</sup>, G. A. Du<sup>2</sup>*

<sup>1</sup>School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore

<sup>2</sup>GLOBALFOUNDRIES Singapore Pte. Ltd., Singapore

**Separation of NBTI Component from Channel Hot Carrier Degradation in pMOSFETs Focusing on Recovery Phenomenon** %/\$

*Y. Mitani<sup>1</sup>, S. Fukatsu<sup>2</sup>, D. Hagishima<sup>3</sup>, K. Matsuzawa<sup>1</sup>*

<sup>1</sup>Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba Corporation, Yokohama, Japan

<sup>2</sup>Device Process Development Center, Toshiba Corporation, Japan

<sup>3</sup>Toshiba Semiconductor Company, Japan

## Session H: High Power/High Voltage

### [On the Impact of the Edge Profile of Interconnects on the Occurrence of Passivation Cracks of Plastic-Encapsulated Electronic Power Devices](#)

Jan Ackaert<sup>1</sup>, Daniel Vanderstraeten<sup>1</sup>, Bart Vandeveld<sup>2</sup>

<sup>1</sup>Corporate R&D, ON Semiconductors, Oudenaarde, Belgium

<sup>2</sup>Imec, Leuven, Belgium

### [Domestic Indirect Feedback Compensation of Multiple-Stage Amplifiers for Multiple-Voltage Level-Converting Amplification](#)

Shang-Hsien Yang, Chua-Chin Wang

Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

## Session I: Low Power

### [Microwatt Low-noise Variable-Gain Amplifier](#)

Chun-Yi Li, Yu-Bin Lin, Robert Rieger

Electrical Engineering Department, National Sun Yat-Sen University, Kaohsiung, Taiwan

### [Invited Paper: SRAM Bitcell Design for Low Voltage Operation in Deep Submicron Technologies](#)

Young Hwi Yang<sup>1</sup>, Jisu Kim<sup>1</sup>, Hyunkook Park<sup>1</sup>, Joseph Wang<sup>2</sup>, Geoffrey Yeap<sup>2</sup>, Seong-Ook Jung<sup>1</sup>

<sup>1</sup>School of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea

<sup>2</sup>Qualcomm Inc., San Diego, CA, USA.

### [An Ultra-Low Power K-Band Low-Noise Amplifier Co-Designed With ESD Protection in 40-nm CMOS](#)

Ming-Hsien Tsai<sup>1,2</sup>, Shawn S. H. Hsu<sup>1</sup>, Fu-Lung Hsueh<sup>2</sup>, Chewn-Pu Jou<sup>2</sup>, Tzu-Jin Yeh<sup>2</sup>, Ming-Hsiang Song<sup>2</sup>, Jen-Chou Tseng<sup>2</sup>

<sup>1</sup>Dept. of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan

<sup>2</sup>Design Technology Division, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

### [Invited Paper: Low Power Embedded Memory Design – Process to System Level Considerations](#)

Esin Terzioglu, Sei Seung Yoon, ChangHo Jung, Ritu Chaba, Venu Boynapalli, Mohamed Abu-Rahma, Joseph Wang, Sam Yang, Giri Nallapati, Aaron Thean, Chidi Chidambaram, Michael Han, Geoffrey Yeap, Mehdi Sani

Qualcomm Inc., San Diego, CA, USA

### [65nm PD-SOI Glitch-Free Retention Flip-Flop for MTCMOS Power Switch applications](#)

J. Le-Coz<sup>1</sup>, P. Flatresse<sup>1</sup>, S. Clerc<sup>1</sup>, M. Belleville<sup>2</sup>, A. Valentian<sup>2</sup>

<sup>1</sup>STMicroelectronics, Crolles, France

<sup>2</sup>CEA LETI, MINATEC campus, Grenoble, France

## Session J: RF & Analog, Mixed signal

### [An Ultra-Low Energy Capacitive DAC Array switching Scheme for SAR ADC in Biomedical Applications](#)

Chao Yuan, Yvonne Y. H. Lam

School of Electrical and Electronics Engineering, VIRTUS, IC Design Centre of Excellence, Nanyang Technological University, Singapore

### [Slew-Rate Controlled Output Stages for Switching DC-DC Converters](#)

Jia-Ming Liu, Yi-Cheng Huang, Yu-Chun Ying, Tai-Haur Kuo

Department of Electrical Engineering, National Cheng Kung University, Tainan City, Taiwan

### Temperature Dependence of Device Mismatch and Harmonic Distortion in Nanoscale Uniaxial-Strained PMOSFETs

Jack J.-Y. Kuo, William P.-N. Chen, Pin Su

Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

### A 8-bit 50-Msamples/s Switched-Current Pipelined ADC with Residue Generator and Interlaced Stage

Guo-Ming Sung, Ying-Tzu Lai

Department of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan

### Continuously Auto-Tuned and Self-Ranged Dual-Path PLL Design with Hybrid AFC

Min Wang, Bo Zhou, Woogeun Rhee, Zhihua Wang

Institute of Microelectronics, Tsinghua University, Beijing, China

## Session K: SoC/MPSoC/SIP

### An Integrated HDTV Predictive Pixel Compensator for H.264/AVC Decoder

Ting-Chi Tong, Yun-Nan Chang

Department of Computer Science and Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan

### Invited Paper: IBM zEnterprise™ Energy Efficient 5.2Ghz Processor Chip

H. Wen<sup>1</sup>, J. Warnock<sup>2</sup>, Y. Chan<sup>3</sup>, G. Mayer<sup>4</sup>, B. Truong<sup>1</sup>, T. Strach<sup>4</sup>, T. Slegel<sup>3</sup>, S. Carey<sup>3</sup>, G. Salem<sup>3</sup>, F. Malgioglio<sup>3</sup>, D. Malone<sup>3</sup>, D. Plass<sup>3</sup>, B. Curran<sup>3</sup>, Y.-H. Chan<sup>3</sup>, M. Mayo<sup>3</sup>, W. Huott<sup>3</sup>, P. Mak<sup>3</sup>

<sup>1</sup>IBM Systems and Technology Group, Austin, TX, USA

<sup>2</sup>IBM Systems and Technology Group, Yorktown Heights, NY, USA

<sup>3</sup>IBM Systems and Technology Group, Poughkeepsie, NY, USA

<sup>4</sup>IBM Systems and Technology Group, Boeblingen, Germany

### Ultra-Low Power FIR Filter using STSC-CVL Logic

Sajib Roy, Md. Murad Kabir Nipun, J Jacob Wikner

Division of Electronic Systems, Linkoping University, Sweden

### Design of a Low-Cost Floating-Point Programmable Vertex Processor for Mobile Graphics Applications Based on Hybrid Number System

Shen-Fu Hsiao, Chan-Feng Chiu, Chia-Sheng Wen

Department of Computer Science and Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

## Session L: I/O Circuits and ESD Protection

### A Low Jitter Active Body-Biasing Control-based Output Buffer in 65nm PD-SOI

Dimitri Soussan<sup>1,2</sup>, Sylvain Majcherczak<sup>1</sup>, Alexandre Valentian<sup>2</sup>, Marc Belleville<sup>2</sup>

<sup>1</sup>STMicroelectronics Crolles, Crolles, France

<sup>2</sup>CEA LETI, Minatec campus, Grenoble, France

### Adaptable Stimulus Driver for Epileptic Seizure Suppression

Ming-Dou Ker<sup>1,2</sup>, Wei-Ling Chen<sup>1</sup>, Chun-Yu Lin<sup>1</sup>

<sup>1</sup>Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

<sup>2</sup>Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan

### Gate-Driven 3.3V ESD Clamp Using 1.8V Transistors

Guang-Cheng Wang, Chia-Hui Chen, Wen-Hsin Huang, Kuo-Ji Chen, Ming-Hsiang Song, Ta-Pen Guo

Taiwan Semiconductor Manufacturing Corp., Hsinchu, Taiwan

### Beta-Matrix ESD Network: throughout End of Placement Rules?

J. Bourgeat, P. Galy, B. Jacquier

STMicroelectronics, Crolles, France

**Invited Paper: Design of on-chip Transient Voltage Suppressor in a Silicon-based Transceiver IC to meet IEC System-Level ESD Specification** `&\$`

Ryan Hsin-Chin Jiang, Tang-Kuei Tseng, Chi-Hao Chen, Che-Hao Chuang  
Amazing Microelectronic Corp., HsinChiu, Taiwan R.O.C.

## Session M: Soft Error Rate

**Invited Paper: Soft Error Modeling, Simulation, and Testing at Advanced Technology Nodes** `&\$+`

B. L. Bhuvu, W. T. Holman, L. W. Massengill  
Vanderbilt University, Nashville, TN, USA

**Layout Optimization to Maximize Tolerance in SEILA: Soft Error Immune Latch** `&/\$`

Taiki Uemura, Tsunehisa Sakoda, Hideya Matsuyama  
Fujitsu Semiconductor Ltd., Boulder, Akiruno, Tokyo, Japan

**Comparative Analysis of Flip-Flop designs for Soft Errors at Advanced Technology Nodes** `&/%`

B. L. Bhuvu<sup>1</sup>, K. Lilja<sup>2</sup>, J. Holts<sup>3</sup>, S.-J. Wen<sup>3</sup>, R. Wong<sup>3</sup>, S. Jagannathan<sup>1</sup>, T. D. Loveless<sup>1</sup>, M. McCurdy<sup>1</sup>, Z. J. Diggins<sup>1</sup>

<sup>1</sup>Vanderbilt University, Nashville, TN, USA

<sup>2</sup>Robust Chip, Inc., Pleasanton, CA, USA

<sup>3</sup>Cisco Systems, Inc. San Jose, CA, USA.

## Session N: Emerging Technologies

**Invited Paper: Silicon Quantum Well Light-Emitting Diode** `&/%`

S. Saito

Institute for Photonics-Electronics Convergence System Technology (PECST), Photonics Electronics Technology Research Association (PETRA), and Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, Japan

**A Frequency-Shift Readout System for FPW Allergy Biosensor** `&&&`

Chia-Hao Hsu, Yain-Reu Lin, Yue-Da Tsai, Yun-Chi Chen, Chua-Chin Wang, Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan

**Invited Paper: Scaled Nanoelectromechanical (NEM) Hybrid Devices** `&&\*`

Hiroshi Mizuta<sup>1,2</sup>, Mario A. Garcia-Ramirez<sup>2</sup>, Zakaria Moktadir<sup>2</sup>, Yoshishige Tsuchiya<sup>2</sup>, Shunichiro Sawai<sup>3</sup>, Jun Ogi<sup>3</sup>, Shunri Oda<sup>3</sup>

<sup>1</sup>School of Materials Science, Japan Advanced Institute of Science and Technology (JAIST), Ishikawa, Japan

<sup>2</sup>NANO Group, Electronics and Computer Science, Faculty of Physical and Applied Sciences, University of Southampton, Highfield, Southampton, U.K.

<sup>3</sup> Quantum Nano Electronics Research, Center, Tokyo Institute of Technology, Ookayama, Meguro-ku, Tokyo, Japan

**Evaluation of DC and AC Performance of Junctionless MOSFETs in the Presence of Variability** `& \$`

Xin Qian<sup>1</sup>, Yinglin Yang<sup>1</sup>, Zhiwei Zhu<sup>1</sup>, Shi-Li Zhang<sup>1,2</sup>, Dongping Wu<sup>1</sup>

<sup>1</sup>State Key Laboratory of ASIC and System, Fudan University, Shanghai, People's Republic of China

<sup>2</sup>Solid-State Electronics, The Ångström Laboratory, Uppsala University, Uppsala, Sweden