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An Efficient Modeling of the Multi-Gigabit SSO Interference to the Pre-Driver in the Weak Power Supply System Based on the Charge Exchange Domain Partitioning Technique with Intentionally Utilizing High Power Supply Impedance 1864
Ryuichi Oikawa – Renesas Electronics Corporation

Effect of Fine Solder Ball Diameters on Intermetallic Growth of Sn-Ag-Cu Solder at Cu and Ni Pad Finish Interfaces During Thermal Aging 1870
Yong-Sung Park and Kyung-Wook Paik – KAIST; Jeong-Tak Moon, Young-Woo Lee, and Jae-Hong Lee – MK Electron Co., Ltd

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Evaluation of the Use of a Rubber Buffer Layer to Protect Embedded SIP Devices from High Mechanical Forces 1883
Amjad Alsakarneh, Liam Moore, and John Barrett – Cork Institute of Technology

Microwave Artificially Structured Periodic Media Microfluidic Sensor 1889
Nophadon Wiwatcharagoses, Kyoung Youl Park, Jose A. Hejase, Lanea Williamson, and Prem Chahal – Michigan State University

Effect of Chemical Aging on Warpage for Encapsulated Packages—Characterization and Simulation 1894
Tz-Cheng Chiu and Hong-Wei Huang – National Cheng Kung University; Yi-Shao Lai – Advanced Semiconductor Engineering, Inc.

Prospects and Limits in Wafer-Level-Packaging of Image Sensors 1901
Martin Wilke, Kai Zoschke, Michael Toepper, Oswin Ehrmann, Herbert Reichl, and Klaus-Dieter Lang – Fraunhofer IZM; Frank Wippermann – Fraunhofer IOF

Evaluation of Additives and Current Mode on Copper Via Filling 1908
Myung-Won Jung and Jae-Ho Lee – Hongik University; Young-Sik Song and Tae-Hong Yim – Korea Institute of Industrial Technology

Electropolishing and Electroless Plating of Copper and Tin to Replace CMP and Lithographic Processes in Cu/Sn Bump Fabrication 1913
Myung-Won Jung and Jae-Ho Lee – Hongik University; Seoung-Hun Kim and Yun-Sung Moon – LS-Nikko Company; Suk-Ei Lee and Yeong-Kwon Ko – Samsung Electronics Company

Effects of Bonding Parameters and ACF Material Properties on the ACF Joint Morphology in Ultrasonic Bonding 1917
Yoo-Sun Kim – Institute of Microelectronics, A*STAR; Kiwon Lee, Won-Chul Kim, and Kyung-Wook Paik – KAIST

Miniature Detachable Photonic Turn Connector for Optical Module Interface 1922
Darrell Childers, Eric Childers, Joe Graham, Mike Hughes, Dirk Schoellner, and Alan Ugolini – US Conec, Ltd.

Conformal Atomic Layer Deposition (ALD) of Alumina on High Surface-Area Porous Copper Electrodes to Achieve Ultra-High Capacitance Density on Silicon Interposers 1928
Kanika Sethi, Himani Sharma, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology

Electromigration Prediction and Test for 0.18µm Power Technology in Wafer Level Reliability 1933
Jifa Hao, Yong Liu, and Mark Rioux – Fairchild Semiconductor Corporation; Yuanxiang Zhang and Lihua Liang – Zhejiang University of Technology

Novel Chip Stacking Process for 3D Integration 1939
Jaesik Lee, Daniel M. Fernandez, Myo Paing, Yen Chen Yeo, and Shan Gao – Institute of Microelectronics, A*STAR

Identification of Failure Modes in Portable Electronics Subjected to Mechanical-Shock Using Supervised Learning of Damage Progression 1944
Pradeep Lall and Prashant Gupta – Auburn University; Kai Goebel – NASA Ames Research Center

Thermal Modeling for Silicon-On-Sapphire (SOS) Based Power Amplifier Design in Wireless Communication 1958
John Zhiyuan Yang and Shing Lee – Peregrine Semiconductor

Compact 3D Integrable SU8 Embedded Microwave Bandpass Filters Using Complementary Split Ring Resonator Loaded Half Mode Substrate Integrated Waveguide 1963
D.E. Senior, X. Cheng, P. Jao, C. Kim, and Y.K. Yoon – University of Florida

Compact Electromagnetic-Bandgap Structures for Embedding into Si and Glass Interposers 1970
Koichi Takemura, Noriaki Ando, Hiroshi Toyao, Takashi Manako, and Tsuneo Tsukagoshi – NEC Corporation

Delamination Toughness of Cu-EMC Interfaces at Harsh Environment 1976
M. Sadeghinia, K.M.B Jansen, and L.J. Ernst – Delft University of Technology; G. Schlottig and H. Pape – Infineon Technologies AG

Study on TSV with New Filling Method and Alloy for Advanced 3D-SiP 1981
Akihiro Tsukada, Ryohei Sato, Yukihiro Sato, Yoshiharu Iwata, and Hidenori Murata – Osaka University; Shigenobu Sekine, Ryuji Kimura, and Keijiroh Kishi – Napura Co., Ltd.

Solution-Derived Electrodes and Dielectrics for Low-Cost and High-Capacitance Trench and Through-Silicon-Via (TSV) Capacitors 1987
Yushu Wang, Shu Xiang, P. Markondeya Raj, Himani Sharma, and Rao Tummala – Georgia Institute of Technology; Byron Williams – Texas Instruments

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Chairs: Nam Pham – IBM Corporation; and Mark Eblen – Kyocera America, Inc.

Electrical, Optical, and Fluidic Through-Silicon Vias for Silicon Interposer Applications 1992
Mahavir S. Parekh, Paragkumar A. Thadesar, and Muhannad S. Bakir – Georgia Institute of Technology

Mechanical Characterization of Nickel Nanowires by Using a Customized Atomic Microscope in Scanning Electron Microscope 1999
Emrah Celik, Ibrahim Guven, and Erdogan Madenci – University of Arizona

Variation-Tolerant and Low-Power Clock Network Design for 3D ICs 2007
Xin Zhao, Saibal Mukhopadhyay, and Sung Kyu Lim – Georgia Institute of Technology

Reliability of Fine Pitch Halogen-Free Organic Substrates for Green Electronics 2015
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High Throughput and Fine Pitch Cu-Cu Interconnection Technology for Multichip Chip-Last Embedding 2021
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