

2011 IEEE International Interconnect Technology Conference and 2011 Materials for Advanced Metallization

(IITC/MAM 2011)

**Dresden, Germany
8-12 May 2011**



**IEEE Catalog Number: CFP11ITR-PRT
ISBN: 978-1-4577-0503-8**

Table of Contents

Session 2: CHIP-PACKAGE-INTERACTION (CPI)

- 2.1 **INVITED- Aspects of Chip/Package Interaction and 3-D Integration Assessed by the Investigation of Crack and Damage Phenomena in low-k BEoL Stacks**
J. Auersperg, S. Rzepka and B. Michel, *Fraunhofer ENAS, Micro Materials Center, Chemnitz, Germany* *****3
- 2.2 **Shear Microprobing of Chip-Package Interaction in Advanced Interconnect Structures**
Alexander Hsing, Andrew Kearney*, Li Li*, Jie Xue*, Mark Brillhart*, and Reinhold Dauskardt, *Stanford University, Stanford, CA and *Cisco Systems, San Jose, CA* *****6

Session 3: NOVEL SYSTEMS

- 3.1 **INVITED- Silicon Photonics Integration with Electronic Circuit**
J.M. Fedeli, *CEA-LETI, Grenoble, France* *****9
- 3.2 **Benchmarking On-chip Optical Against Electrical Interconnect for High-Performance Applications**
Michele Stucchi, Stefan Cosemans, Joris Van Campenhout, Zsolt Tokei and Gerald Beyer, *IMEC, Leuven, Belgium* *****32

POSTER SESSION I

- P1.1 **Cu Electromigration Improvement by Adhesion Promotion Treatment**
Jengyi Yu, Hui-Jung Wu, Roey Shaviv, Tom Mountsier, Bart van Schravendijk, Girish Dixit, Gengwei Jiang, Pramod Subramonium, Mandy Sriram and Andy Antonelli, *Novellus Systems, San Jose, CA* *****35
- P1.2 **Process Integration of iALD TaN for Advanced Cu Interconnects**
Hui-Jung Wu, Sanjay Gopinath, Kenneth Jow, Emery Kuo, Victor Lu, Kie-Jin Park, Roey Shaviv, Tom Mountsier and Girish Dixit, *Novellus Systems, San Jose, CA* *****38
- P1.3 **Wet Process Optimization to Deposit Conformal Cu Diffusion Barrier into TSV**
Carole Pernel, Xavier Avale*, Marc Veillerot, Louis Hortemel, Patrick Leduc and Tom Ritzdorf**, *CEA-LETI-MINATEC, Grenoble, France, *SEMITOOL France, Grenoble,* *****3;

France and **Applied Materials, Kalispell, MT

- P1.4 **Electrical Property Improvements of Ultra Low-k ILD using a Silylation Process feasible for Process Integration**
Oszinda Thomas, Matthias Schaller*, Lukas Gerlich, Daniel Fischer*, Susanne Leppack*, Christin Bartsch* and Stefan E. Schulz**, *Fraunhofer Center Nanoelektronische Technologien, Dresden, Germany, *GLOBALFOUNDRIES Dresden Module Two GmbH & Co. KG, Dresden, Germany and **Fraunhofer Institute for Electronic Nano Systems, Dresden, Germany*44
- P1.5 **Reliability Performance of Advanced Metallization Options for 30nm ½ pitch in SiCOH Low-k Materials**
Kristof Croes, Steven Demuynck, Yong Kong Siew, Christopher J. Wilson, Nancy Heylen, Gerald P. Beyer and Zsolt Tokei, *IMEC, Leuven, Belgium*47
- P1.6 **Texture Change of NiSi Film with Dopant Implantation**
Hiroshi Kimura and Ryuji Tomita, *Renesas Electronics Corporation, Kanagawa, Japan*4:
- P1.7 **Behavior of the Alloying Element in Cu Interconnects**
Ryohei Kitao, Kaori Noda, Emiko Nakazawa, Yasuaki Tsuchiya and Kunihiro Fujii, *Renesas Electronics Corporation, Kanagawa, Japan*53
- P1.8 **Control of Plasma Polymerization Reaction for the 2nd generation Molecular_pore_stack (MPS) SiOCH Film with High Deposition Rate**
Hironori Yamamoto, Jun Kawahara, Naoya Inoue, Makoto Ueki, Koichi Ohto, Tatsuya Usami and Yoshihiro Hayashi, *Renesas Electronics Corporation, Kanagawa, Japan*56
- P1.9 **Relevance of Electromigration Wafer Level Test for Advanced CMOS Interconnects Reliability Control**
Franck Bana, Emmanuel Petitprez, David Ney, Lucile Arnaud* and Yves Wouters**, *STMicroelectronics, Crolles, France, *CEA LETI, Grenoble, France and **SIMaP, St-Martin-d'Hères, France*59
- P1.10 **Fundamental Study of Atomic Layer Deposition in and on Porous Low-k Films**
Patrick Verdonck, Annelies Delabie, Johan Swerts, Leo Farrell, Mikhail Baklanov, Hilde Tielens, Els Van Besien, Johan Witters, Laura Nyns and Sven Van Elshocht, *IMEC, Leuven, Belgium*62
- P1.11 **CPI Assessment Using a Novel Characterization Technique Based on Bump-Assisted Scratch-Indentation Testing**
Holm Geisler, Matthias U. Lehr, Alexander Platz, Frank Kuechenmeister, Ulrich Mayer, Thomas Roessler, Jens Paul, Lothar Lehmann, Petra Hofmann and Hans-Juergen Engelmann, *GLOBALFOUNDRIES Dresden Module One LLC & Co. KG*65

University

- P1.13 **In-situ Study and Modeling of the Decreasing Reaction Rate at the End of CoSi₂ Formation**
Roger Delattre, Roberto Simola, Christian Rivero, Valérie Serradeil, Carine Perrin-Pellegrino* and Olivier Thomas*, *STMicroelectronics, Rousset, France and *IM2NP, CNRS and Aix-Marseille University, Marseille, France* *****68
- P1.14 **Characterization of Thermal Stability of Ni(SiGe)/n-SiGe Contact formed by Isothermal Annealing**
Yao-Juan Xu, Xiao Guo, Guo-Ping Ru, Yu-Long Jiang, Xin-Ping Qu and Bing-Zong Li, *Fudan University, Shanghai, China* *****6;
- P1.15 **Photo-imageable Spin-on Dielectrics for TSV 3D Packaging Applications**
Ruzhi Zhang, Chien-Hsien Lee, Elizabeth Wolfer and Tatsuro Nagahara, *AZ Electronic Materials, Somerville, NJ* *****74
- P1.16 **Investigation of Electrical Programmable Metal Fuse in 28nm and beyond CMOS Technology**
Kuei-Sheng Wu, Ching-Hsiang Tseng, Chang-Chien Wong, Sinclair Chi, Titan Su, Yensong Liu, Huan-Sheng Wei, Wai Yi Lien and Chuck Chen, *United Microelectronics Corp. (UMC), Tainan, Taiwan, ROC* *****77
- P1.17 **Low Damage Etch Approach for Next Generation Cu Interconnect**
Sunil. K. Singh , C. J. Lee , C. H. Tsai, T. M. Huang, C. W. Lu, T. J. Tsai, Y. S. Chang, T.I. Bao,S. L. Shue & C.H. Yu, *Taiwan Semiconductor Manufacturing Co., Ltd., Tainan, Taiwan, ROC* *****7:
- P1.18 **Multilevel Interconnect Networks for the End of the Roadmap: Conventional Cu/low-k and Emerging Carbon Based Interconnects**
Ahmet Ceyhan and Azad Naeemi, *Georgia Institute of Technology, Atlanta, GA* *****83
- P1.19 **Surface Modification of Porous Low-k Material by Plasma Treatment and its Application on Reducing the Damage from Sputtering and CMP Process**
Hai-Sheng Lu, Knut Gottfried, Nicole Ahner, Stefan Schulz and Xin-Ping Qu, *Fudan University, Shanghai, China and *TU Chemnitz/ZfM and Fraunhofer ENAS, Chemnitz, Germany* *****86
- P1.20 **Robust Porous SiOCH (k=2.5) for 28nm and beyond Technology Node**
Janghee Lee, Sang Hoon Ahn, Insun Jung*, Kyu-Hee Han, Gyeonghee Kim, Sang-Don Nam, Woo Sung Jeon*, Byeong Hee Kim, Gil Heyun Choi, Siyoung Choi, Ho-Kyu Kang and Chilhee Chung, *Samsung Electronics Co. Ltd., Hwasung City, Korea and *Samsung Advanced Institute of Technology, Yongin City, Korea* *****89
- P1.21 **Comparison of Electrical Performances of Metal-Insulator-Metal Capacitors with Sputtered HfO₂ and BZT-HfO₂ Dielectrics**
Li-Feng Zhang, Hui Xu, Qiu-Xiang Zhang, Shi-Jin Ding and David Wei Zhang, *Fudan University, Shanghai, China* *****92

Temporal Instability of Suppressor Ensembles under Reactive Conditions

Alexander Fluegel, Marco Arnold, Anja Wagner, Dieter Mayer, MNT Hai*, HTM Trung*, J Odermatt* and Peter Broekmann, *BASF SE, Ludwigshafen, Germany and *University of Bern, Bern, Switzerland* *****95

P1.23 **Grain Boundary as Relevant Microstructure Feature for Electromigration in Advanced Technology Studied by Electron BackScattered Diffraction**

Romain Galand, Lucile Arnaud*, Emmanuel Petitprez, Guillaume Brunetti*, Laurent Clément, Patrice Waltz and Yves Wouters**, *STMicroelectronics, Crolles, France, *CEA LETI, Grenoble, France and **SIMap, ST Martin D'Herès, France* *****98

P1.24 **Investigation of Ultra-thin Al₂O₃ Film as Cu Diffusion Barrier on Low-k (k=2.5) Dielectrics**

Shao-Feng Ding, Qi Xie*, Fei Chen, Hai-Sheng Lu, Shao-Ren Deng*, Christophe Detavernier*, Guo-Ping Ru, Yu-Long Jiang and Xin-Ping Qu, *Fudan University, Shanghai, China and *Ghent University, Ghent, Belgium* *****9;

P1.25 **Ultrathin TaN/Ta Barrier Modifications to Fullfill Next Technology Node Requirements**

Lukas Gerlich, Susanne Ohsiek*, Christoph Klein*, Mario Geiß*, Michael Freidemann*, Peter Kücher and Dieter Schmeisser**, *Fraunhofer CNT, Dresden, Germany, *GLOBALFOUNDRIES Dresden Module One, Dresden, Germany and **BTU Cottbus, Cottbus, Germany* *****:4

P1.26 **Si Ohmic Contacts on N-type SiC**

Stanislav Cichoň, Petr Macháček, Bohumil Barda and Marie Kudrnová, *Institute of Chemical Technology, Prague, Czech Republic* *****!7

P1.27 **Impact of Through-Silicon-Via Scaling on the Wirelength Distribution of Current and Future 3D ICs**

Dae Hyun Kim and Sung Kyu Lim, *Georgia Institute of Technology, Atlanta, Georgia* *****::

P1.28 **A Study of TSV Variation Impact on Power Supply Noise**

Moongon Jung, Shreepad Panth and Sung Kyu Lim, *Georgia Institute of Technology, Atlanta, Georgia* *****!3

P1.29 **Impact of TSV Proximity on 45nm CMOS Devices in Wafer Level**

Sungdong Cho, Sinwoo Kang, Kangwook Park, Jaechul Kim, Kiyong Yun, Kisoong Bae, Woon Seob Lee, Sangwook Ji, Eunji Kim, Jangho Kim, Yeong L. Park and ES Jung, *Samsung Co., Ltd., Yongin City, Korea* *****!6

P1.31 **Helium Ion Microscope Characterization for Cu / Low-k Interconnects - SE Imaging and Focused Helium Ion Beam Luminescence Detection**

Shinichi Ogawa, Tomohiko Iijima, Shogo Awata*, Shigeru Kakimuna*, Shintaro Komatani* and Toshihiko Kanayama, *National Institute of Advanced Industrial Science and Technology (AIST), Ibaraki, Japan* and **HORIBA, Ltd., Kyoto, Japan* *****;9

Session 4: MATERIALS AND PROCESSES I

- 4.1 **INVITED- Future of PECVD and Spin-on ultra low-k Materials**
W. Volksen, T. Frot, T. Magbitang, S. Gates*, Mark Oliver**, R. Dauskardt**, and G. Dubois, *1IBM Almaden Research Center, San Jose, CA, *IBM T. J. Watson Research Center, Yorktown Heights, NY, and **Stanford University, Stanford, CA* *****322
- 4.2 **Highly Reliable Enhanced Nitride Interface (ENI) Process of Barrier Low-k using Absorption-Free Ultra-Thin SiN (UT-SiN)**
Tatsuya Usami, Yukio Miura, Tomoyuki Nakamura, Hideaki Tsuchiya, Chikako Kobayashi, Koichi Ohto, Shoichi Hiroshima, Mikio Tanaka, Hiroyuki Kunishima, Issei Ishizuka, Teruhiro Kuwajima, Michio Sakurai, Shinji Yokogawa and Kunihiro Fujii, *Renesas Electronics Corporation, Yamagata, Japan* *****325
- 4.3 **CVD Co Capping Layers for Cu/Low-k Interconnects: Cu EM Enhancement vs. Co Thickness**
Chih-Chao Yang, F. Baumann*, P.-C. Wang*, SY Lee**, P. Ma**, J. AuBuchon** and D. Edelstein, *IBM Research, Albany, NY, IBM Microelectronics, East Fishkill, NY and **Applied Materials, Inc., Santa Clara, CA* *****328

Session 5: CHARACTERIZATION

- 5.1 **INVITED- Nanoindentation for Quality Control of ULK Films**
Kong Boon Yeap, K. Zeng*, Ude Hangen** and Ehrenfried Zschech, *Fraunhofer IZFP Dresden, Germany, *National University of Singapore, Singapore and **Hysitron, Inc., Aachen, Germany* *****32;
- 5.3 **Direct Measurement of Grain Boundary Resistance in Copper Nanowires**
An-Ping Li, Tae-Hwan Kim, X.-G. Zhang, Don Nicholson, B.M. Evans, N.S. Kulkarni, E.A. Kenik, H.M. Meyer and B. Radhakrishnan, *Oak Ridge National Lab., Oak Ridge, TN* *****334

Session 6: RELIABILITY

- 6.1 **INVITED- Comprehensive Lifetime Prediction for Intrinsic and Extrinsic TDDB Failures in Cu/Low-k Interconnects**
N. Suzumura, M. Ogasawara, K. Makabe, T. Kamoshima, T. Ouchi, S. Yamamoto, T. Furusawa and E. Murakami, *Renesas Electronics Corp., Ibaraki, Japan*337
- 6.2 **Impact of Low-k Moisture Absorption during Queue-time on Cu-alloy/Low-k Reliability and its Suppression**
Hideaki Tsuchiya, Shinji Yokogawa, Hiroyuki Kunishima, Teruhiro Kuwajima, Tatsuya Usami, Yukio Miura, Koichi Ohto, Kunihiro Fujii and Michio Sakurai, *Renesas Electronics Corp., Kanagawa, Japan*33:
- 6.3 **Effects of Metal-cap Coverage on Electro-migration (EM) Tolerance for Scaled-down Cu Interconnects**
Makoto Ueki, Emiko Nakazawa, Ryohei Kitao, Shoichi Hiroshima, Tetsuya Kurokawa, Naoya Furutake, Hironori Yamamoto, Naoya Inoue, Yasuaki Tsuchiya and Yoshihiro Hayashi, *Renesas Electronics Corp., Kanagawa, Japan*343
- 6.4 **INVITED- Backend-of-Line Reliability Improvement Options for 28nm Node Technologies and Beyond**
O. Aubel, C. Hennesthal, M. Hauschildt, A. Beyer, J. Poppe, G. Talut, M. Gall, J. Hahn, J. Boemmels, M. Nopper and R. Seidel, *GLOBALFOUNDRIES Dresden, Germany*346
- 6.5 **Line Edge Roughness (LER) Correlation and Dielectric Reliability with Spacer-Defined Double Patterning (SDDP) at 20nm Half Pitch**
Yong Kong Siew, Michele Stucchi, Janko Versluijs, Philippe Roussel, Eddy Kunnen, Marianna Pantouvaki, Gerald Beyer and Zsolt Tokei, *IMEC, Leuven, Belgium*349

Session 7: MEMORIES

- 7.1 **INVITED- Scaling Effect of Device Area and Film Thickness on Electrical and Reliability Characteristics of RRAM**
Joonmyoung Lee, Jubong Park, Seungjae Jung, and Hyunsang Hwang, *Gwangju Institute of Science and Technology, Korea*352
- 7.2 **Demonstration of Phase Change Memories Devices using Ge₂Sb₂Te₅ Films deposited by Atomic Layer Deposition**
Sylvain Maitrejean, Sandrine Lhostis*, Suvi Haukka**, Carine Jahan, Emmanuel Gourvest, Raija Matero**, Tom Blomberg**, Alain Toffoli, Alain Persico, Celine Jayet, Marc Veillerot, Jean Paul Barnes, Francois Pierre, Frederic Fillot, Luca Perniola, Veronique Sousa, Hessel Sprey**, Fabien Boulanger, Barbara De Salvo, and Thierry Billon, *CEA LETI, Grenoble, France, *STMicroelectronics, Crolles, France and **ASM Microchemistry Oy, Helsinki, Finland*355

Fully CMOS BEOL Compatible HfO₂ RRAM Cell, with Low (μ A) Program Current, Strong Retention and High Scalability, using an Optimized Plasma Enhanced Atomic Layer Deposition (PEALD) Process for TiN Electrode

Yang Yin Chen, Ludovic Goux, Luigi Pantisano, Johan Swerts, Christoph Adelman, Sofie Mertens, Valeri Afanasiev*, Xin Peng Wang, Bogdan Govoreanu, Robin Degraeve, Stefan Kubicek, Vasile Paraschiv, Beatrijs Verbrugge, Nico Jossart, Laith Altimime, Malgorzata Jurczak, Jorge Kittl, Guido Groeseneken, and Dirk Wouters, *IMEC, Leuven, Belgium and *KU Leuven, Leuven, Belgium* *****358

POSTER SESSION II

- P2.33 **Crack Propagation and Delamination Analysis within the Die by Camera-Assisted Double Cantilever Beam Technique**
Michael Hecker, Robert Hentschel, Marco Hensel and Matthias U. Lehr, *GLOBALFOUNDRIES Dresden Module One LLC & Co KG, Dresden, Germany* *****35;
- P2.34 **Copper Electrochemical Deposition in Macroporous Silicon Arrays for Through Silicon Via Applications**
Thomas Defforge, Loïc Coudron, Gaël Gautier, Virginie Grimal, Laurent Ventura and François Tran Van, *Université de Tours, Tours, France* *****364
- P2.35 **Temporary Passivation of Cu for Low Temperature (< 300°C) 3D Wafer Stacking**
Dau Fatt Lim, Jun Wei*, Kam Chew Leong** and Chuan Seng Tan, *Nanyang Technological University, Singapore, *Singapore Institute of Manufacturing Technology, Singapore and **GLOBALFOUNDRIES Singapore* *****367
- P2.36 **Cu dry-fill on CVD Ru liner for advanced gap-fill and lower resistance**
Tadahiro Ishizaka, Atsushi Gomi, Takara Kato, Takashi Sakuma, Osamu Yokoyama, Chiaki Yasumuro, Hiroyuki Toshima, Yasushi Mizusawa, Tatsuo Hatano, Cheon Soo Han and Masamichi Hara, *Tokyo Electron AT LTD, Nirasaki, Japan* *****36:
- P2.38 **Fundamental Relationship between Capacitance-Time Measurements and Gravimetric Measurements for Water Absorption in a Low-k Dielectric**
Christoph Kubasch and Johann W. Bartha, *Technische Universität Dresden, Dresden, Germany* *****373
- P2.39 **Modeling and Optimization for Multi-Layer Graphene Nanoribbon Conductors**
Vachan Kumar, Shaloo Rakheja and Azad Naeemi, *Georgia Institute of Technology* *****376
- P2.40 **Highly Reliable Molecular-Pore-Stacking (MPS)/Cu Interconnects using Novel Post-etching Treatment (PET) for 28 nm-node and Beyond**
D. Oshida, I. Kume, H. Kunishima, H. Tsuchiya, H. Katsuyama, M. Ueki, M. Iguchi, S. Yokogawa, N. Inoue, N. Oda and M. Sakurai, *Renesas Electronics Corporation,* *****379

- P2.41 **High-performance metal hard mask process using novel TiN film for 32-nm node Cu interconnect and beyond**
Naoki Torazawa, Toru Hinomura, Takeshi Harada, Tatsuya Kabe, Daisuke Inagaki, Yasunori Morinaga, Junichi Shibata, Takushi Shigetoshi, Shunsuke Hazue, Dai Motojima*, Susumu Matsumoto and Takenobu Kishida, *Panasonic Corporation, Toyama, Japan and * Panasonic Semiconductor Engineering Co., Ltd., Kyoto, Japan*382
- P2.42 **CVD and ALD of Cobalt-tungsten alloy film as a novel Copper diffusion barrier**
Hideharu Shimizu, Kaoru Sakoda and Yukihiro Shimogaki*, *Taiyo Nippon Sanso and *The University of Tokyo, Tokyo, Japan*385
- P2.43 **Thermal Stability and Interface Improvement of Thin NiSiGe by C+ ion implantation**
Bo Zhang, Wenjie Yu, Qing-Tai Zhao, Dan Buca, Bernhard Hollaender, Jean-Michel Hartmann**, Miao Zhang*, Xi Wang and Siegfried Mantl, *Forschungszentrum Juelich, Juelich, Germany, * Shanghai Institute of Microsystem and Information Technology, Shanghai, China and **CEA-LETI, Grenoble, France*388
- P2.44 **Cu Damascene Interconnects with an Organic Low-k Fluorocarbon Dielectric Deposited by Microwave Excited Plasma Enhanced CVD**
Xun Gu, Takenao Nemoto, Yugo Tomita, Akihide Shirotori, Ricardo Duyos-Mateo, Kotaro Miyatani*, Akane Saito*, Yasuo Kobayashi*, Akinobu Teramoto, Shin-Ichiro Kuroki, Toshihisa Nozawa*, Takaaki Matsuoka*, Shigetoshi Sugawa and Tadahiro Ohmi, *Tohoku University, Sendai, Japan and * Tokyo Electron Technology Development Institute, Inc., Nirasaki, Japan*38;
- P2.45 **Influence of copper on the catalytic carbon nanotube growth process**
Holger Fiedler, Sascha Hermann, Stefan E. Schulz* and Thomas Gessner*, *TU Chemnitz, Chemnitz, Germany and *Fraunhofer Research Institution for Electronic Nano Systems (ENAS)*394
- P2.46 **Effect of Oxygen Diffusion into TiN on Resistance Switching Characteristics of ZrO₂ films with Annealing Temperatures**
Jonggi Kim, Sunghoon Lee, Heedo Na, Kyumin Lee and Hyunchul Sohn, *Yonsei University, Seoul, Korea*397
- P2.47 **Impact of ambient atmosphere on plasma-damaged porous low-k characterization**
Maxime Darnon, Thierry Chevolleau, Thibaut David*, Nicolas Posseme*, Regis Bouyssou**, Romain Hurand**, Olivier Joubert, Christophe Licitra*, Nevine Rochat*, Fanny Bailly** and Christophe Verove**, *UJF-Grenoble1, Grenoble, France, *CEA-LETI-MINATEC, Grenoble, France and **STMicroelectronics, Crolles, France*39:
- P2.48 **Pad roughness effects on the planarization and material removal rate in CMP processes**
Boris Vasilev, Sascha Bott, Roland Rzehak**, Peter Kücher and Johann W. Bartha*, *Fraunhofer Center Nanoelectronic Technologies (CNT), Dresden, Germany, and*

**Dresden University of Technology (IHM), Dresden, Germany and **Helmholtz-Zentrum Dresden-Rossendorf (HZDR), Germany*3:3

P2.49 **Scatterometric Porosimetry for porous low-k patterns characterization**
Romain Hurand, Regis Bouyssou**, Maxime Darnon, Charles Tiphine, Christophe Licitra*, Mohamed El-kodadi, Thierry Chevolleau, Thibaut David, Nicolas Posseme*, Maxime Besacier, Patrick Schiavone, Fanny Bailly**, Olivier Joubert and Christophe Verove**, *UJF-Grenoble1, Grenoble, France, *CEA-LETI-MINATEC, Grenoble, France and **STMicroelectronics, Crolles, France*3:6

P2.50 **Investigation of local stress around TSVs by micro-Raman spectroscopy and finite element simulation**
François Le Texier, Jessica Mazuir, Man Su-Yin, Mohamed Saadaoui, Jean-Luc Liotard* and Karim Inal, *ENSM.SE/CMP-GC, Gardanne, France and *STMicroelectronics, Rousset, France*3:9

P2.51 **Thermal Stability of Copper Through-Silicon Via Barriers during IC Processing**
Yann Civale, Kristof Croes, Yuichi Miyamori*, Sarasvathi Thangaraju, Augusto Redolfi, Annemie Van Ammel, Dimitrios Velenis, Vladimir Cherman, Geert Van der Plas, Andrew Cockburn**, Virginie Gravey**, Nirajan Kumar***, Zhitao Cao***, Deniz S. Tezcan, Philippe Soussan, Y. Travalay, Zsolt Tókei, Eric Beyne, and Bart Swionnen, *IMEC, Leuven, Belgium, *Sony Corporation (assigned at IMEC), **Applied Materials Belgium and ***Applied Materials, Santa Clara, CA*3:2

P2.52 **Integrated NiSi defect reductions in 45nm node and beyond**
Jerander Lai, Yi-Wei Chen, Nien-Ting Ho, J. F. Lin, C.C. Huang and J.Y. Wu, *UMC, Tainan, Taiwan, ROC*3:5

P2.53 **Investigation on MOCVD CoSi₂ Process for Reduction of Contact Resistance at Metal-Silicon Interface**
Eui Seong Hwang, Bo Min Seo, Juhyun Myeong, Jun Yeol Cho, Jongmin Lee, Kwon Hong and Sungki Park, *Hynix Semiconductor, Inc., Kyoungki-do, Korea*3:8

P2.54 **Robust low-voltage program-erasable capacitors of Pd-Al₂O₃-Si with high density Ru-based nanocrystals embedded**
Hong-Yan Gou, Shi-Jin Ding, Qing-Qing Sun and David Wei Zhang, *Fudan University, Shanghai, China*3;;

P2.56 **Nanowire Filled Polymer Films for 3D System Integration**
Matthias Graf, Karsten Meier, Veronika Haehne*, Heike Schlörb*, Alexander Eychmüller and Klaus-Jürgen Wolter, *Technische Universität Dresden, Dresden, Germany, *Leibniz-Institute for Solid State and Materials Research, Dresden, Germany*424

The Simplest Modification of Cu Diffusion Barrier Dielectrics to Improve Cu/Low-k Interconnects Reliability

Kinya Goto, Yoshihiro Oka, Naohito Suzumura, Ryuji Shibata, Takahisa Furuhashi, Masahiro Matsumoto, Takeshi Kawamura, Masazumi Matsuura, Masahiko Fujisawa and Koyu Asai, *Renesas Electronics Corp., Ibaraki, Japan*427

P2.58 **Electrical Performances of Low Resistive W Buried Gate using B₂H₆-reduced W Nucleation Layer Technology for 30nm-based DRAM Devices**

Choon-Hwan Kim, Il-Cheol Rho, Byung-Soo Eun, Hyun-Phill Kim, Sung-gon Jin and Hyo-Sang Kang, *Hynix Semiconductor, Kyounggki-do, Korea*42:

P2.59 **Lifetime of Thermosonic Copper Ball bonds on Aluminum Metallization Pads**

Wolfgang Trasischker, Alice Lassnig, Golta Khatibi, Brigitte Weiss, Michael Nelhiebel* and Rainer Pelzer*, *University of Vienna, Austria and *Infineon Technologies, Austria*433

P2.60 **Modulation of Schottky Barrier Height for NiSi/Si(110) Diodes Using an Antimony Interlayer**

Xiao Guo, Yao-Juan Xu, Yu-Long Jiang, Guo-Ping Ru and Bing-Zong Li, *Fudan University, Shanghai, China*436

P2.61 **Grain structure effect on EM of Cu interconnects with CoWP capping – a statistical model**

Lijuan Zhang, Linjun Cao and Paul Ho, *University of Texas at Austin, Austin, TX*439

P2.62 **Reliability testing and Failure Analysis of 3D Integrated Systems**

Armin Klumpp, Peter Ramm, German Franz*, Chad Rue** and Laurens Kwakman*, *Fraunhofer EMFT, Munich, Germany, *FEI Electron Optics, Eindhoven, The Netherlands and **FEI Company, Hillsboro, OR*442

P2.64 **Quantum mechanical methods for the simulation of electronic transport through carbon nanotubes**

Andreas Zienert, Jörg Schuster*, Reinhard Streiter* and Thomas Gessner, *Chemnitz University of Technology, Chemnitz, Germany and *Fraunhofer Research Institution for Electronic Nano Systems, Chemnitz, Germany*445

Session 8: 3D INTEGRATION I

8.1 **INVITED- 3D Technology Roadmap and Status**

Paul Marchal, Geert Van der Plas, Geert Eneman, Victor Moroz*, Mustafa Badaroglu, Abdelkarim Mercha, Steven Thijs, Dimitri Linten, Katti Guruprasad, Michele Stucchi, Bart Vandeveld, Herman O'Prins, Vladimir Cherman, Kristof Croes, Augusto Redolfi, Antonio La Manna, Youssef Travaly, Eric Beyne, Rudi Cartuyvels, *IMEC, Leuven,*448

- 8.2 **Process and RF Modelling of TSV Last Approach for 3D RF Interposer**
Christine Fuchs, Jean Charbonnier, Séverine Cheramy, Lionel Cadix*, David Henry, Pascal Chausse, Ouafa Hajji, Alexis Farcy*, Gennie Garnier, Catherine Brunet-Manquat, Julien Diaz, Romain Anciant, Pierre Vincent, Nicolas Sillon and Pascal Ancey*, *CEA LETI, Grenoble, France and *STMicroelectronics, Crolles, France*44;
- 8.3 **Study of the Evolution of Cu-Cu Bonding Interface Imperfection Under Direct Current Stressing for Three Dimensional Integrated Circuits**
Riko I Made, Peng Lan, Hong Yu Li*, Chee Lip Gan and Chuan Seng Tan, *Nanyang Technological University, Singapore and *Institute of Microelectronics, Singapore*454

Session 9: PROCESS INTEGRATION I

- 9.1 **INVITED- Yield Improvement and Ramp Up to Production of Advanced CMOS Technologies Interconnect**
Roberto Gonella, *STMicroelectronics, Crolles, France*457
- 9.2 **Optimization of Porous Ultra Low- κ Dielectrics ($\kappa \leq 2.55$) for 28nm Generation**
Dimitri Kioussis, Todd Ryan***, Anita Madan*, Nancy Klymko*, Steven Molis*, Zhiguo Sun, Hideaki Masuda**, Shurong Liang, Tim Lee*, Darryl Restaino*, Larry Clevenger*, Roger Quon*, Rod Augur, Craig Child, Steven Gates^^, Alfred Grill^^, Hosadurga Shobha***, Brian Sundlof*, T. Shaw^^*, G. Bonilla^^*, T. Daubenspeck*, G. Osborne*, S. Cohen^^, and K. Virwani^^^, *GLOBALFOUNDRIES, Hopewell Junction, NY, *IBM, Hopewell Junction, NY, **Toshiba, Hopewell Junction, NY, ***IBM, Albany, NY, ^GLOBALFOUNDRIES at Albany Nanotech, NY, ^^T.J. Watson Research Center, Yorktown Heights, NY, ^^^Almaden Research Center, San Jose, CA*45:
- 9.3 **Robust Self-Aligned Via Process for 64nm Pitch Dual-Damascene Interconnects using Pitch Split Double Exposure Patterning Scheme**
Hideyuki Tomizawa, Shyng-Tshong Chen*, David Horak*, Hirokazu Kato, Yunpeng Yin*, Masao Ishikawa, James Kelly*, Chiew-seng Koay*, Guillaume Landie**, Sean Burns*, K. Tsumura, Masayoshi Tagami***, Hosadurga Shobha*, Muthumanickam Sankarapandian*, Oscar Van der Straten*, Joseph Maniscalco*, T. Vo*, J. Arnold*, M. Colburn*, T. Usui, and T. Spooner*, *Toshiba America Electronic Components, Inc., *IBM Corp. Albany Nanotech, **STMicroelectronics ***Renesas Electronics, Albany, NY*463

Session 10: MATERIAL AND PROCESSES II

- 10.1 **INVITED- Atomic Layer Deposition for Nanoscale Contact Applications**
Hyungjun Kim, Jaehong Yoon, and Han-Bo-Ram Lee, *Yonsei University, Seoul, Republic of Korea*466

Direct Seed Electroplating of Copper on Ruthenium Liners

Rohan Akolkar, Tejaswi Indukuri, James Clarke, Thomas Ponnuswamy*, Jonathan Reid*, Andrew McKerrow* and Sesha Varadarajan*, *Intel Corp., Hillsboro, OR and *Novellus Systems, Tualatin, OR*469"

10.3 **Investigations on Ru-Mn Films as Plateable Cu Diffusion Barriers**

Henry Wojcik, Rainer Kaltofen*, Cornelia Krien*, Ulrich Merkel, Christian Wenzel, Johann Bartha, Michael Friedemann**, Barbara Adolphi, Romy Liske***, Volker Neumann and Marion Geidel, *Semiconductor & Microsystems Technology Laboratory (IHM), TU Dresden, Germany, *Leibniz Institute For Solid State & Materials Research (IFW), ** GLOBALFOUNDRIES Module Two LLC & CoKG, *** Fraunhofer Center for Nanotechnologies (CNT), Dresden, Germany*472

10.4 **Enabling Cu-Cu Connection in (Dual) Damascene Interconnects by Selective Deposition of two Different SAM molecules**

Arantxa Maestre Caro, Youssef Travaly, Guido Maes*, Gustaaf Borghs and Silvia Armini, *IMEC. Leuven, Belgium and *KU Leuven, Leuven, Belgium*475

Session 11: POWER AND AUTOMOTIVE INTERCONNECT

11.1 **INVITED- Interconnect Technologies for SmartPower Integrated Circuits in the area of Automotive Power Applications**

M. Stecher, P. Nelle, J. Busch, P. Alpern, *Infineon Technologies AG, Neubiberg, Germany*478

11.2 **INVITED- Process Transfers Provide Opportunities for More Reliable Products**

Fred Kuper, Piet Wessels, Eric Ooms, Joost van Herk, Marcel Rijnsburger, Willem van Driel*, Jos Plagge, NXP Semiconductors, Nijmegen, The Netherlands, *now with Philips Electronics, The Netherlands47;

11.3 **INVITED- Qualification of Extrinsic in BEOL – The New Challenge**

A.H. Fischer, S. Penka, G. Antonin, M. Czekalla*, S. Wallace*), P. Oesinghaus*, and J. Kritz, *Infineon Technologies AG, Neubiberg, Germany and *Infineon Technologies GmbH, Dresden, Germany*484

Session 12: NOVEL MATERIALS AND CONCEPTS

12.1 **INVITED- Interconnect Performance and Energy-Per-Bit for Post-CMOS Logic Circuits- Modeling**

Analysis and Comparison with CMOS Logic, Shaloo Rakheja and Azad Naeemi *Georgia Institute of Technology, Atlanta, GA*487

12.2 **Mechanism of Resistivity Decrease in Networked-Nanographite Wires for Multi-layer Graphene Interconnects**

Motonobu Sato, Shuichi Ogawa*, Manabu Inukai**, Eiji Ikenaga**, Takayuki Muro**, Yuji Takakuwa*, Mizuhisa Nihei and Naoki Yokoyama, *AIST, Tsukuba, Japan*, **Tohoku University, Sendai, Japan* and ***Japan Synchrotron Radiation Research Institute (JASRI), Sayo, Japan*48:

12.4 **Integration of Dense CNTs in Vias on 200mm Diameter Wafers: Study of Post CNT Growth Processes**

Murielle Fayolle, Jean Francois Lugand, Riadh Kachtouli, Hanako Okuno, Jean Dijon*, Pauline Gautier and Thierry Billon, *CEA LETI, Grenoble, France* and *CEA LITEN, Grenoble, France*493

12.5 **Carbon Nanotube Interconnects: Electrical Characterization of 150 nm CNT Contacts with Cu Damascene Top Contact**

Nicolò Chiodarelli, Marleen H. van der Veen, Bart Vereecke, Daire Cott, Guido Groeseneken, Philippe M. Vereecken, Cedric Huyghebaert and Zsolt Tokei, *IMEC, Leuven, Belgium*496

Session 13: METAL GATE

13.1 **Evaluation of Aluminum Film Properties and Microstructure for Replacement Metal Gate Application at 28nm Technology Node**

R. P. Huang, Y. H. Hsien, T. C. Tsai, Welch Lin, H. F. Huang, C. M. Hsu, M. C. Tsai, K. H. Lin, H. K. Hsu, J. F. Lin, C. L. Yang and J. Y. Wu, *United Microelectronics Corporation, Tainan, Taiwan, ROC*499

Session 14: PROCESS INTEGRATION II

14.1 **Post Porosity Plasma Protection: A New Approach to Integrate $k \leq 2.2$ Porous ULK Materials**

Theo Frot, Willi Volksen, Teddie Magbitang, Dolores Miller, Sampath Purushothaman*, Micheal Lofaro*, Robert Bruce*, and Geraud Dubois, *IBM Almaden Research Center*,4: 2

- 14.2 **64 nm pitch Cu Dual-Damascene Interconnects using Pitch Split Double Exposure Patterning Scheme**
 Shyng-Tsong Chen, Hideyuki Tomizawa*, Kazumichi Tsumura*, Masayoshi Tagami**, Hosadurga Shobha, Muthumanickam Sankarapandian, Oscar Van der Straten, James Kelly, Donald Canaperi, Theodore Levin, Stephan Cohen^, Yunpeng Yin, Dave Horak, Masao Ishikawa*, Yann Mignot***, Chiew-seng Koay, Sean Burns, Scott Halle, Hirokazu Kato*, Guillaume Landie**, Y. Xu, A. Scaduto, E. McIellan, J.C. Arnold, M. Coburn, T. Usui* and Terry Spooner, *IBM Corp. at Albany Nano-Technology Center, *Toshiba America Electronic Components, Inc., **Renesas Electronics, ***STMicroelectronics, Albany, NY and ^IBM T.J. Watson Research Center, Yorktown Heights, NY* 4:5
- 14.3 **Improvement of RC Performance for Advanced ULK/Cu Interconnects with CVD Hybrid Dielectric/Metal Liner**
 Masayoshi Tagami, Chih-Chao Yang*, Hosadurga Shobha*, Eiichi Soda, Anita Madan**, Patrick DeHaven**, Richard Murphy**, Robert E. Davis**, Christopher Parks**, Steven Molis**, Stephan A. Cohen^, Fuminori Ito and Terry Spooner*, *Renesas Electronics, *IBM Corp., Albany, NY, ** IBM Corp., Hopewell Junction, NY, and ^IBM T.J. Watson Research Center, Yorktown Heights, NY* 4:8

Session 15: 3D INTEGRATION II

- 15.1 **INVITED- Thermal and Spatial Dependence of TSV-induced Stress in Si**
 C. McDonough, B. Backes, W. Wang, R. Caramto* and R. E. Geer, *University at Albany SUNY, Albany, NY and *SEMATECH, Albany, NY* 4:;
- 15.2 **Orthotropic Stress Field Induced by TSV and Its Impact on Device Performance**
 Cheng-Chieh Hsieh, Hung-An Teng, Shin-Puu Jeng, San-Bor Jan, Ming-Fa Chen, J.H. Chang, Cheng-Hung Chang, Ku-Feng Yang, Yung-Chi Lin, Tsang-Jiun Wu, Wen-Chih Chiou, Shang-Yun Hou and Doug C.H. Yu, *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan* 4:4
- 15.3 **ZrBO Dielectrics for TSV Production Process**
 Masanobu Hatanaka, Akihiro Shibata, Masamichi Harada, Satoru Toyoda, Michio Ishikawa and Koukou Suu, *ULVAC, Inc., Shizuoka, Japan* 4:7

Session 16: SILICIDES AND CONTACTS

- 16.1 **INVITED- Strain Measurement for the Semiconductor Industry with nm-Scale Resolution by Dark Field Electron Holography and Nanobeam Electron Diffraction**
 D. Cooper, A. B  ch  *, J.M. Hartmann, V. Carron, J-L Rouviere*, *CEA-LETI, Grenoble,* 4:;

- 16.2 **Stress-induced Voids in Ni-Pt Silicide: Disconnection of Narrow (Ni-Pt)Si between Gate Canyons on Wide Active Area**
Takuya Futase, Toshiyuki Oashi*, Hitoshi Maeda*, Yutaka Inaba* and Hisanori Tanimoto, *University of Tsukuba, Tsukuba, Japan* and **Renesas Electronics Corp., Kawasaki, Japan* 523
- 16.4 **Millisecond Annealing for Salicide Formation: Challenges of NiSi Agglomeration Free Process**
Magali Gregoire, Remi Beneyton and Pierre Morin, *STMicroelectronics, Crolles, France* 526
- 16.5 **CVD-Cobalt for Low Resistance Word Line Electrode of 3D NAND Flash Memory**
MinSoo Kim, SungJin Whang, YoungJin Lee, JooHee Han, JinHae Choi, ByoungHo Lee, DongSun Sheen, SeungHo Pyi and JinWoong Kim, *Hynix Semiconductor, Inc., Gyeonggi-do, Korea* 529
- 16.6 **NiSi Nano-contacts to Strained and Unstrained Silicon Nanowires**
Stefan Habicht, Qing-Tai Zhao, Sebastian Feste, Lars Knoll, Stefan Trellenkamp, Konstantin Bourdelle* and Siegfried Mantl, *Forschungszentrum Juelich, Juelich, Germany* and **SOITEC, Bernin, France* 532