

2011 IEEE 9th Symposium on Application Specific Processors

(SASP 2011)

**San Diego, California, USA
5 – 6 June 2011**



**IEEE Catalog Number: CFP11SPP-PRT
ISBN: 978-1-4577-1212-8**

TABLE OF CONTENTS

SESSION 1: DESIGN TOOLS AND SYNTHESIS

How Sensitive is Processor Customization to the Workload’s Input Datasets?	1
<i>M. Breughe, Z. Li, Y. Chen, S. Eyerman, O. Temam, C. Wu, L. Eeckhout</i>	
TARCAD: A Template Architecture for Reconfigurable Accelerator Designs	8
<i>M. Shafiq, M. Pericas, N. Navarro, E. Ayguade</i>	
Customized MPSoC Synthesis for Task Sequence	16
<i>L. Chen, N. Boichat, T. Mitra</i>	
Integrating Formal Verification and High-Level Processor Pipeline Synthesis	22
<i>E. Nurvitadhi, J. Hoe, T. Kam, S. Lu</i>	

SESSION 2: BEST PAPER CANDIDATES

USHA : Unified Software and Hardware Architecture For Video Decoding	30
<i>A. Rao, S. Nandy, H. Nikolov, E. Deprettere</i>	
Modular High-throughput and Low-latency Sorting Units for FPGAs in the Large Hadron Collider	38
<i>A. Farmahini-Farahani, A. Gregerson, M. Schulte, K. Compton</i>	
Memory-Efficient Volume Ray Tracing on GPU for Radiotherapy	46
<i>B. Zhou, X. Hu, D. Chen</i>	
System Integration of Elliptic Curve Cryptography on an OMAP Platform	52
<i>S. Morozov, C. Tergino, P. Schaumont</i>	

SESSION 3: SHORT PAPERS

ISIS: An Accelerator for Sphinx Speech Recognition	58
<i>A. Chun, J. Chang, Z. Fang, R. Iyer, M. Deisher</i>	
Dynamically Reconfigurable Architecture for a Driver Assistant System	62
<i>N. Harb, S. Niar, M. Saghir, Y. Hillali, R. Attallah</i>	
FPGA Based Parallel Architecture Implementation of Stacked Error Diffusion Algorithm	66
<i>R. Venugopal, J. Heath, D. Lau</i>	
3D Recursive Gaussian IIR on GPU and FPGAs: A Case for Accelerating Bandwidth-Bounded Applications	70
<i>J. Cong, M. Huang, Y. Zou</i>	
A Fast CUDA Implementation of Agrep Algorithm for Approximate Nucleotide Sequence Matching	74
<i>H. Li, B. Ni, M. Wong, K. Leung</i>	
Frameworks for GPU Accelerators: A Comprehensive Evaluation using 2D/3D Image Registration	78
<i>R. Membarth, F. Hannig, J. Teich, M. Korner, W. Eckert</i>	
A Massively Parallel Implementation of QC-LDPC Decoder on GPU	82
<i>G. Wang, M. Wu, Y. Sun, J. Cavallaro</i>	

SESSION 4: APPLICATION – SPECIFIC HARDWARE AND SOFTWARE SYSTEMS

ARTE: an Application-specific Run-Time Management Framework for Multi-core Systems	86
<i>G. Mariani, G. Palermo, C. Silvano, V. Zaccaria</i>	
A Hardware Acceleration Technique for Gradient Descent and Conjugate Gradient	94
<i>D. Kesler, B. Deka, R. Kumar</i>	
A Multi-Threaded Coarse-Grained Array Processor for Wireless Baseband	102
<i>T. Vander, M. Palkovic, M. Hartmann</i>	
Hardware/Software Co-Designed Accelerator for Vector Graphics Applications	108
<i>S. Chen, H. Lin, H. Wei, Y. Chen, C. Huang, Y. Chung</i>	

SESSION 5: FPGAS AND GPUS

Scalable Object Detection Accelerators on FPGAs Using Custom Design Space Exploration.....	115
<i>C. Huang, F. Vahid</i>	
A Parallel Accelerator for Semantic Search	122
<i>A. Majumdar, S. Cadambi, S. Chakradhar, H. Graf</i>	
A Novel Parallel Tier-1 Coder for JPEG2000 using GPUs	129
<i>R. Le, I. Bahar, J. Mundy</i>	
Author Index	