

# **2011 IEEE International Conference on Anti-Counterfeiting, Security and Identification**

**(ASID 2011)**

**Xiamen, China  
24 – 26 June 2011**



**IEEE Catalog Number: CFP1120C-PRT  
ISBN: 978-1-61284-631-6**

# TABLE OF CONTENTS

## SESSION1: CLOUD COMPUTING AND INFORMATION SECURITY

0001-021402	<b>A NEW P2P CAMPUS CLOUD FRAMEWORK</b> <i>Conghuan Ye, Junshan Pan</i>	1
0002-040602	<b>P2P FILE SEARCH SYSTEM BASED ON REALPEER</b> <i>Lei You, Zhongwen Li, Fang Fang, Jian Liu, Jun Hu</i>	5
0003-021404	<b>AN INDIVIDUAL ORIENTED SERVICE SUPPORT MODEL FOR CAMPUS CLOUD</b> <i>Conghuan Ye, Xiaowen Chen</i>	9
0004-050602	<b>A FAST GPU-BASED IMPLEMENTATION FOR MD5 HASH REVERSE</b> <i>Hongwei Wu, Xiangnan Liu, Weibin Tang</i>	13
0005-031501	<b>ANTI-THEFT TRACKING SYSTEM FOR AUTOMOBILES (AUTOGSM)</b> <i>G.S.Prasanth Ganesh, B.Balaji, T.A.Srinivasa Varadhan</i>	17
0006-040601	<b>THE MECHANISM TO CONTROL FILE-POLLUTION BASED ON HYBRID TRUST-MODEL IN P2P NETWORK</b> <i>Zhongwen Li, Jing Yao, Liang Shi</i>	20
0007-031202	<b>BLIND SEPARABILITY FOR SINGLE-CHANNEL MIXTURES IN SATELLITE CHANNELS</b> <i>Guosheng Rui, Bin Xu</i>	25
0008-031503	<b>AN IDENTITY-BASED GROUP-ORIENTED THRESHOLD ENCRYPTION SCHEME</b> <i>Jinghao Xing, Qiuliang Xu</i>	30
0009-030101	<b>EVOLUTION OF PRIVACY-PRESERVING DATA PUBLISHING</b> <i>Yongbin Yuan, Jing Yang, Jianpei Zhang, Sheng Lan, Junwei Zhang</i>	34
0010-031601	<b>AES FINALISTS IMPLEMENTATION FOR GPU AND MULTI-CORE CPU BASED ON OPENCL</b> <i>Xingliang Wang, Xiaochao Li, Mei Zou, Jun Zhou</i>	38

## SESSION2: PATTERN RECOGNITION AND RFID TECHNOLOGY

0011-021401	<b>CO-OCCURRENCE MATRIX FEATURES FOR FINGERPRINT VERIFICATION</b> <i>Mohammed S. Khalil, Muhammad Khurram Khan, Muhammad Imran Razzak</i>	43
0012-031102	<b>DESIGN OF EMBEDDED FINGERPRINT IDENTIFICATION SYSTEM BASED ON DSP</b> <i>Yanpeng Wang, Qing Li, Li Zhang</i>	47

0013-032301	<b>THE MULTI-QR CODES EXTRACTION METHOD IN ILLEGIBLE IMAGE BASED ON CONTOUR TRACING</b> <i>Qiaoling Liu,Xiaochao Li,Mei Zou,Jun Zhou</i>	51
0014-010502	<b>A NEW DWT &amp; MULTI-STRATEGY WATERMARK EMBEDDING ALGORITHM</b> <i>Qiwei Lin,Jisheng Tang,Xufeng Wu</i>	57
0015-042701	<b>FORMATION OF CHECKERBOARD PATTERNS IN ONE-DIMENSIONAL COMPUTATIONAL VERB CELLULAR NETWORKS</b> <i>Xiaoli Lin,Tao Yang</i>	61
0016-021503	<b>FRONTAL FACE GENERATION FROM PROFILE FACE IMAGE</b> <i>Sandesh Gupta,Shashank Kapoor,Phalguni Gupta</i>	65
0017-042601	<b>COMPUTATIONAL VERB COLOR IMAGE INTERPOLATION</b> <i>Huiqing Liu,Yinghao Liao,Tao Yang</i>	69
0018-010501	<b>MOTION VECTOR AND MODE SELECTION BASED FRAGILE VIDEO WATERMARKING ALGORITHM</b> <i>Gui Feng,Guozheng Wu</i>	73
0019-050601	<b>COMPUTATIONAL VERB SIMILARITY BETWEEN VERBS WITH DISTORTIONS OF TIME</b> <i>Juanjuan Sun,Tao Yang</i>	77
0020-010401	<b>COMPOSITE SPIRAL ANTENNA WITH II SNOWFLAKE FRACTAL PBG STRUCTURE DESIGNED FOR MODERN RFID SYSTEM</b> <i>Bin Lin,Minghe Lin,Jianhua Zhou, Baiqiang You</i>	81
0021-031505	<b>LOW POWER DESIGN OF RFID TAGS</b> <i>X. Yao, X. A. Wang, J. F. Huang, M. Ye</i>	85
0022-011101	<b>DESIGN OF LOW POWER LOW NOISE AMPLIFIER FOR PORTABLE ELECTROCARDIOGRAM RECORDING SYSTEM APPLICATIONS</b> <i>Xiao Yang,Qi Cheng,Lifen Lin,Weiwei Huang,Chaodong Ling</i>	89
0023-042501	<b>CAPACITY COMPARSION OF UWB SYSTEM BASED ON COMBINED COSINUSOID GAUSSIAN PULSES</b> <i>Bihong Lin,Guofa Cai,Mingjie Zhuang</i>	93
0024-031504	<b>3D IMAGE SKELETON ALGORITHMS</b> <i>Jiangui Wu,Hong Duan,Qi Zhong</i>	97
0025-021602	<b>PSO-BASED FUZZY IMAGE MOBILE ROBOT SYSTEMS DESIGN</b> <i>Hsuan-Ming Feng ,Hua-Ching Chen,Dong-hui Guo</i>	101
0026-051901	<b>FORMATION OF HOMOGENOUS AND FLIP-FLOP PATTERNS IN ONE-DIMENSIONAL COMPUTATIONAL VERB CELLULAR NETWORKS</b> <i>Xiaoli Lin and TaoYang</i>	106

0027-011402	<b>RESEARCH OF REAL-TIME CONTROL ALGORITHM FOR TRAFFIC LIGHTS BASED ON CPU PROCESS SCHEDULING</b>	110
	<i>Jin-rong Zhou,Xiaofang Zhou,Zhi-bin Chen,Xiao Chen</i>	
0028-011201	<b>THE APPLICATION OF LEVEL-CROSS INDUCTOR TO CURRENT-CARRYING LEAD INTELLIGENT VEHICLE</b>	115
	<i>Boda Zhang,Mudan Zhou,Yi Zhou,Zhibin Chen,Yunying Huang</i>	
0029-033104	<b>A NEW COMPUTATIONAL VERB IMAGE INTERPOLATION ALGORITHM</b>	119
	<i>Xin Wang,Yinghao Liao,Huiqing Liu,Zhujun Guo,Caiqin Yi</i>	

### **SESSION3:IC DESIGN AND SYSTEM INTEGRATION**

0030-042001	<b>THE DYNAMIC RELOCATION CACHE AND ITS ENERGY CONSUMPTION MODEL FOR LOW POWER PROCESSOR</b>	123
	<i>Hongyin Luo,Shaojun Wei,Donghui Guo</i>	
0031-021601	<b>CMOS TIME-TO-DIGITAL CONVERTER WITH LOW PVT SENSITIVITY 20.8PS RESOLUTION AND -0.25~0.22 LSB INACCURACY</b>	127
	<i>Poki Chen,Kai-Ming Wang,Chuan-Yuan Li,Po-Yu Chen,Juan-Shan Lai,Cheng-Wei Liu</i>	
0032-030401	<b>A 1.5-BIT PIPELINED STAGE WITH TIME-INTERLEAVED DUAL-PIPELINE ARCHITECTURE USED IN SHA-LESS PIPELINED ADC</b>	131
	<i>Yan Wang,Yuxin Wang,Tao Liu,Ting Li,Jinbao Lan</i>	
0033-022401	<b>DESIGN AND IMPLEMENTATION OF FDPM IN NETWORK PROCESSOR</b>	135
	<i>Kun Zeng, Zhongwen Li,Shan He</i>	
0034-030701	<b>AN 8-BIT 1MHZ SUCCESSIVE APPROXIMATION REGISTER (SAR) A/D WITH 7.98 ENOB</b>	139
	<i>Yafei Ye,Liyuan Liu,Fule Li,Dongmei Li, Zhihua Wang</i>	
0035-031403	<b>A 2GSPS 8-BIT ADC WITH DIGITAL FOREGROUND CALIBRATION TECHNOLOGY</b>	143
	<i>Zhengping Zhang,Yonglu Wang,Xinfa Huang</i>	
0036-031201	<b>A 12-BIT HIGH-SPEED ADC BASED ON GESI BICMOS PROCESS</b>	146
	<i>Liang Li,Xingfa Huang,MingYuan Xu</i>	
0037-031103	<b>A 14BIT 10MSPS LOW POWER PIPELINED ADC WITH 0.99PJ/STEP FOM</b>	150
	<i>Ting Li,Fule Li,Chun Zhang,Zhihua Wang</i>	
0038-031101	<b>A CURRENT SWITCH OF CURRENT-STEERING DAC OUTPUT STAGE</b>	154
	<i>Pu Luo,Weidong Yang,Dongbing Fu</i>	
0039-021502	<b>THE 10 GHZ WIDE TUNING AND LOW PHASE-NOISE PLL CHIP DESIGN</b>	157
	<i>Jhin-Fang Huang,Che-Chi Mao,Ron-Yi Liu</i>	
0040-031507	<b>A SHA-LESS 12-BIT 200-MS/S PIPELINE ADC</b>	161

	<i>Xiaoxiao Zhao,Fule Li,Wu Bin</i>	
0041-033103	<b>THE FPGA IMPLEMENT OF ADPLL WITHOUT RETIMED CLOCK</b> <i>Shuai Jiang, Songbai He,Fei You</i>	<b>165</b>
	<b>IP DESIGN OF UNIVERSAL MULTIPLE DEVICES SPI INTERFACE</b> <i>Tianxiang Liu,Yunfeng Wang</i>	<b>169</b>
0043-031402	<b>A CMOS LOW POWER, WIDE DYNAMIC RANGE RSSI WITH INTEGRATED AGC LOOP</b> <i>Qianqian Lei,Min Lin, Miao Peng,Zhiming Chen,Yin Shi</i>	<b>173</b>
0044-031001	<b>A HIGH SIDE CURRENT SENSING CIRCUIT WITH HIGH PSRR BASED ON BCD PROCESS</b> <i>Jianbin Lin,Huihui Cheng,Jianli Xing</i>	<b>177</b>
0045-031405	<b>A NOVEL SUB-1-V BANDGAP REFERENCE IN 0.18MM CMOS TECHNOLOGY</b> <i>Min Tan,Fan Liu,Fei Xiang</i>	<b>180</b>
0046-011103	<b>A BANDGAP VOLTAGE REFERENCE DESIGN FOR HIGH POWER SUPPLY</b> <i>Weiwei Huang,Xiao Yang,Chaodong Ling</i>	<b>184</b>
0047-031502	<b>A FEEDBACK BASED CHARGE PUMP</b> <i>Ting Li,Yuxin Wang,Ruzhang Li</i>	<b>188</b>
0048-011102	<b>DESIGN OF CMOS INDUCTOR-LESS LNA WITH ACTIVE BALUN</b> <i>Chaodong Ling,Lifen Lin,Xiao Yang,Weiwei Huang</i>	<b>191</b>
0049-033102	<b>DESIGN OF A POF RECEIVER WITH INTEGRATED PHOTODIODE IN 0.5MM BCD PROCESS</b> <i>Jifang Li,Huangping Yan,Xiang Cheng,Yuanqing Huang</i>	<b>194</b>
0050-031401	<b>A 8-BIT 200MSMAPLE/S CMOS DAC</b> <i>Binjie Zhu,Ziqi Song,Dongxu Yang,Ye Yafei,Fule Li</i>	<b>198</b>
0051-031404	<b>A TWO-STAGE AMPLIFIER WITH ACTIVE MILLER COMPENSATION</b> <i>Min Tan, Qianneng Zhou</i>	<b>201</b>
0052-031406	<b>POWER DISTRIBUTION NETWORK DESIGN OF CURRENT-STEERING, NYQUIST RATE DA CONVERTERS</b> <i>Yuhan Gao,Lintao Liu,Ruzhang Li</i>	<b>205</b>