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C.-P. Chang, Applied Materials, Inc.

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TSV Process Optimization for Reduced Device Impact on 28nm CMOS, C.L. Yu, C.H. Chang, H.Y. Wang, J.H. Chang, L.H. Huang, C.W. Kuo, S.P. Tai, S.Y. Hou, W.L. Lin, E.B. Liao, K.F. Yang, T.J. Wu, W.C. Chiou, C.H. Tung, S.P. Jeng and C.H. Yu, tsmc, Taiwan **138**

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SESSION 8B - Reliability and Stability [Shunju II]
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Chairpersons: Y. Nakao, ROHM Co., Ltd.
R. Klein, AMD

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Understanding Short-Term BTI Behavior through Comprehensive Observation of Gate-Voltage Dependence of RTN in Highly Scaled High- κ / Metal-Gate pFETs, H. Miki*, M. Yamaoka*, N. Tega*, Z. Ren**, M. Kobayashi**, C.P. D'Emic**, Y. Zhu**, D.J. Frank**, M.A. Guillorn**, D.-G. Park**, W. Haensch** and K. Torii***, *Hitachi America, Ltd., **T.J. Watson Research Center, IBM Corp., USA and ***Hitachi Ltd., Japan 148

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From Mean Values to Distributions of BTI Lifetime of Deeply Scaled FETs through Atomistic Understanding of the Degradation, M. Toledano-Luque*,**, B. Kaczer*, J. Franco*,***, Ph.J. Roussel*, T. Grasser****, T.Y. Hoffmann* and G. Groeseneken*,***, *imec, Belgium, **UCMadrid, Spain, ***KULeuven, Belgium and ****TUWien, Austria 152

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Chairpersons: T. Iwamatsu, Renesas Electronics Corp.
T.-J. K. Liu, Univ. of California, Berkely

9A-1 - 8:30
Demonstration of Low Temperature 3D Sequential FDSOI Integration Down to 50 nm Gate Length, P. Batude*, M. Vinet*, C. Xu**, B. Previtali*, C. Tabone*, C. Le Royer*, L. Sanchez*, L. Baud*, L. Brunet*, A. Toffoli*, F. Allain*, D. Lafond*, F. Aussenac*, O. Thomas*, T. Poiroux* and O. Faynot*, *CEA, LETI, MINATEC and **IMEP-LAHC, Grenoble INP - Minatec, France 158

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SESSION 9B - DRAM and CMOS Sensor [Shunju II]
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Chairpersons: H. Miyake, Elpida Memory Inc.
C. Mazure, Soitec Group

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Towards 1X DRAM: Improved Leakage 0.4 nm EOT STO-Based MIMcap and Explanation of Leakage Reduction Mechanism Showing Further Potential, M.A. Pawlak*, B. Kaczer*, W.-C. Wang**, M.-S. Kim*, M. Popovici*, J. Swerts*, K. Tomida*, K. Opsomer*, M. Schaekers*, C. Vrancken*, B. Govoreanu*, A. Belmonte*, C. Demeurisse*, I. Debusschere*, L. Altimime*, V.V. Afanas'ev** and J.A. Kittl*, *imec and **K.U. Leuven, Belgium 168

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Offset Buried Metal Gate Vertical Floating Body Memory Technology with Excellent Retention Time for DRAM Application, S.-M. Hwang*, S. Banna**, C. Tang**, S. Bhardwaj**, M. Gupta**, T. Thurgate**, D. Kim**, J. Kwon**, J.-S. Kim*, S.-H. Lee*, J.-Y. Lee*, S.-J. Chung*, J.-W. Park*, S.-W. Chung*, S.-H. Cho*, J.-S. Roh*, J.-H. Lee*, M. Van Buskirk** and S.-J. Hong*, *Hynix Semiconductor Inc., Korea and **Innovative Silicon Inc., USA 172

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Chairpersons: T. Tanaka, Tohoku Univ.
T. Ernst, CEA-LETI, MINATEC

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3D Approaches for Non-volatile Memory, J. Choi and K. S. Seol, Samsung Electronics Co., Ltd., Korea **178**

10A-2 - 10:55 **(Invited)**
From 3D-SOC to 3D Heterogeneous Systems: Technology and Applications, P. Ancey, STMicroelectronics, France **B#5**

10A-3 - 11:20 **(Invited)**
Design Methods and Tools for 3D Integration, G. De Micheli, V. Pavlidis, D. Atienza and Y. Leblebici, EPFL, Switzerland **182**

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Chairpersons: S. Yamakawa, Sony Corp.
S. Yu, Texas Instruments, Inc.

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Optical Charge-Pumping: A Universal Trap Characterization Technique for Nanoscale Floating Body Devices, S. Kim, S.-J. Choi, D.-I. Moon and Y.-K. Choi, KAIST, Korea **190**

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Proposal of a Model for Increased NFET Random Fluctuations, K. Takeuchi*, A. Nishida*, S. Kamohara*, T. Hiramoto** and T. Mogami*, *MIRAI-Selete and **The University of Tokyo, Japan **192**

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Organizer: K. Kobayashi, Kyoto Institute of Technology

Recent Studies about Computer Aided Origami Design, J. Mitani, Univ. of Tsukuba

SESSION 11A - RTN [Shunju I]
Thursday, June 16, 14:20
Chairpersons: R. Yamada, Hitachi Ltd.
R. Jammy, Sematech

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Comprehensive Understanding of Random Telegraph Noise with Physics Based Simulation, Y. Higashi, N. Momo, H.S. Momose, T. Ohguro and K. Matsuzawa, Toshiba Corporation, Japan **200**

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Direct Real-Time Observation of Channel Potential Fluctuation Correlated to Random Telegraph Noise of Drain Current Using Nanowire MOSFETs with Four-Probe Terminals, K. Ohmori*,**,***, W. Feng**,***, S. Sato****, R. Hettiarachchi**,***, M. Sato**,***, T. Matsuki**,***, K. Kakushima****, H. Iwai**** and K. Yamada*,**,***, *University of Tsukuba, **Waseda University, ***JST-CREST and ****Tokyo Institute of Technology, Japan **202**

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Impact of Random Telegraph Signaling Noise on SRAM Stability, S.O. Toh, T.-J.K. Liu and B. Nikolić, University of California, Berkeley, USA **204**

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A New Approach of NAND Flash Cell Trap Analysis Using RTN Characteristics, D. Kang*, S. Lee*, H.-M. Park*, D.-j. Lee*, J. Kim*, J. Seo*, C. Lee*, C. Song*, C.-S. Lee*, H. Shin**, J. Song*, H. Lee*, J.-H. Choi* and Y.-H. Jun*, *Samsung Electronics Co. and **Seoul National Univ., Korea **206**

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Chairpersons: N. Kasai, Tohoku Univ.
J. Lutze, Sandisk Corp.

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J. Cheek, Freescale

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Non-Gaussian Distribution of SRAM Read Current and Design Impact to Low Power Memory Using Voltage Acceleration Method, J. Wang, P. Liu, Y. Gao, P. Deshmukh, S. Yang, Y. Chen, W. Sy, L. Ge, E. Terzioglu, M. Abu-Rahma, M. Garg, S.S. Yoon, M. Han, M. Sani and G. Yeap, Qualcomm Inc, USA **220**

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