

2011 69th Annual Device Research Conference

(DRC 2011)

**Santa Barbara, California, USA
20-22 June 2011**



**IEEE Catalog Number: CFP11DRC-PRT
ISBN: 978-1-61284-243-1**

Table of Contents

Session I. PLENARY SESSION

1-10

- I.-1 **Soft, Curvilinear Semiconductor Devices for Bio-Integrated Electronics** 003
8:50 AM J. Rogers, Department of Materials Science and Engineering University of Illinois Urbana/Champaign, Champaign, Illinois, USA
- I.-2 **Devices for high performance computing beyond 14nm node- Is there anything other than Si?** 005
10:10 AM W. Haensch, IBM TJ Watson Research Center, Yorktown Heights, New York, USA
- I.-3 **The latest performance of GaN-based nonpolar and semipolar emitting devices** 009
11:10 AM Shuji Nakamura, Materials Department, University of California Santa Barbara, California, USA

Session II.A. III-V FETs

11-28

- II.A-1 **Ultra-thin Compound Semiconductors on Insulator (XOI) for MOSFETS and TFETS** 013
1:30 PM R. Kapadia^{1,2,3}, K. Takei^{1,2,3}, A. C. Ford^{1,2,3}, H. Fang^{1,2,3}, S. Chuang^{1,2,3}, M. Madsen^{1,2,3}, S. Krishna⁴ and A. Javey^{1,2,3}, ¹Electrical Engineering and Computer Sciences, University of California, Berkeley, California, ²Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California, ³Berkeley Sensor and Actuator Center, University of California, Berkeley, California, and ⁴Center for High Technology Materials, University of New Mexico, Albuquerque, New Mexico, USA
- II.A-2 **Experimental Investigation of Scalability and Transport in In_{0.7}Ga_{0.3}As Multi-Gate Quantum Well FET (MuQFET)** 017
2:10 PM L. Liu, V. Saripalli, V. Narayanan and S. Datta, The Pennsylvania State University, University Park, Pennsylvania, USA
- II.A-3 **60 nm gate length Al₂O₃ / In_{0.53}Ga_{0.47}As gate-first MOSFETs using InAs raised source-drain regrowth** 019
2:30 PM A. D. Carter, J. J. M. Law, E. Lobisser, G. J. Burek, W. J. Mitchell, B. J. Thibeault, A. C. Gossard, and M. J. W. Rodwell, ECE Department, University of California, Santa Barbara, California, USA
- II.A-4 **15 nm diameter InAs nanowire MOSFETs** 021
2:50 PM A. W. Dey¹, C. Thelander², M. Borgström², B. Mattias Borg², E. Lind², and L.-E. Wernersson¹, ¹Dept. of Electrical and Information Technology and ²Dept. of Solid State Physics, Lund University, Lund, SWEDEN
- II.A-5 **The Nanoelectric Modeling Tool NEMO5: Capabilities, Validation and Applications to Sb-Heterostructures** 023
3:30 PM S. Steiger¹, M. Povolotskyi¹, H.-H. Park¹, T. Kubis¹, G. Hegde¹, B. Haley¹, M. Rodwell² and G. Klimeck^{1,3}, ¹Network for Computational Nanotechnology, Purdue University, West Lafayette Indiana, USA and ²University of California, Santa Barbara, California, USA
- II.A-6 **Experimental Determination of Dominant Scattering Mechanisms in Scaled InAsSb Quantum Well** 027
4:10 PM A. Agrawal¹, A. Ali¹, R. Misra², P. E. Schiffer², B. R. Bennett³, J. B. Boos³ and S. Datta¹, ¹Department of Electrical Engineering, The Pennsylvania State University, University Park, Pennsylvania, USA ²Department of Physics, The Pennsylvania State University, University Park, Pennsylvania, USA, and ³Naval Research Laboratory, Washington, District of Columbia, USA

- II.B-1 **Integration of High Quality Top-Gated Graphene Field Effect Devices on 150 mm Substrate** 031
1:30 PM J. Heo, H.-J. Chung, S.-H. Lee, H. Yang, J. Shin, U-I. Chung, S. Seo, Semiconductor Device Lab, Samsung Advanced Institute of Technology, Yongin-si, KOREA
- II.B-2 **Complementary-Type Graphene Inverters Operating at Room-Temperature** 033
1:50 PM H.-Y. Chen and J. Appenzeller, ECE Department and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA
- II.B-3 **Gate capacitance scaling and graphene field-effect transistors with ultra-thin top-gate dielectrics** 035
2:10 PM B. Fallahazad, K. Lee, S. Kim, C. Corbet, E. Tutuc, Microelectronics Research Center, University of Texas at Austin, Austin, Texas, USA
- II.B-4 **Synthesis and Applications of Graphene for Flexible Electronics** 037
2:30 PM B. H. Hong, Department of Chemistry & SKKU Advanced Institute of Nanotechnology, Sungkyungwan University, Suwon, KOREA
- II.B-5 **Sub-10 nm Epitaxial Graphene Nanoribbon FETs** 039
3:30 PM K. Tahy¹, W. S. Hwang¹, J. L. Tedesco², R. L. Myers-Ward², P.M. Campbell², C. R. Eddy² Jr., D. K. Gaskill², H. Xing¹, A. Seabaugh¹, and D. Jena¹, ¹Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA and ²U.S. Naval Research Laboratory, Washington, District of Columbia, USA
- II.B-6 **Effect of Oxide Thickness Scaling on Self-Heating in Graphene Transistors** 041
3:50 PM S. Islam, M.-H. Bae, V. Dorgan, and E. Pop, Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, Illinois, USA and Micro and Nanotechnology Lab, Urbana, Illinois, USA
- II.B-7 **Graphene Quantum Capacitance Varactors for Wireless Sensing Applications** 043
3:50 PM S. J. Koester, University of Minnesota-Twin Cities, Minneapolis, Minnesota, USA

- III-1 **Effects of Heavily Doped Source on the Subthreshold Characteristics of Nanowire Tunneling Transistors** 051
M. A. Khayer and R. K. Lake, Laboratory for Terascale and Terahertz Electronics (LATTE), Department of Electrical Engineering, University of California, Riverside, California, USA
- III-2 **Spatially resolved photovoltaic performance of axial GaAs nanowire pn-diodes** 053
A. Lysov, C. Gutsche, M. Offer, I. Regolin, W. Prost, F.-J. Tegude, Center for Nanointegration Duisburg-Essen, University of Duisburg-Essen, Duisburg, GERMANY
- III-3 **Low loss AlInN/GaN Monolithic Microwave Integrated Circuit Switch** 055
A. Sattu¹, D. Billingsley¹, J. Deng¹, J. Yang¹, R. Gaska¹, M. Shur², G. Simin³, ¹Sensor Electronic Technology, Inc., Columbia, South Carolina, USA, ²Electrical and Computer Science Engineering, Rensselaer Polytechnic Institute, Troy, New York, USA, and ³Electrical Engineering, University of South Carolina, Columbia, South Carolina, USA
- III-4 **High-Mobility Organic Thin-Film Transistors with Photolithographically Patterned Top Contacts** 057
U. Zschieschang¹, N. H. Hansen², J. Pflaum², T. Yamamoto³, K. Takimiya³, H. Kuwabara⁴, M. Ikeda⁴, T. Sekitani⁵, T. Someya⁵, and H. Klauk¹, ¹Max Planck Institute for Solid State Research, Stuttgart, GERMANY, ²University Würzburg and ZAE Bayer e.V., GERMANY, ³Hiroshima University, Higashi-Hiroshima, JAPAN, ⁴Nippon Kayaku Co., Ltd., Kita-ku, Tokyo, JAPAN, and ⁵University of Tokyo, Tokyo, JAPAN

- III-5 **High Breakdown Voltage ZnMgO/In-Ga-Zn-O Heterostructure Transistors** 059
J. Yamaguchi, I. Soga, and T. Iwai, Fujitsu Laboratories Ltd., Atsugi, Kanagawa, JAPAN
- III-6 **High-Resolution Temperature Sensing with Source-Gated Transistors** 061
R. A. Sporea, J. M. Shannon, and S. R. P. Silva, Advanced Technology Institute, FEPS, University of Surrey, Guildford, Surrey, UNITED KINGDOM
- III-7 **Voltage-Controlled Spin-Wave-Based Logic Gate** 063
T. Liu and G. Vignale, Department of Physics and Astronomy, University of Missouri, Columbia, Missouri, USA
- III-8 **Effect of Disorder on Superfluidity in Double Layer Graphene** 065
B. Dellabetta and M. J. Gilbert, Department of Electrical and Computer Engineering and Micro and Nanotechnology Laboratory, University of Illinois, Urbana, Illinois, USA
- III-9 **Dual Pillar Spin Transfer Torque MRAM with tilted magnetic anisotropy for fast and error-free switching and near-disturb-free read operations** 067
N. N. Mojumder, S. K. Gupta and K. Roy, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA
- III-10 **Giant Magnetoelectric Effect in Nanofabricated $\text{Pb}(\text{Zr}_{0.52}\text{Ti}_{0.48})\text{O}_3\text{-Fe}_{85}\text{B}_5\text{Si}_{10}$ Cantilevers and Resonant Gate Transistors** 069
F. Li¹, Z. Fang¹, R. Misra³, S. Tadigadapa¹, Q. Zhang^{1,2} and Suman Datta¹, ¹Electrical Engineering, ²Materials Research Institute, and ³Physics Department, The Pennsylvania State University, University Park, Pennsylvania, USA
- III-11 **Observation of Trap-Assisted Steep Sub-threshold Swing in Schottky Source/Drain $\text{Al}_2\text{O}_3/\text{InAlN}/\text{GaN}$ MISHEMT** 071
Q. Zhou¹, H. Chen¹, C. Zhou¹, Z. Feng², S. Cai², K. J. Chen¹, ¹Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong and ²National Key Laboratory of Application Specific Integrated Circuit, Hebei Semiconductor Research Institute, Shijiazhuang, CHINA
- III-12 **Towards Electronics at 1000 °C** 073
D. Maier¹, M. Alomari¹, N. Grandjean², J.-F. Carlin², M.-A. Diforte-Poisson³, C. Dua³, S. L. Delage³, and E. Kohn¹, ¹Institute of Electron Devices and Circuits, University of Ulm, Ulm, GERMANY, ²École polytechnique fédérale de Lausanne, Lausanne, SWITZERLAND, and ³III/V Lab, Marcoussis, FRANCE
- III-13 **Bias Temperature Stress Analysis of ZnO Thin Film Transistors with HfO_2 Gate Dielectrics** 075
J. J. Siddiqui¹, J. D. Phillips¹, K. Leedy², and B. Bayraktaroglu², ¹EECS Department, University of Michigan, Ann Arbor, Michigan, USA and ²Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, Ohio, USA
- III-14 **Carbon Nanotube Purified Ink-Based Printed Thin Film Transistors: Novel Approach in Controlling the Electrical Performance** 077
N. Rouhi, D. Jain, and P. J. Burke, Electrical Engineering and Computer Science Department, University of California-Irvine, Irvine, California, USA
- III-15 **Monolayer MoS_2 Transistors – Ballistic Performance Limit Analysis** 079
K. Ganapathi, Y. Yoon, and S. Salahuddin, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California, USA
- III-16 **RF performance projections for 2D Graphene Transistors: Role of Parasitics at the Ballistic transport limit** 081
P. Zhao¹, D. Jena¹, and S. O. Koswatta², ¹Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA and ²IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York, USA
- III-17 **High Performance N- and P-Type Gate-All-Around Nanowire MOSFETs Fabricated on Bulk Si by CMOS-Compatible Process** 083
Y. Song, H. Zhou, Q. Xu, J. Luo, C. Zhao and Q. Liang, Key Laboratory of Microelectronics Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, CHINA

- III-18 **The effect of field effect device channel dimensions on the effective mobility of graphene** 085
A. Venugopal¹, J. Chan¹, W. P. Kirk¹, L. Colombo² and E. M. Vogel¹, ¹University of Texas at Dallas, and ²Texas Instruments Incorporated, Dallas, Texas, USA
- III-19 **Top-gated single-electron transistor in germanium nanowires** 087
S.-K. Shin, S. Huang, N. Fukata, and K. Ishibashi, Advanced Device Laboratory, RIKEN, Wako, Saitama, JAPAN
- III-20 **Reliability of Ambipolar Switching Poly-Si Diodes for Cross-Point Memory Applications** 089
M. H. Lee¹, C.-Y. Kao¹, C.-L. Yang¹, Y.-S. Chen², H. Y. Lee², F. Chen², and M.-J. Tsai² ¹Institute of Electro-Optical Science and Technology, National Taiwan Normal University, Taipei, TAIWAN and ²Electronics and Optoelectronics Research Laboratories, Industrial Technology Research Institute, Hsinchu, TAIWAN
- III-21 **Electrochemical supercapacitor based on flexible pillar graphene nanostructures** 091
J. Lin¹, J. Zhong¹, D. Bao², J. Reiber-kyle³, W. Wang⁴, V. Vullev², M. Ozkan³, C. S. Ozkan^{1,4}, ¹Department of Mechanical Engineering, ²Department of Bioengineering, ³Department of Electrical Engineering, and ⁴Materials Science and Engineering Program, University of California, Riverside, California, USA
- III-22 **“Zero” Drain-Current Drift of Inversion-Mode NMOSFET on InP (111)A Surface** 093
C. Wang, M. Xu, R. Colby, E. A. Stach and P. D. Ye, School of Electrical and Computer Engineering and Birk Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA
- III-23 **Improvement of efficiency in inverted bottom-emission white OLEDs by doping the hole transport layer** 095
H. Lee¹, J. Kwak², J. Lim³, K. Char³, S. Lee⁴ and C. Lee¹, ¹School of Electrical Engineering and Computer Science, Inter-University Semiconductor Research Center, Seoul National University, Seoul, KOREA, ²Department of Electronics Engineering, Dong-A University, Busan, KOREA, ³School of Chemical and Biological Engineering, Intelligent Hybrids Research Center, Seoul National University, Seoul, KOREA, and ⁴Department of Chemistry, Seoul National University, Seoul, KOREA
- III-24 **Vertical Organic Field-Effect Transistor Array Fabrication Based on Laser Holography Lithography Process** 097
D. Kim and Y. Hong, Department of Electrical Engineering and Computer Science, Seoul National University, Seoul, KOREA
- III-25 **Ambipolar Nano-crystalline-silicon TFTs with Submicron Dimensions and Reduced Threshold Voltage Shift** 099
A. Subramaniam, K. D. Cantley, R. A. Chapman, B. Chakrabarti, and E. M. Vogel, Department of Electrical Engineering, The University of Texas at Dallas, Richardson, Texas, USA
- III-26 **Monolithically Grown In_xGa_{1-x}As Nanowire on Silicon Tandem Solar Cells with High Efficiency** 101
J. C. Shin¹, K. H. Kim², H. Hu², K. J. Yu¹, J. A. Rogers^{2,1}, J.-M. Zuo², and X. Li^{1,2}, ¹Department of Electrical and Computer Engineering and ²Department of Materials Science and Engineering, University of Illinois, Urbana, Illinois, USA
- III-27 **3D Simulation of Electrical Characteristic Fluctuation Induced by Interface Traps at Si/high-k Oxide Interface and Random Dopants in 16-nm-Gate CMOS Devices** 103
H.-W. Cheng, Y.-Y. Chiu, F.-H. Li, and Y. Li, Department of Electrical Engineering, National Chiao Tung University, Hsinchu, TAIWAN
- III-28 **Creating dynamic nanowire devices using wrapped gates** 105
K. Storm, G. Nylund, M. Borgström, J. Wallentin, C. Fasth, C. Thelander and L. Samuelson, Solid State Physics, the Nanometer Structure Consortium, Lund University, Lund, SWEDEN
- III-29 **InAlAs/InGaAs Metamorphic HEMT and MOS-HEMT with Regrown Source/Drain by MOCVD** 107
X. Zhou, Q. Li, and K. M. Lau, Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, HONG KONG

- III-30 **Numerical Study of Electronic Transport Through Bilayer Graphene Nanoribbons** 109
K. M. M. Habib and R. K. Lake, Department of Electrical Engineering, University of California, Riverside, California, USA
- III-31 **Tunnel-FET Architecture with Improved Performance due to Enhanced Gate Modulation of the Tunneling Barrier** 111
L. De Michielis¹, L. Lattanzio¹, P. Palestri², L. Selmi², and A. M. Ionescu¹, ¹ Nanoelectronic Devices Laboratory (Nanolab), Ecole Polytechnique Fédérale de Lausanne, SWITZERLAND and ²Department of Electrical, Managerial and Mechanical Engineering, University of Udine, Udine, ITALY
- III-32 **Orientation dependent complex bandstructure of Si_{1-x}Ge_x alloys** 113
A. Ajoy¹, K. V. R. M. Murali², S. Karmalkar¹, and S.E. Laux³, ¹Indian Institute of Technology Madras, INDIA, ²IBM SRDC, Bangalore, INDIA, and ³IBM SRDC, T. J. Watson Center, Yorktown Heights, New York, USA
- III-33 **Towards Planar GaAs Nanowire Array High Electron Mobility Transistor** 115
X. Miao, and X. Li, Department of Electrical and Computer Engineering, Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, Urbana, Illinois, USA
- III-34 **Interface States at high-κ/InGaAs interface: H₂O vs. O₃ based ALD Dielectric** 117
H. Madan^{1,2}, D. Veksler¹, Y.T. Chen^{1,3}, J. Huang¹, N. Goel¹, G. Bersuker¹ and S. Datta², ¹SEMATECH, Albany, New York, USA, ²The Pennsylvania State University, University Park, Pennsylvania, USA, and ³University of Texas at Austin, Texas, USA
- III-35 **C-V Measurements of Single Vertical Nanowire Capacitors** 119
P. Mensch, K. E. Moselund, S. Karg, E. Lörtscher, M. T. Björk, H. Schmid and H. Riel, IBM Research – Zurich, Rüschlikon, SWITZERLAND
- III-36 **Barrier Height, Interface Charge & Tunneling Effective Mass in ALD Al₂O₃/AlN/GaN HEMTs;** 121
S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing, D. Jena, University of Notre Dame, Department of Electrical Engineering, Notre Dame, Indiana, USA
- III-37 **Graphene Field-Effect Transistors Using Large-Area Monolayer Graphene Grown by Chemical Vapor Deposition on Co Thin Films** 123
M. E. Ramón¹, A. Gupta¹, C. Corbet¹, D. A. Ferrer¹, H.C.P. Movva¹, G. Carpenter², L. Colombo³, G. Bourianoff⁴, M. Doczy⁴, D. Akinwande¹, E. Tutuc¹, and S.K. Banerjee¹, ¹Microelectronics Research Center, The University of Texas at Austin, Austin, Texas, USA, ²IBM Research, Austin, Texas, USA, ³Texas Instruments Incorporated, Dallas, Texas, USA, and ⁴Intel Corporation, Austin, Texas, USA
- III-38 **Modeling of Dielectric Breakdown-Induced Time-Dependent STT-MRAM Performance Degradation** 125
G. Panagopoulos, C. Augustine and K. Roy, School of ECE, Purdue University, West Lafayette, Indiana, USA
- III-39 **Introduction of ALD Beryllium Oxide Gate Dielectric for III-V MOS Devices** 127
T. Akyol¹, J. H. Yum^{1,5}, D. A. Ferrer¹, M. Lei², M. Downer², C. W. Bielawski³, T. W. Hudnall⁴, G. Bersuker⁵, J.C. Lee¹, S. K. Banerjee¹, ¹Microelectronics Research Center – Dept. of Electrical and Computer Eng., ²Dept. of Physics, ³Dept. of Chemistry, University of Texas at Austin, Texas, USA, ⁴Texas State University at San Marcos, San Marcos, Texas, USA and ⁵Sematech Austin, Texas, USA
- III-40 **Transport Properties of CVD-Grown Graphene Nanoribbon Field-Effect Transistors** 129
A. S. Lyons, A. Behnam, E. K. Chow, and E. Pop, Dept. of Electrical and Computer Engineering, Micro and Nanotechnology Lab, University of Illinois, Urbana-Champaign, Illinois, USA
- III-41 **Protein Nanopore-gated Bio-transistor for Membrane Ionic Current Recording** 131
T.-S. Lim, D. Jain, and P. J. Burke, Integrated Nanosystems Research Facility, Department of Electrical Engineering and Computer Science, University of California Irvine, Irvine, California, USA
- III-42 **Tunnel FET-Based Pass-Transistor Logic for Ultra-Low-Power Applications** 133
S. H. Kim, Z. A. Jacobson, P. Patel, C. Hu, and T.-J. K. Liu, EECS Department, University of California, Berkeley, California, USA

- III-43 **Metal/III-V Effective Barrier Height Tuning using ALD High- κ Dipoles** 135
J. Hu, K. Saraswat, and H.-S. P. Wong, Department of Electrical Engineering, Stanford University, Stanford, California, USA
- III-44 **Intrinsic DC Operation and Performance Potential of 50nm Gate Length Hydrogen-terminated Diamond Field Effect Transistors** 137
D. A. J. Moran¹, O. J. L. Fox², H. McLelland¹, S. Russell¹, P. W. May², ¹The School of Engineering, The University of Glasgow, Glasgow, United Kingdom and ²The School of Chemistry, The University of Bristol, Bristol, United Kingdom
- III-45 **Improvement of f_T in InAl(Ga)N barrier HEMTs by Plasma Treatments** 139
R. Wang¹, G. Li¹, T. Fang¹, O. Laboutin², Y. Cao², J. W. Johnson², G. Snider¹, P. Fay¹, D. Jena¹, and H. Xing¹, ¹Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA and ²Kopin Corporation, Tauton, Massachusetts, USA
- III-46 **Scaling behavior and velocity enhancement in Self-aligned N-polar GaN/AlGaIn HEMTs with maximum f_T of 163 GHz** 141
N. Nidhi¹, S. Dasgupta¹, D. F. Brown², J. S. Speck¹ and U. K. Mishra¹, ¹ECE Department, University of California Santa Barbara, Santa Barbara, California, USA and ²Hughes Research Laboratories, Malibu, California, USA
- III-47 **Fermi-level Pinning at Metal/Antimonides Interface and Demonstration of Antimonides-based Metal S/D Schottky pMOSFETs** 143
Z. Yuan¹, A. Nainani¹, J.-Y. Lin¹, B. R. Bennett², J. B. Boos², M. G. Ancona² and K. C. Saraswat¹, ¹Dept. of Electrical Engineering, Stanford University, California, USA and ²Naval Research Laboratory, Washington, District of Columbia, USA
- III-48 **Uniaxially Tensile Strained Accumulation-Mode Gate-All-Around Si Nanowire nMOSFETs** 145
M. Najmzadeh, D. Bouvet, W. Grabinski, and A. M. Ionescu, Nanoelectronic devices lab., Swiss Federal Institute of Technology (EPFL), Lausanne, SWITZERLAND
- III-49 **Spintronics Search Engines** 147
H. Dery¹, H. Wu¹, B. Ciftcioglu¹, M. Huang¹, Y. Song², R. Kawakami³, J. Shi³, I. Krivorotov⁴, I. Zutic⁵, and L. J. Sham⁶, ¹Department of Electrical and Computer Engineering, University of Rochester, Rochester, New York, USA, ²Department of Physics, University of Rochester, Rochester, New York, USA, ³Department of Physics, University of California Riverside, Riverside, California, USA, ⁴Department of Physics, University of California Irvine, Irvine, California, USA, ⁵Department of Physics, State University of New-York at Buffalo, Buffalo, New York, USA, and ⁶Department of Physics, University of California San Diego, San Diego, California, USA
- III-50 **Low Frequency Transconductance and Output Resistance Dispersion of Epitaxial Graphene Nanoribbon-based Field Effect Transistors** 149
G. Aroshvili¹, N. Meng², D. Vignaud², D. Pavlidis¹ and H. Happy², ¹Department of High Frequency Electronics, Darmstadt University of Technology, Darmstadt, GERMANY and ²Institute of Electronics, Microelectronics and Nanotechnology, CNRS and Univ.p Lille 1, Villeneuve d'Ascq, FRANCE
- III-51 **InAs/SiGe on Si Nanowire Tunneling Field Effect Transistors** 151
C. Kshirsagar and S. J. Koester, University of Minnesota-Twin Cities, Minneapolis, Minnesota, USA

Session IV.A. Spin/Memory

153-174

- IV.A-1 **Electrical measurement of the spin Hall effects in Fe/In_xGa_{1-x}As heterostructures** 155
8:20 E. S. Garlid¹, Q. O. Hu², C. Geppert¹, M. K. Chan¹, C. J. Palmström^{2,3}, and P. A. Crowell¹, ¹School of Physics and Astronomy, University of Minnesota, Minneapolis, Minnesota, USA, ²Dept. of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA, and ³Dept. of Materials, University of California, Santa Barbara, California, USA
- IV.A-2 **Simultaneous Spin and Charge Transport in Gated Si Devices** 159
9:00 J. Li and I. Appelbaum, Center for Nanophysics and Advanced Materials and Department of Physics, University of Maryland, College Park, Maryland, USA

- IV.A-3 **Unidirectional information transfer with cascaded All Spin Logic devices: A Ring Oscillator** 161
9:20 AM S. Srinivasan^{1,2}, A. Sarkar^{1,2}, B. Behin-Aien^{1,2}, and S. Datta^{1,2}, ¹School of Electrical and Computer Engineering, Purdue University, W. Lafayette, Indiana, USA and ²NSF Network for Computational Nanotechnology (NCN), W. Lafayette, Indiana, USA
- IV.A-4 **Proposal for piezoelectric-ferromagnet bilayer based microwave Oscillators without any external magnetic field or spin transfer torque** 163
9:40 AM D. Bhowmik and S. Salahuddin, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley California, USA
- IV.A-5 **Orthogonal Spin Transfer MRAM** 165
10:20 AM D. Bedau¹, D. Backes¹, H. Liu¹, J. Langer², P. Manandhar³ and A. D. Kent¹, ¹Department of Physics, New York University, New York, New York, USA, ²Singulus Technologies AG, Kahl am Main, GERMANY, and ³Spin-Transfer Technologies, Quincy, Massachusetts, USA
- IV.A-6 **Thermal Effects and Instability in Unipolar Resistive Switching Devices** 167
10:40 AM A. Chen and M.-R. Lin, Strategic Technology Group, GLOBAL FOUNDRIES, Sunnyvale, California, USA
- IV.A-7 **A Hybrid Ferroelectric and Charge Nonvolatile Memory** 169
11:00 AM S. R. Rajwade, K. Auluck, J. Shaw, K. Lyon and E. C. Kan, School of Electrical and Computer Engineering, Cornell University, Ithaca, New York, USA
- IV.A-8 **Spin-torque switchable perpendicular magnetic junctions for solid-state memory** 171
11:20 AM J. Z. Sun^{1,2}, R. P. Robertazzi¹, J. J. Nowak¹, P. L. Trouilloud¹, G. Hu¹, M. C. Gaidis¹, S. L. Brown¹, D. W. Abraham¹, E. J. O'Sullivan¹, W. J. Gallagher¹, D. C. Worledge¹, and A. D. Kent², ¹IBM-MagIC MRAM Development Alliance, IBM T. J. Watson Research Center, Yorktown Heights, New York, USA and ²Dept of Physics, New York University, New York, USA

Session IV.B. Alternative Transistor Concepts

175-190

- IV.B-1 **Combinational and Sequential Logic with Transistors based on Individual Carbon Nanotubes** 177
8:20 AM H. Ryu¹, D. Kälblein¹, U. Zschieschang¹, O. G. Schmidt², and H. Klauk¹, ¹Max Planck Institute for Solid State Research, Stuttgart, GERMANY and ²Faculty of Electrical Engineering and Information Technology, Chemnitz University of Technology, GERMANY
- IV.B-2 **Comparative Study of Fabricated Junctionless and Inversion-mode Nanowire FETs** 179
8:40 AM C.-H. Park¹, M.-D. Ko¹, K.-H. Kim¹, C.-W. Sohn¹, C. K. Baek¹, Y.-H. Jeong^{1,2}, and J.-S. Lee^{1,2}, ¹Dept. of Electronic and Electrical Engineering, and ²Division of IT-Convergence Engineering, POSTECH, Pohang, Gyeongbuk, KOREA
- IV.B-3 **Fabrication of Vertical InAs-Si Heterojunction Tunnel Field Effect Transistors** H. Schmid, K. E. 181
9:00 AM Moselund, M. T. Björk, M. Richter, H. Ghoneim, C. D. Bessire and H. Riel, IBM Research – Zurich, Rüschlikon, SWITZERLAND
- IV.B-4 **Challenges for Post-CMOS Devices & Architecture** 183
9:20 AM J. Welser^{1,2} and K. Bernstein², ¹SRC-NRI, Durham, North Carolina, USA and ²IBM Research, Yorktown Heights, New York & San Jose, California, USA
- IV.B-5 **Correlated Oxide Phase Transition Switch: A Paradigm in Electron Devices** 187
10:20 AM Z. Yang, C. Ko, V. Balakrishnan, and S. Ramanathan Harvard School of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts, USA
- IV.B-6 **Lateral Gate Suspended-Body Carbon Nanotube Field-Effect-Transistors with Sub-100nm Air Gap by Precise Positioning Method** 189
11:00 AM J. Cao and A. M. Ionescu, Nanoelectronic Devices Laboratory (Nanolab), Ecole Polytechnique Fédérale de Lausanne, Lausanne, SWITZERLAND

- V.A-1 **Si-based Tunnel Field-Effect Transistors for Low-Power Nano-Electronics** 193
1:30 PM A. S. Verhulst¹, W. G. Vandenberg^{1,2}, D. Leonelli^{1,2}, R. Rooyackers¹, A. Vandooren¹, J. Zhuge⁴, K-H. Kao, B. Sorée^{1,5}, W. Magnus^{1,5}, M. V. Fischetti⁶, G. Pourtois¹, C. Huyghebaert¹, R. Huang⁴, Y. Wang⁴, K. De Meyer¹, W. Dehaene^{1,2}, M. M. Heyns^{1,3}, and G. Groeseneken^{1,2}, ¹imec, Leuven, BELGIUM, ²Department of Electrical Engineering, ³Department of Metallurgy and Materials Engineering, K.U.Leuven, Leuven, BELGIUM, ⁴Institute of Microelectronics, Peking University, Beijing, CHINA, ⁵Department of Physics, Universiteit Antwerpen, Wilrijk, BELGIUM; ⁶Department of Materials Science and Engineering, University of Texas Dallas, Richardson, Texas, USA
- V.A-2 **Compact Model and Performance Estimation for Tunneling Nanowire FET** 197
2:10 PM P. M. Solomon, D. J. Frank, and S.O. Koswatta, IBM, SRDC, T.J. Watson Research. Center, Yorktown Heights, New York, USA
- V.A-3 **Using Dimensionality to Achieve a Sharp Tunneling FET (TFET) Turn-On** 199
2:30 PM S. Agarwal and E. Yablonovitch, University of California, Berkeley, California, USA
- V.A-4 **Investigation on Superlattice Heterostructures for Steep-Slope Nanowire FETs** 201
2:50 PM E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi and G. Baccarani ARCES and DEIS, University of Bologna, Bologna, ITALY
- V.A-5 **Self-aligned Gate NanoPillar In_{0.53}Ga_{0.47}As Vertical Tunnel Transistor** 203
3:30 PM D. K. Mohata, R. Bijesh, V. Saripalli, T. Mayer and S. Datta, The Pennsylvania State University, University Park, Pennsylvania, USA
- V.A-6 **Self-aligned InAs/Al_{0.45}Ga_{0.55}Sb vertical tunnel FETs** 205
3:50 PM G. Zhou¹, Y. Lu¹, R. Li¹, Q. Zhang¹, W. Hwang¹, Q. Liu¹, T. Vasen¹, H. Zhu², J. Kuo², S. Koswatta³, T. Kosel¹, M. Wistey¹, P. Fay¹, A. Seabaugh¹, and H. G. Xing¹, ¹Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA, ²IntelliEPI, Richardson, Texas, USA, and ³IBM T. J. Watson Research Center, Yorktown Heights, New York, USA
- V.A-7 **P-type Tunneling FET on Si (110) Substrate with Anisotropic Effect** 207
4:10 PM M. H. Lee¹, C.-Y. Kao¹, C.-L. Yang¹, and C.-H. Lee², ¹Institute of Electro-Optical Science and Technology, National Taiwan Normal University, Taipei, TAIWAN and ²Graduate Institute of Electronics Engineering (GIEE) and Department of Electrical Engineering, National Taiwan University, Taipei, TAIWAN
- V.A-8 **Late News**
4:30 PM
- V.A-9 **Late News**
4:50 PM

- V.B-1 **Anomalous output conductance in N-polar GaN-based MIS-HEMTs** 211
1:30 PM M. H. Wong¹, U. Singiseti¹, J. Lu¹, J. S. Speck², and U. K. Mishra¹, ¹Electrical and Computer Engineering and ²Materials Departments University of California, Santa Barbara, California, USA
- V.B-2 **Normally-off Gate-Recessed AlGaIn/GaN-on-Si Hybrid MOS-HFET with Al₂O₃ Gate Dielectric** 213
1:50 PM A. L. Corrion, M. Chen, R. Chu, S. D. Burnham, S. Khalil, D. Zehnder, B. Hughes, and K. Boutros, HRL Laboratories LLC, Malibu, California, USA

- V.B-3
2:10 PM **N-Polar AlGaIn/GaN MIS-HEMTs on SiC with a 16.7 W/mm Power Density at 10 GHz Using an Al₂O₃ Based Etch Stop Technology for the Gate Recess**
S. Kolluri, S. Keller, S. P. DenBaars and U. K. Mishra, Department of ECE, University of California, Santa Barbara, California, USA
- V.B-4
2:30 PM **Total GaN Solution for Electrical Power Conversion**
Y.-F. Wu, R. Coffie, N. Fichtenbaum, Y. Dora, C.S. Suh, L. Shen, P. Parikh and U.K. Mishra, Transphorm Inc., Goleta, California, USA
- V.B-5
3:30 PM **First AlN/GaN HEMTs power measurement at 18 GHz on Silicon substrate**
F. Medjdoub, M. Zegaoui, D. Ducatteau, N. Rolland and P.A. Rolland, IEMN, Villeneuve d'Ascq, FRANCE
- V.B-6
3:50 PM **Enhanced mobility for MOCVD grown AlGaIn/GaN HEMTs on Si substrate**
S. L. Selvaraj, A. Watanabe and T. Egawa, Research Center for Nano-Device and System, Nagoya Institute of Technology, Gokiso-cho, Showa-ku, Nagoya, JAPAN
- V.B-7
4:10 PM **High Performance GaN-on-Si Power Switch: Role of Substrate Bias in Device Characteristics**
R. Chu, D. Zehnder, B. Hughes, and K. Boutros, HRL Laboratories LLC, Malibu, California, USA

Rump Sessions

225-226

- R.1
8:30 PM **Large Area OFETs: Organic or Oxide?**
Session Organizers: Ioannis Kymissis, Columbia University and Yongtaek Hong, Seoul National University
- R.2
8:30 PM **What is the Ultimate Low Power Device?**
Session Organizers: Kirsten Moselund, IBM, Siyuranga Koswatta, IBM, and Erik Lind, Lund University
- R.3
8:30 PM **Graphene--What is it good for?**
Session Organizers: Eric Pop, University of Illinois Urbana-Champaign, Dimitris Pavlidis, Technical University Darmstadt, and Jeong Moon, HRL

Joint DRC/EMC Plenary Session

227-228

- 8:30 AM **New Concepts and Materials for Solar Power Conversion**
Wladyslaw Walukiewicz, Lawrence Berkeley National Laboratory

Session VI.A pFETs

229-238

- VI.A-1
10:00 AM **High Mobility Strained P-Channel Germanium Quantum Well Field Effect Transistor for Low Power (V_{cc} = 0.5 V) III-V CMOS Applications**
R. Pillarisetty, Intel Corporation, Components Research, Technology and Manufacturing Group, Hillsboro, Oregon, USA
- VI.A-2
10:40 AM **Performance enhancement of GaAs UTB pFETs by strain, orientation and body thickness engineering**
A. Paul¹, S. Mehrotra¹, G. Klimeck¹ and Mark Rodwell², ¹ECE Department and NCN, Purdue University, West Lafayette, Indiana, USA and ²ECE Department, University of California, Santa Barbara, California, USA

- VI.A-3 **Highly-Strained SGOI p-Channel MOSFETs Fabricated by Applying Ge Condensation Technique to Strained-SOI Substrates** G H
11:00 AM J. Suh, R. Nakane, N. Taoka, M. Takenaka and S. Takagi, School of Engineering, The University of Tokyo, Tokyo, JAPAN
- VI.A-4 **Hole Mobility Enhancement in Uniaxially Strained SiGe FINFETs: Analysis and Prospects** G +
11:20 AM R. Bijesh¹, I. Ok², M. Baykan², C. Hobbs², P. Majhi², R. Jammy², and S. Datta¹, ¹The Pennsylvania State University, University Park, Pennsylvania, USA and ²Sematech, Austin, Texas, USA

Session VI.B Thin- Film

239-250

- VI.B-1 **Defect Analysis of Roll-to-Roll SAIL Manufactured Flexible Display Backplanes** G F
10:00 AM C. Taussig¹, R. E. Elder¹, W. B. Jackson¹, A. Jeans¹, M. Jam, E. Holland¹, H. Luo¹, J. Maltabes¹, C. Perlov¹, S. Trovinger¹, M. Almanza-Workman², R. A. Garcia², H. Kim², O. Kwon², and F. Jeffrey², ¹HP Labs, Palo Alto, California, USA and ²Phicot Inc., Palo Alto, California, USA
- VI.B-2 **Indium-free Transparent Thin Film Transistors Based on Nanocrystalline ZnO** G I
10:20 AM B. Bayraktaroglu¹, K. Leedy¹ and R. C. Scott², ¹Air Force Research Laboratory, Sensors Directorate, AFRL/RYYD, Wright Patterson AFB, Ohio, USA and ²Arizona State University, Tempe, Arizona, USA
- VI.B-3 **Circuit applications based on solution-processed zinc-tin oxide TFTs** G I
10:40 AM C.-G. Lee, T. Joshi, K. Divakar, and A. Dodabalapur, Microelectronics Research Center, University of Texas at Austin, Austin, Texas, USA
- VI.B-4 **Aluminum Top-Gate ZnO Nanowire Transistors with Improved Transconductance** G J
11:00 AM D. Kälblein¹, B. Fenk¹, K. Hahn², U. Zschieschang¹, K. Kern^{1,3}, H. Klauk¹, ¹Max Planck Institute for Solid State Research, Stuttgart, GERMANY, ²Max Planck Institute for Metals Research, GERMANY, and ³Ecole Polytechnique Fédérale de Lausanne, Lausanne, SWITZERLAND

Session VII.A Optoelectronic Devices

251-266

- VII.A-1 **Monolithic Integration of CMOS and Nanophotonic Devices for Massively Parallel Optical Interconnects in Supercomputers** G H
1:30 PM S. Assefa¹, W. M. J. Green¹, A. Rylyakov¹, C. Schow¹, F. Horst² and Y. A. Vlasov¹, ¹IBM Thomas J. Watson Research Center, Yorktown Heights, New York, USA and ²IBM Zurich GMBH, Rueshlikon, SWITZERLAND
- VII.A-2 **Electrical pumped integrated III/V laser lattice-matched to a Silicon substrate** G I
2:10 PM B. Kunert¹, S. Liebich², M. Zimprich², A. Beyer², S. Ziegler¹, K. Volz², W. Stolz², N. Hossain³, S. R. Jin³, and S. J. Sweeney³, ¹NAsP III/V GmbH, Marburg, GERMANY and ²Material Sciences Center and Faculty of Physics, Philipps-University Marburg, Marburg, GERMANY, and ³Advanced Technology Institute and Department of Physics, University of Surrey, Guildford, Surrey, UK
- VII.A-3 **Lateral Carrier Injection with n-type Modulation-doped Quantum Wells in VCSELs** G J
2:30 PM C.-H. Lin¹, Y. Zheng¹, M. Gross³, M. J. W. Rodwell¹, and L. A. Coldren^{1,2}, ¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA, ²Department of Materials, University of California, Santa Barbara, California, USA, and ³Ziva Corporation, San Diego, California, USA

- VII.A-4 **Near UV AlGaIn-Cladding Free Nonpolar InGaIn/GaN Laser Diodes 261**
 2:50 PM D. A. Haeger¹, C. Holder¹, R. M. Farrell¹, P. S. Hsu¹, K. M. Kelchner², K. Fujito³, D. A. Cohen², S. P. DenBaars^{1,2}, J. S. Speck¹, and S. Nakamura^{1,2}, ¹Materials Department, University of California, Santa Barbara, California, USA, ²Electrical and Computer Engineering Department, University of California, Santa Barbara, California, USA, and ³Optoelectronic Laboratory, Mitsubishi Chemical Corporation, Ushiku, Ibaraki, JAPAN
- VII.A-5 **RIE Lag Directional Coupler based Integrated InGaAsP/InP Ring Mode-locked Laser 263**
 3:30 PM J. S. Parker¹, P. R. A. Binetti¹, Y.-J. Hung², Erik J. Norberg¹, and L. A. Coldren¹, ¹Electrical and Computer Engineering Department, University of California, Santa Barbara, California, USA and ²Dept. of Electronic Engineering, National Taiwan University of Science and Technology, Taipei, TAIWAN
- VII.A-6 **Integrated Non-III-Nitride/III-Nitride Tandem Solar Cell 265**
 3:50 PM N. G. Toledo¹, S. C. Cruz², C. J. Neufeld¹, M. A. Scarpulla², T. Buehl², A. C. Gossard^{1,2}, S. P. Denbaars^{1,2}, J. S. Speck² and U. K. Mishra¹, ¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, and ²Materials Department, University of California, Santa Barbara, California, USA

Session VII.B High Speed Devices

267-282

- VII.B-1 **N-polar GaN HEMTs with $f_{\max} > 300$ GHz using high-aspect-ratio T-gate design 269**
 1:30 PM D.J. Denninghoff¹, S. Dasgupta¹, D.F. Brown³, S. Keller¹, J. Speck², and U.K. Mishra¹, ¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA, ²Department of Materials, University of California, Santa Barbara, California, USA, and ³HRL, Malibu, California, USA
- VII.B-2 **1.0 THz f_{\max} InP DHBTs in a refractory emitter and self-aligned base process for reduced base access resistance 271**
 1:50 PM V. Jain¹, J. C. Rode¹, H.-W. Chiang¹, A. Baraskar¹, E. Lobisser¹, B. J. Thibeault¹, M. Rodwell¹, M. Urteaga², D. Loubychev³, A. Snyder³, Y. Wu³, J. M. Fastenau³, W. K. Liu³, ¹ECE Department, University of California, Santa Barbara, California, USA, ²Teledyne Scientific & Imaging, Thousand Oaks, California, USA, and ³IQE Inc., Bethlehem, Pennsylvania, USA
- VII.B-3 **Effect of optical phonon scattering on the performance limits of ultrafast GaN transistors 273**
 2:10 PM T. Fang, R. Wang, G. Li, H. Xing, S. Rajan, and D. Jena, Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA
- VII.B-4 **Device Scaling Technologies for Ultra-High-Speed GaN-HEMTs 275**
 2:30 PM K. Shinohara¹, D. Regan¹, I. Milosavljevic¹, A. L. Corrion¹, D. F. Brown¹, S. Burnham¹, P. J. Willadsen¹, C. Butler¹, A. Schmitz¹, S. Kim¹, V. Lee², A. Ohoka², P. M. Asbeck², and M. Micovic¹, ¹HRL Laboratories LLC, California, USA, and ²Department Electrical and Computer Engineering, University of California, San Diego, California, USA
- VII.B-5 **Trap-related Delay analysis of self-aligned N-polar GaN/InAlN HEMTs with record extrinsic g_m of 1105 mS/mm 279**
 3:30 PM Nidhi, S. Dasgupta, J. Lu, F. Wu, S. Keller, J. S. Speck and U. K. Mishra, ECE Department, University of California Santa Barbara, Santa Barbara, California, USA

VII.B-6
3:50 PM

130nm InP DHBTs with $f_t > 0.52\text{THz}$ and $f_{max} > 1.1\text{THz}$ 281

M. Urteaga¹, R. Pierson¹, P. Rowell¹, V. Jain², E. Lobisser², M.J.W. Rodwell², ¹Teledyne Scientific Company, Thousand Oaks, California, USA and ²Department of ECE, University of California, Santa Barbara, California, USA