

2011 Symposium on VLSI Circuits

(VLSIC 2011)

**Kyoto, Japan
15 – 17 June 2011**



**IEEE Catalog Number: CFP11VLS-PRT
ISBN: 978-1-61284-175-5**

TABLE OF CONTENTS

SESSION 1 - Welcome and Plenary Session I [Suzaku I, II]

Wednesday, June 15, 8:30

Chairpersons: M. Nagata, Kobe Univ.
V. De, Intel Corp.

1-1 - 8:30

Welcome and Opening Remarks

M. Mizuno, Renesas Electronics Corp.
A. Amerasekera, Texas Instruments, Inc.

1-2 - 8:45

(Invited)

The Hayabusa Mission - Its Seven Years Flight, J. Kawaguchi, Japan Aerospace Exploration Agency (JAXA), Japan

2

1-3 - 9:25

(Invited)

The Swarm at the Edge of the Cloud - A New Perspective on Wireless, J.M. Rabaey, University of California at Berkeley, USA

6

SESSION 2 - Switching DC-DC Converters [Suzaku I]

Wednesday, June 15, 10:30

Chairpersons: C. Yoo, Hanyang Univ.
U.-K. Moon, Oregon State Univ.

2-1 - 10:30

A 50.3ns Transient-Response CR-Free SIMO Power Converter with Adaptive Current Compensation, Y. Zhang and D. Ma, The University of Texas at Dallas, USA

10

2-2 - 10:55

A 98% Cross-Talk Self-Cancellation Single-Inductor Dual-Output DC-DC Converter Using Bidirectional Power Prediction (BPP) Control in 65nm CMOS, Y.-H. Lee*, Y.-Y. Yang*, T.-C. Huang*, C.-Y. Hsieh*, K.-H. Chen*, Y.-K. Chen**, C.-C. Huang** and Y.-H. Lin**, *National Chiao Tung University and **Realtek Semiconductor Corp., Taiwan

12

2-3 - 11:20

A Single-Inductor 8-Channel Output DC-DC Boost Converter with Time-Limited One-Shot Current Control and Single Shared Hysteresis Comparator, J. Kim, D. S. Kim and C. Kim, Korea University, Korea

14

2-4 - 11:45

Fixed-Frequency Adaptive-On-Time Boost Converter with Fast Transient Response and Light Load Efficiency Enhancement by Auto-Frequency-Hopping, X. Jing and P.K.T. Mok, The Hong Kong University of Science and Technology, China

16

2-5 - 12:10

A Spurious-Free Switching Buck Converter Using a Delta-Sigma Modulation Controller with a Scalable Sampling Frequency, M.K. Alghamdi and A.A. Hamoui, McGill University, Canada

18

SESSION 3 - Advanced Wireless Transceivers [Suzaku II]

Wednesday, June 15, 10:30

Chairpersons: H. Ishikuro, Keio Univ.
A. Cathelin, STMicroelectronics

3-1 - 10:30

A 0.38THz Fully Integrated Transceiver Utilizing Quadrature Push-Push Circuitry, J.-D. Park, S. Kang and A.M. Niknejad, University of California, Berkeley, USA

22

3-2 - 10:55

A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS, C. Thakkar*, L. Kong*, K. Jung*, A. Frappé** and E. Alon*, *University of California, Berkeley, USA and **Institut Supérieur de l'Electronique et du Numérique, France

24

3-3 - 11:20

A 2.5GHz Delay-Based Wideband OFDM Outphasing Modulator in 45nm-LP CMOS, A. Ravi, P. Madoglio, M. Verhelst, M. Sajadieh, M. Aguirre, H. Xu, S. Pellerano, I. Lomeli, J. Zarate, L. Cuellar, O. Degani, H. Lakdawala, K. Soumyanath and Y. Palaskas, Intel Corp., USA

26

3-4 - 11:45

A Configurable Multi-Band Multi-Mode Transmitter with Spur Cancellation Through Digital Baseband, Y. Tang, M. Chen, W. Leung, C. Narathong, M. Ranjan, K. Godbole, G. Zhang, O. Choksi, V. Panikkath, C. Hostenstein, A. Hadjichristos and K. Sahota, Qualcomm, USA

28

3-5 - 12:10

A 3.5mm², Inductor-Less Digital-Intensive Radio SoC for 300-to-950MHz ISM-Band Applications Supporting 1.0-to-240kbps Multi-Data-Rates, T. Tokairin*, H. Saito**, H. Ishizaki*, Y. Oka*, T. Maeda*, S. Oshima**, M. Soda*, M. Okada*, S. Hori***, M. Kitsunezuka*** and M. Mizuno*, *Renesas Electronics Corporation, **Renesas Micro Systems Co., Ltd. and ***NEC Corporation, Japan

30

SESSION 4 - Oversampling Converters [Suzaku III]

Wednesday, June 15, 10:30

Chairpersons: M. Ito, Renesas Electronics Corp.
J. Lloyd, Analog Devices, Inc.

4-1 - 10:30

A 12-ENOB 6X-OSR Noise-Shaped Pipelined ADC Utilizing a 9-bit Linear Front-End, O. Rajaei** and U. Moon*, *Oregon State University and **Qualcomm, USA

34

4-2 - 10:55

A 32nm, 1.05V, BIST Enabled, 10-40MHz, 11-9 Bit, 0.13mm² Digitized Integrator MASH $\Delta\Sigma$ ADC, B. R. Carlton, H. Lakdawala, E. Alpman, J. Rizk, Y.W. Li, B. Perez-Esparza, V. Rivera, C.F. Nieva, E. Gordon, P. Hackney, C.-H. Jan, I.A. Young and K. Soumyanath, Intel Corporation, USA

36

4-3 - 11:20

A Continuous-Time, Jitter Insensitive $\Sigma\Delta$ Modulator Using a Digitally Linearized G_m -C Integrator with Embedded SC Feedback DAC, D. Kim*, T. Matsuura** and B. Murmann*, *Stanford University, USA and **Renesas Electronics Corp., Japan

38

4-4 - 11:45

A 48-dB DR 80-MHz BW 8.88-GS/s Bandpass $\Delta\Sigma$ ADC for RF Digitization with Integrated PLL and Polyphase Decimation Filter in 40nm CMOS, E. Martens, A. Bourdoux, A. Couvreur, P. Van Wesemael, G. Van der Plas, J. Craninckx and J. Ryckaert, IMEC, Belgium

40

4-5 - 12:10

A 2.8 mW $\Delta\Sigma$ ADC with 83 dB DR and 1.92 MHz BW Using FIR Outer Feedback and TIA-Based Integrator, J. Gealow*, M. Ashburn*, C.-H. Lou*, S. Ho*, P. Riehl*, A. Shabra**, J. Silva* and Q. Yu*, *MediaTek Wireless, Inc., USA and **Masdar Institute of Science and Technology, UAE

42

SESSION 5 - Circuit and System Integration [Suzaku I]

Wednesday, June 15, 13:55

Chairpersons: C. Hou, TSMC
J. Barth, IBM Microelectronics**5-1 - 13:55****Measurement, Analysis and Improvement of Supply Noise in 3D ICs**, P. Jain, D. Jiao, X. Wang and C.H. Kim, University of Minnesota, USA

46

5-2 - 14:20**Isolation Techniques Against Substrate Noise Coupling Utilizing Through Silicon Via (TSV) for RF/Mixed-Signal SoCs**, S. Uemura, Y. Hiraoka, T. Kai and S. Doshu, Panasonic Corp., Japan

48

5-3 - 14:45**A Fully-Integrated Cantilever-Based DNA Detection SoC in a CMOS Bio-MEMS Process**, Y.-J. Huang*, C.-W. Huang*, T.-H. Lin*, C.-T. Lin*, L.-G. Chen*, P.-Y. Hsiao*, B.-R. Wu*, H.-T. Hsueh*, B.-J. Kuo*, H.-H. Tsai**, H.-H. Liao**, Y.-Z. Juang**, C.-K. Wang* and S.-S. Lu*, *National Taiwan University and **National Applied Research Laboratories, Taiwan

50

5-4 - 15:10**A 65nm CMOS Movable Parts Manager for Optical Disc System**, F. Senoue*, K. Okamoto*, S. Sakiyama*, T. Morie*, S. Doshu*, H. Nishino**, K. Tanimoto**, A. Kawabe** and H. Kobayashi**, *Panasonic Corporation and **Panasonic Corporation Semiconductor Company Corporate, Japan

52

5-5 - 15:35**20- μ W Operation of an a-IGZO TFT-Based RFID Chip Using Purely NMOS "Active" Load Logic Gates with Ultra-Low-Consumption Power**, H. Ozaki, T. Kawamura, H. Wakana, T. Yamazoe and H. Uchiyama, Hitachi, Ltd., Japan

54

SESSION 6 - High Performance DACs and Amplifiers [Suzaku III]

Wednesday, June 15, 13:55

Chairpersons: J. Lee, National Taiwan Univ.
M. Flynn, Univ. of Michigan**6-1 - 13:55****A 100dB DR Ground-Referenced Single-Ended Class-D Amplifier in 65nm CMOS**, X. Jiang, J. Song, M. Wang, J. Chen, H. Zheng, S. Galal, K. Abdelfattah and T.L. Brooks, Broadcom Corporation, USA

58

6-2 - 14:20**A Ping-Pong-Pang Current-Feedback Instrumentation Amplifier with 0.04% Gain Error**, S. Sakunia*, F. Witte**, M. Pertijs* and K. Makinwa*, *Delft University of Technology and **National Semiconductor, The Netherlands

60

6-3 - 14:45**A 7.2-GSa/s, 14-bit or 12-GSa/s, 12-bit DAC in a 165-GHz f_T BiCMOS Process**, K. Poulton, B. Jewett and J. Liu, Agilent Technologies, USA

62

6-4 - 15:10**A 3GS/s, 9b, 1.2V Single Supply, Pure Binary DAC with >50dB SFDR up to 1.5GHz in 65nm CMOS**, S.L. Tual*, P.N. Singh****, A. Bal** and C. Garnier*, *STMicroelectronics Crolles, France, **STMicroelectronics G. Noida, India and ***Wolfson Microelectronics Edinburgh, UK

64

6-5 - 15:35**A 10b 600MS/s Multi-Mode CMOS DAC for Multiple Nyquist Zone Operation**, S.Y.-S. Chen, N.-S. Kim and J. Rabaey, University of California, Berkeley, USA

66

SESSION 7 - Embedded SRAM and Applications [Suzaku I]

Wednesday, June 15, 16:10

Chairpersons: M. Yamaoka, Hitachi America, Ltd.
M. Clinton, Texas Instruments, Inc.**7-1 - 16:10****A 40nm Fully Functional SRAM with BL Swing and WL Pulse Measurement Scheme for Eliminating a Need for Additional Sensing Tolerance Margins**, Y.-H. Chen***, S.-Y. Chou*, Q. Lee*, W.-M. Chan*, D. Sun*, H.-J. Liao*, P. Wang*, M.-F. Chang** and H. Yamauchi***, *TSMC, **National Tsing Hua University, Taiwan and ***Fukuoka Institute of Technology, Japan

70

7-2 - 16:35**A 40-nm 0.5-V 20.1- μ W/MHz 8T SRAM with Low-Energy Disturb Mitigation Scheme**, S. Yoshimoto*, M. Terada*, S. Okumura*, T. Suzuki**, S. Miyano**, H. Kawaguchi* and M. Yoshimoto*, *Kobe University and **Semiconductor Technology Academic Research Center (STARC), Japan

72

7-3 - 17:00**A Larger Stacked Layer Number Scalable TSV-Based 3D-SRAM for High-Performance Universal-Memory-Capacity 3D-IC Platforms**, M.-F. Chang*, W.-C. Wu*, C.-S. Lin**, P.-F. Chiu**, M.-B. Chen***, Y.-H. Chen****, H.-C. Lai**, Z.-H. Lin**, S.-S. Sheu**, T.-K. Ku** and H. Yamauchi****, *National Tsing Hua University, **ITRI, ***TSMC, Taiwan and ****Fukuoka Institute of Technology, Japan

74

7-4 - 17:25**A Chip-ID Generating Circuit for Dependable LSI Using Random Address Errors on Embedded SRAM and On-Chip Memory BIST**, H. Fujiwara, M. Yabuuchi, H. Nakano, H. Kawai, K. Nii and K. Arimoto, Renesas Electronics Corporation, Japan

76

SESSION 8 - Multi Gigabit Wireline Communication [Suzaku II]

Wednesday, June 15, 16:10

Chairpersons: K. Sunaga, NEC Corp.
T. C. Carusone, Univ. of Toronto**8-1 - 16:10****An 8x10-Gb/s Source-Synchronous I/O System Based on High-Density Silicon Carrier Interconnects**, T.O. Dickson, Y. Liu, S.V. Rylov, B. Dang, C.K. Tsang, P.S. Andry, J.F. Bulzacchelli, H.A. Ainspan, X. Gu, L. Turlapati, M.P. Beakes, B.D. Parker, J.U. Knickerbocker and D.J. Friedman, IBM T. J. Watson Research Center, USA

80

8-2 - 16:35**A 5.6Gb/s 2.4mW/Gb/s Bidirectional Link With 8ns Power-On**, J. Zerbe*, B. Daly*, W. Dettloff*, T. Stone*, W. Stonecypher*, P. Venkatesan*, K. Prabhu*, B. Su*, J. Ren*, B. Tsang*, B. Leibowitz*, D. Dunwell**, A.C. Carusone** and J. Eble*, *Rambus Inc, USA and **University of Toronto, Canada

82

8-3 - 17:00**An 8Gb/s Forwarded-Clock I/O Receiver with up to 1GHz Constant Jitter Tracking Bandwidth Using a Weak Injection-Locked Oscillator in 0.13 μ m CMOS**, S.-H. Chung*, L.-S. Kim*, S.-J. Bae**, K.-S. Ha**, J.-B. Lee** and J.S. Choi**, *KAIST and **Samsung Electronics, Korea

84

8-4 - 17:25**A 0.12mm² 5Gbps Receiver with a Level Shifting Equalizer and a Cumulative-Histogram-Based Adaptation Engine**, Y. Tomita*, H. Yamaguchi*, S. Kawahara**, T. Higuchi**, T. Yamamoto*, H. Ishida***, K. Gotoh*** and H. Tamura*, *Fujitsu Laboratories LTD., **Fujitsu LSI Solutions LTD. and ***Fujitsu Semiconductor LTD., Japan

86

SESSION 9 - Image Sensors [Suzaku III]

Wednesday, June 15, 16:10

Chairpersons: Y. Kato, Panasonic Corp.
M. Whatley, Cypress Semiconductor**9-1 - 16:10****A Digital CDS Scheme on Fully Column-Inline TDC Architecture for An APS-C Format CMOS Image Sensor**, T. Takahashi*, H. Ui*, N. Takatori**, S. Sanada**, T. Hamamoto**, H. Nakayama**, Y. Moriyama*, M. Akahide*, T. Ueno* and N. Fukushima*, *Sony Corporation and **Sony LSI Design Incorporated, Japan

90

9-2 - 16:35**A 640x480 Image Sensor with Unified Pixel Architecture for 2D/3D Imaging in 0.11µm CMOS**, S.-J. Kim, J.D.K. Kim, S.-W. Han, B. Kang, K. Lee and C.-Y. Kim, Samsung Advanced Institute of Technology, Korea

92

9-3 - 17:00**A Dual In-Pixel Memory CMOS Image Sensor for Computation Photography**, G. Wan***, X. Li*, G. Agranov*, M. Levoy** and M. Horowitz**, *Aptina, LLC and **Stanford University, USA

94

9-4 - 17:25**A CMOS Σ-Δ Photodetector Array for Bioluminescence-Based DNA Sequencing**, R.R. Singh, B. Li, A. Elligton and A. Hassibi, University of Texas at Austin, USA

96

SESSION10 - Plenary Session II [Suzaku I, II]

Thursday, June 16, 8:45

Chairpersons: M. Nagata, Kobe Univ.
V. De, Intel Corp.**10-1 - 8:45**

(Invited)

Circuit Challenges for Future Computing Systems, W. J. Dally, NVIDIA and Stanford University, USA

100

10-2 - 9:25

(Invited)

Smart Devices and Services in Healthcare and Wellness, H. Nakajima* and T. Shiga**, *Omron Corporation and **Omron Healthcare Co., Ltd., Japan

104

SESSION 11 - Fractional-N PLLs [Suzaku I]

Thursday, June 16, 10:30

Chairpersons: S.H. Cho, KAIST
N. Kurd, Intel Corp.**11-1 - 10:30****A Low Spur Fractional-N Digital PLL for 802.11 a/b/g/n/ac with 0.19 ps_{rms} Jitter**, C.-W. Yao, L. Lin, B. Nissim, H. Arora and T. Cho, Marvell Semiconductor, Inc. USA

110

11-2 - 10:55**A -104dBc/Hz In-Band Phase Noise 3GHz All Digital PLL with Phase Interpolation Based Hierarchical Time to Digital Converter**, D. Miyashita, H. Kobayashi, J. Deguchi, S. Kousai and M. Hamada, Toshiba Corporation, Japan

112

11-3 - 11:20**A 3.6GHz 1MHz-Bandwidth ΔΣ Fractional-N PLL with a Quantization-Noise Shifting Architecture in 0.18µm CMOS**, W.-H. Chiu and T.-H. Lin, National Taiwan University, Taiwan

114

11-4 - 11:45**A 2 GHz Fractional-N Digital PLL with 1b Noise Shaping ΔΣ TDC**, D.-W. Jee, Y.-H. Seo, H.-J. Park and J.-Y. Sim, Pohang University of Science and Technology, Korea

116

SESSION 12 - Pipelined ADCs [Suzaku III]

Thursday, June 16, 10:30

Chairpersons: S. Dosho, Panasonic Corp.
C.-M. Hung, MStar Semiconductor, Inc.**12-1 - 10:30****A 12b 3GS/s Pipeline ADC with 500mW and 0.4 mm² in 40nm Digital CMOS**, C.-Y. Chen and J. Wu, Broadcom Corporation, USA

120

12-2 - 10:55**An 11b 300MS/s 0.24pJ/Conversion-Step Double-Sampling Pipelined ADC with On-Chip Full Digital Calibration for All Nonidealities Including Memory Effects**, T. Miki, T. Morie, T. Ozeki and S. Dosho, Panasonic Corporation, Japan

122

12-3 - 11:20**A 22-mW 7b 1.3-GS/s Pipeline ADC with 1-Bit/Stage Folding Converter Architecture**, T. Yamase*, H. Uchida** and H. Noguchi*, *NEC Corporation and **NEC Engineering, Ltd., Japan

124

12-4 - 11:45**A 10b 320 MS/s 40 mW Open-Loop Interpolated Pipeline ADC**, M. Miyahara, H. Lee, D. Paik and A. Matsuzawa, Tokyo Institute of Technology, Japan

126

12-5 - 12:10**A 16-mW 8-Bit 1-GS/s Subranging ADC in 55nm CMOS**, Y.-H. Chung*** and J.-T. Wu*, *National Chiao-Tung University and **MediaTek Inc., Taiwan

128

Luncheon Talk [Suzaku II]

Thursday, June 16, 12:45-14:05

Organizer: K. Kobayashi, Kyoto Institute of Technology

Recent Studies about Computer Aided Origami Design, J. Mitani, Univ. of Tsukuba**SESSION 13 - High Speed Digital for Interconnects [Suzaku I]**

Thursday, June 16, 14:20

Chairpersons: M. Igarashi, Sony Corp.
C. Sechen, Univ. of Texas at Dallas**13-1 - 14:20****The 10G-EPON OLT and ONU LSIs for the Coexistence of 10G-EPON and GE-PON toward the Next FTTH Era**, M. Urano, T. Kawamura, S. Ohteru, H. Suto, K. Kawai, R. Kusaba, N. Miura, J. Kato, A. Miyazaki, T. Hatano, S. Yasuda, N. Tanaka, S. Shigematsu, M. Nakanishi and T. Shibata, NTT Microsystem Integration Laboratories, Japan

132

13-2 - 14:45**A 2.37Gb/s 284.8mW Rate-Compatible (491,3,6) LDPC-CC Decoder**, C.-L. Chen, Y.-H. Lin, H.-C. Chang and C.-Y. Lee, National Chiao Tung University, Taiwan

134

13-3 - 15:10**A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric**, C.C. Wang, F.-L. Yuan, H. Chen and D. Marković, University of California, Los Angeles, USA

136

13-4 - 15:35**SWIFT: A 2.1Tb/s 32x32 Self-Arbitrating Manycore Interconnect Fabric**, S. Satpathy, R. Dreslinski, T.-C. Ou, D. Sylvester, T. Mudge and D. Blaauw, University of Michigan, USA

138

SESSION 14 - Bio Interfaces [Suzaku III]

Thursday, June 16, 14:20

Chairpersons: C.-Y. Lee, National Chiao Tung Univ.
K. Chang, Xilinx**14-1 - 14:20****A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications**, H. Kim*, R.F. Yazicioglu*, S. Kim*, N. Van Helleputte*, A. Artes**, M. Konijnenburg**, J. Huiskens**, J. Penders** and C. Van Hoof***, *imec, Belgium and **imec-nl/Holst center, The Netherlands

142

14-2 - 14:45 A 96-Channel Full Data Rate Direct Neural Interface in 0.13μm CMOS , R.M. Walker*, H. Gao*, P. Nuyujukian*, K. Makinwa**, K.V. Shenoy*, T. Meng* and B. Murmann*, *Stanford University, USA and **Delft University of Technology, The Netherlands	144
14-3 - 15:10 BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication , S.-I. Chang, K. AlAshmouny, M. McCormick, Y.-C. Chen and E. Yoon, University of Michigan, USA	146
14-4 - 15:35 A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor , S. Ayazian*, E. Soenen** and A. Hassibi*, *University of Texas at Austin and **Taiwan Semiconductor Manufacturing Company, USA	148
Session 15 - Clocking Building Blocks [Suzaku I] Thursday, June 16, 16:15 Chairpersons: H.-J. Park, Pohang Univ. of Science and Technology (POSTECH) J. Tierno, IBM TJ Watson Research Center	148
15-1 - 16:15 A 0.63ps Resolution, 11b Pipeline TDC in 0.13μm CMOS , Y.-H. Seo, J.-S. Kim, H.-J. Park and J.-Y. Sim, Pohang University of Science and Technology, Korea	152
15-2 - 16:40 553-GHz Signal Generation in CMOS Using a Quadruple-Push Oscillator , D. Shim*, D. Koukis*, D.J. Arenas*, D.B. Tanner* and Kenneth K. O.**, *University of Florida and **University of Texas at Dallas, USA	154
15-3 - 17:05 High-PSRR All-Digital Delay Locked Loop with Burst Update Mode and Power Noise Damping Scheme , Y. Kim, J. Jang, J. Moon, S. Lee, D. Kwon, H. Choi, G. Park and B. Chung, Hynix Semiconductor, Korea	156
15-4 - 17:30 A Programmable MEMS-Based Clock Generator with Sub-ps Jitter Performance , F.S. Lee*, J. Salvia*, C. Lee**, S. Mukherjee*, R. Melamud*, N. Arumugam*, S. Pamarti***, C. Arft*, P. Gupta*, S. Tabatabaei*, B. Garlepp**, H.-C. Lee*, A. Partridge*, M.H. Perrott**** and F. Assaderaghi*, *SiTime, **Silicon Laboratories, ***UCLA, USA and ****Masdar Institute, UAE	158
Session 16 - Ultra Low Power Transceivers [Suzaku II] Thursday, June 16, 16:15 Chairpersons: K. Agawa, Toshiba Corp. J. Savoj, Xilinx	158
16-1 - 16:15 A Battery-Less WiFi-BER Modulated Data Transmitter with Ambient Radio-Wave Energy Harvesting , H. Ikeda*, Y. Yoshida**, T. Maeda*, T. Kuroda** and M. Mizuno*, *Renesas Electronics Corporation and **Keio University, Japan	162
16-2 - 16:40 315MHz Energy-Efficient Injection-Locked OOK Transmitter and 8.4μW Power-Gated Receiver Front-End for Wireless Ad Hoc Network in 40nm CMOS , L. Liu, T. Sakurai and M. Takamiya, The University of Tokyo, Japan	164
16-3 - 17:05 A 550μW Inductorless Bandpass Quantizer in 65nm CMOS for 1.4-to-3GHz Digital RF Receivers , D. Lachartre, CEA, LETI, France	166
16-4 - 17:30 A 1mm³ 2Mbps 330fJ/b Transponder for Implanted Neural Sensors , M. Mark, Y. Chen, C. Sutardja, C. Tang, S. Gowda, M. Wagner, D. Werthimer and J. Rabaey, University of California, Berkeley, USA	168
SESSION 17 - Bio Sensors and Applications [Suzaku III] Thursday, June 16, 16:15 Chairpersons: M. Ikeda, The Univ. of Tokyo B. Nauta, Univ. of Twente	168
17-1 - 16:15 A 0.5-V Sub-mW Wireless Magnetic Tracking Transponder for Radiation Therapy , W.-F. Loke*, W.-H. Chen*, T. Maleki*, M.A. Khater*, B. Ziaie*, L. Papiez** and B. Jung*, *Purdue University and **UT Southwestern Medical School, USA	172
17-2 - 16:40 A 256 Channel Magneto-resistive Biosensor Microarray for Quantitative Proteomics , D.A. Hall*, R.S. Gaster*, S.J. Osterfeld*, K. Makinwa**, S.X. Wang* and B. Murmann*, *Stanford University, USA and **Delft University of Technology, The Netherlands	174
17-3 - 17:05 Magnetic Relaxation Detector for Microbead Labels in Biomedical Assays , P. Liu, K. Skucha, Y. Duan, M. Megens, J. Kim, I. Izyumin, S. Gambini and B. Boser, UC Berkeley, USA	176
17-4 - 17:30 Low Power Control IC for Efficient High-Voltage Piezoelectric Driving in a Flying Robotic Insect , M. Karpelson, R.J. Wood and G.-Y. Wei, Harvard University, USA	178
RUMP SESSIONS Thursday, June 16, 20:00-22:00	
R-1: Special Evening Session : NVM Technology and New Application Opportunities [Suzaku I, II] Organizers: H. Yamauchi, Fukuoka Institute of Technology M. Bauer, Micron Technology, Inc. Moderator: M. Bauer, Micron Technology, Inc.	182
R-2: Will Circuit Design be a Key Issue in Biomedical Applications? (or Boring Circuits?) [Suzaku III] Organizers: A. Cathelin, STMicroelectronics M. Takamiya, The Univ. of Tokyo Moderator: A. Cathelin, STMicroelectronics	182
Joint Rump Session with Technology Tuesday, June 14, 20:00-22:00 Organizers: K. Nose, Renesas Electronics Corp. K. Chang, Xilinx	
J-R: Low Voltage - How Low Can We Go with Technology and Design Solutions? [Suzaku I, II] Organizers: Technology N. Kasai, Tohoku Univ. T. Skotnicki, STMicroelectronics Circuits S. Doshio, Panasonic Corp. M. Clinton, Texas Instruments, Inc. Moderators: K. Ishimaru, Toshiba Corp. K. Zhang, Intel Corp.	183

SESSION 18 - High Performance Circuit Techniques [Suzaku I]

Friday, June 17, 8:30

Chairpersons: H. Kabuo, Panasonic Corp.
J. Chang, TSMC**18-1 - 8:30****A 27% Active-Power-Reduced 40-nm CMOS Multimedia SoC with Adaptive Voltage Scaling Using Distributed Universal Delay Lines**, Y. Ikenaga*, M. Nomura*, S. Suenaga*, H. Sonohara*, Y. Horikoshi*, T. Saito*, Y. Ohdaira**, Y. Nishio***, T. Iwashita**, M. Satou**, K. Nishida*, K. Nose*, K. Noguchi*, Y. Hayashi* and M. Mizuno*, *Renesas Electronics Corporation, **Renesas Mobile Corporation and ***Renesas Micro Systems Co., Ltd., Japan

186

18-2 - 8:55**LC²: Limited Contention Level Converter for Robust Wide-Range Voltage Conversion**, Y. Kim, D. Sylvester and D. Blaauw, University of Michigan, USA

188

18-3 - 9:20**Adaptive Robustness Tuning for High Performance Domino Logic**, B. Giridhar*, D. Fick*, M. Fojtik*, S. Satpathy*, D. Bull**, D. Sylvester* and D. Blaauw*, *University of Michigan, USA and **ARM, UK

190

18-4 - 9:45**A 381 fs/bit, 51.7 nW/bit Nearest Hamming-Distance Search Circuit in 65 nm CMOS**, H.J. Mattausch, M. Yasuda, A. Kawabata, W. Imafuku and T. Koide, Hiroshima University, Japan

192

SESSION 19 - Nonvolatile Memories [Suzaku II]

Friday, June 17, 8:30

Chairpersons: K. Kajigaya, Elpida Memory, Inc.
M. Bauer, Micron Technology, Inc.**19-1 - 8:30****A 21nm High Performance 64Gb MLC NAND Flash Memory with 400MB/s Asynchronous Toggle DDR Interface**, C. Kim, J. Ryu, T. Lee, H. Kim, J. Lim, J. Jeong, S. Seo, H. Jeon, B. Kim, I. Lee, D. Lee, P. Kwak, S. Cho, Y. Yim, C. Cho, W. Jeong, J.-M. Han, D. Song, K. Kyung, Y.-H. Lim and Y.-H. Jun, Samsung Electronics, Korea

196

19-2 - 8:55**A Fast Rewritable 90nm 512Mb NOR "B4-Flash" Memory with 8F² Cell Size**, T. Ogura, M. Mihara, Y. Kawajiri, K. Kobayashi, T. Sakaniwa, K. Nishikawa, S. Shimizu, S. Shukuri, N. Ajika and M. Nakashima, GENUSION, Inc., Japan

198

19-3 - 9:20**4-Times Faster Rising V_{PASS}(10V), 15% Lower Power V_{PGM}(20V), Wide Output Voltage Range Voltage Generator System for 4-Times Faster 3D-Integrated Solid-State Drives**, T. Hatanaka and K. Takeuchi, The University of Tokyo, Japan

200

19-4 - 9:45**A 512Mb Phase-Change Memory (PCM) in 90nm CMOS Achieving 2b/cell**, G.F. Close*, U. Frey****, J. Morrish**, R. Jordan**, S. Lewis**, T. Maffitt**, M. Breitwisch***, C. Hagleitner*, C. Lam*** and E. Eleftheriou*, *IBM Research Zurich, Switzerland, **IBM Essex Junction, ***IBM T. J. Watson Research Center, USA and ****RIKEN, Japan

202

SESSION 20 - High Speed and Low Power Receiver Techniques [Suzaku III]

Friday, June 17, 8:30

Chairpersons: S. Mutoh, NTT Corp.
A. Emami, CalTech**20-1 - 8:30****A 20-Gb/s, 0.66-pJ/bit Serial Receiver with 2-Stage Continuous-Time Linear Equalizer and 1-Tap Decision Feedback Equalizer in 45nm SOI CMOS**, J.E. Proesel and T.O. Dickson, IBM T. J. Watson Research Center, USA

206

20-2 - 8:55**A 40Gb/s Adaptive Receiver with Linear Equalizer and Merged DFE/CDR**, C.-L. Hsieh and S.-I. Liu, National Taiwan University, Taiwan

208

20-3 - 9:20**A 2.6mW/Gbps 12.5Gbps RX with 8-Tap Switched-Cap DFE in 32nm CMOS**, T. Toifl*, C. Menolfi*, M. Ruegg**, R. Reutemann**, A. Prati**, D. Gardellini**, M. Brändli*, M. Kossel*, P. Buchmann*, P.A. Francese* and T. Morf*, *IBM Research GmbH and **Miromico, Switzerland

210

20-4 - 9:45**A 4.4uW Wake-Up Receiver Using Ultrasound Data Communications**, K. Yadav, I. Kymissis and P.R. Kinget, Columbia University, USA

212

SESSION 21 - Device-Based Circuit Techniques [Suzaku I]

Friday, June 17, 10:30

Chairpersons: K. Kobayashi, Kyoto Institute of Technology
G. Lehmann, Infineon Technologies AG**21-1 - 10:30****A True Random Number Generator Using Time-Dependent Dielectric Breakdown**, N. Liu, N. Pinckney, S. Hanson, D. Sylvester and D. Blaauw, University of Michigan, USA

216

21-2 - 10:55**On-Chip Combined C-V/I-V Transistor Characterization System in 45-nm CMOS**, S. Realov and K.L. Shepard, Columbia University, USA

218

21-3 - 11:20**Electrical Monitoring of Gate and Active Area Mask Misalignment Error**, A. Bansal*, A. Singhee*, E. Acar* and G. Costrini**, *IBM Thomas J. Watson Research Center and **IBM Systems & Technology Group, USA

220

21-4 - 11:45**A 80kS/s 36uW Resistor-Based Temperature Sensor Using BGR-Free SAR ADC with a Unevenly-Weighted Resistor String in 0.18um CMOS**, C.-K. Wu, W.-S. Chan and T.-H. Lin, National Taiwan University, Taiwan

222

21-5 - 12:10**PBTI/NBTI Monitoring Ring Oscillator Circuits with On-Chip V_t Characterization and High Frequency AC Stress Capability**, J.-J. Kim*, R.M. Rao*, J. Schaub**, A. Ghosh**, A. Bansal*, K. Zhao***, B.P. Linder* and J. Stathis*, *IBM T. J. Watson Research Center, **IBM Austin Research Lab and ***IBM SRDC, USA

224

SESSION 22 - DRAM and Memory Interfaces [Suzaku II]

Friday, June 17, 10:30

Chairpersons: R. Takemura, Hitachi, Ltd.
J. Zerbe, Rambus**22-1 - 10:30****3D Stackable 32nm High-K/Metal Gate SOI Embedded DRAM Prototype**, J. Golz, J. Safran, B. He, D. Leu, M. Yin, T. Weaver, A. Vehabovic, Y. Sun, A. Cestero, B. Himmel, G. Maier, C. Kothandaraman, D. Fainstein, J. Barth, N. Robson, T. Kirihata, K. Rim and S. Iyer, IBM Systems and Technology Group, USA

228

22-2 - 10:55**In-Substrate-Bitline Sense Amplifier with Array-Noise-Gating Scheme for Low-Noise 4F² DRAM Array Operable at 10-fF Cell Capacitance**, Y. Yanagawa, T. Sekiguchi, A. Kotabe, K. Ono and R. Takemura, Hitachi, Ltd., Japan

230

22-3 - 11:20

A 12.8-Gb/s/Link Tri-Modal Single-Ended Memory Interface for Graphics Applications, A. Amirkhany, J. Wei, N. Mishra, J. Shen, W. Beyene, T. Chin, C. Huang, V. Gadde, K. Kaviani, P. Le, Mahabaleshwara, C. Madden, S. Mukherjee, L. Raghavan, K. Saito, D. Secker, F. Shuaeb, S. Srinivas, T. Wu, C. Tran, A. Vaidyanathan, K. Vyas, M. Jain, K. Chang and C. Yuan, Rambus Inc., USA

22-4 - 11:45

A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface, K. Kaviani, T. Wu, A. Amirkhany, J. Wei, J. Shen, C. Chen, T. Chin, W. Beyene, D. Dressler, V. Gadde, C. Huang, P. Le, Mahabaleshwara, C. Madden, N. Mishra, L. Raghavan, K. Saito, D. Secker, X. Shi, F. Shuaeb, S. Srinivas, C. Tran, A. Vaidyanath, K. Vyas, M. Jain, K. Chang and C. Yuan, Rambus Inc., USA

SESSION 23 - Power Management for Energy Harvesting [Suzaku III]

Friday, June 17, 10:30

Chairpersons: M. Takamiya, The Univ. of Tokyo
B. Nikolic, Univ of California, Berkeley

23-1 - 10:30

Platform Architecture for Solar, Thermal and Vibration Energy Combining with MPPT and Single Inductor, S. Bandyopadhyay and A.P. Chandrakasan, Massachusetts Institute of Technology, USA

23-2 - 10:55

A Reconfigurable SITITO Boost/Buck Regulator with Sub-Threshold Cross-Regulation-Free Dual-Mode Control for Energy-Harvesting Applications, M. Du, H. Lee and J. Liu, University of Texas at Dallas, USA

23-3 - 11:20

A Battery-Free 225 nW Buck Converter for Wireless RF Energy Harvesting with Dynamic On/Off Time and Adaptive Phase Lead Control, C.-Y. Hsieh*, Y.-H. Lee*, Y.-Y. Yang*, T.-C. Huang*, K.-H. Chen*, C.-C. Huang** and Y.-H. Lin**, *National Chiao Tung University and **Realtek Semiconductor Corp., Taiwan

23-4 - 11:45

A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications, M. Lüders*, B. Eversmann**, J. Gerber**, K. Huber**, R. Kuhn**, D. Schmitt-Landsiedel* and R. Brederlow**, *Munich University of Technology and **Texas Instruments, Germany

23-5 - 12:10

A 13.56MHz CMOS Rectifier with Switched-Offset for Reversion Current Control, Y. Lu*, W.-H. Ki* and J. Yi**, *HKUST and **Texas Instruments, China

SESSION 24 - Digital Processors [Suzaku I]

Friday, June 17, 13:55

Chairpersons: H. Kabuo, Panasonic Corp.
K. Wilcox, AMD

24-1 - 13:55

A 45nm 48-Core IA Processor with Variation-Aware Scheduling and Optimal Core Mapping, S. Dighe*, S. Gupta**, V. De*, S. Vangal*, N. Borkar*, S. Borkar* and K. Roy**, *Intel Corporation and **Purdue University, USA

24-2 - 14:20

A 75µW, 16-Channel Neural Spike-Sorting Processor with Unsupervised Clustering, V. Karkare, S. Gibson, C.-H. Yang, H. Chen and D. Marković, University of California, Los Angeles, USA

24-3 - 14:45

A 7.4mW 200MS/s Wideband Spectrum Sensing Digital Baseband Processor for Cognitive Radios, T.-H. Yu, C.-H. Yang, D. Čabrić and D. Marković, University of California, Los Angeles, USA

24-4 - 15:10

Fully Integrated CMOS SoC for 3D Blu-Ray Player Applications, C.-C. Ju, T.-M. Liu, S.-H. Lin, C.-C. Yang, T.-H. Wei, H. Lin, C.C. Chiou, C. Tsai, T. Lin, R. Su, A. Lin, M.N. Tsou, J. Lee, S.H. Tai, C.-M. Wang, C.-C. Chen, H.-M. Lin, C.-Y. Cheng, F. Chiu, Y.-C. Chang, P.H. Liu, C.C. Yu, E. Tsai, Y.C. Fang, K. Peng, J.-B. Yang, D.-P. Liu, K.-H. Chen, B.-W. Hsieh, Y.-C. Lien, W.H. Tu, C.H. Chou, T.H. Kang, L.-C. Wang, T.C. Hsiao, V. Lin, H. Hsieh, C.-S. Wu and J. Chen, Mediatek Inc., Taiwan

24-5 - 15:35

A 52mW Full HD 160-Degree Object Viewpoint Recognition SoC with Visual Vocabulary Processor for Wearable Vision Applications, Y.-C. Su, K.-Y. Huang, T.-W. Chen, Y.-M. Tsai, S.-Y. Chien and L.-G. Chen, National Taiwan University, Taiwan

SESSION 25 - Emerging ADCs [Suzaku II]

Friday, June 17, 13:55

Chairpersons: M. Yoshioka, FUJITSU LABORATORIES LTD.
I. Fujimori, Broadcom Corp.

25-1 - 13:55

A 0.5V 1.1MS/sec 6.3fJ/conversion-step SAR-ADC with Tri-Level Comparator in 40nm CMOS, A. Shikata, R. Sekimoto, T. Kuroda and H. Ishikuro, Keio University, Japan

25-2 - 14:20

A 1-V, 8b, 40MS/s, 113µW Charge-Recycling SAR ADC with a 14µW Asynchronous Controller, J.-H. Tsai, Y.-J. Chen, M.-H. Shen and P.-C. Huang, National Tsing Hua University, Taiwan

25-3 - 14:45

Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells, S. Weaver*, B. Hershberg** and U.-K. Moon**, *Intel Corporation and **Oregon State University, USA

25-4 - 15:10

A Reconfigurable 1GSps to 250MSps, 7-bit to 9-bit Highly Time-Interleaved Counter ADC in 0.13µm CMOS, S. Danesh***, J. Hurwitz**, K. Findlater**, D. Renshaw* and R. Henderson*, *Edinburgh University and **Gigle Networks, UK

25-5 - 15:35

A 71dB SFDR Open Loop VCO-Based ADC Using 2-Level PWM Modulation, S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar and P.K. Hanumolu, Oregon State University Corvallis, USA

SESSION 26 - Power Management Technique [Suzaku III]

Friday, June 17, 13:55

Chairpersons: K. Nose, Renesas Electronics Corp.
G. Van der Plas, IMEC

26-1 - 13:55

Dual-Loop System of Distributed Microregulators with High DC Accuracy, Load Response Time Below 500ps, and 85mV Dropout Voltage, Z. Toprak-Deniz*, J. Bulzacchelli*, T. Rasmus**, J. Iadanza**, W. Bucossi**, S. Kim*, R. Blanco**, C. Cox**, M. Chhabra**, C. Leblanc**, C. Trudeau** and D. Friedman*, *IBM T. J. Watson Research Center and **IBM Systems and Technology Group, USA

232

234

238

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242

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258

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264

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268

270

274

26-2 - 14:20

MEMS-Switch-Based Power Management with Zero-Power Voltage Monitoring for Energy Accumulation Architecture on Dust-Size Wireless Sensor Nodes, T. Shimamura, M. Ugajin, K. Kuwabara, K. Takagahara, K. Suzuki, H. Morimura, M. Harada and S. Mutoh, NTT Microsystem Integration Laboratories, Japan

276

26-3 - 14:45

A 210 nW 29.3 ppm/°C 0.7 V Voltage Reference with a Temperature Range of -50 to 130°C in 0.13 μm CMOS, J. Lee and S.H. Cho, KAIST, Korea

278

26-4 - 15:10

A Voltage-Reference-Free Pulse Density Modulation (VRF-PDM) 1-V Input Switched-Capacitor 1/2 Voltage Converter with Output Voltage Trimming by Hot Carrier Injection and Periodic Activation Scheme, X. Zhang*, Y. Pu*, K. Ishida*, Y. Ryu**, Y. Okuma**, P.-H. Chen*, K. Watanabe**, T. Sakurai* and M. Takamiya*, *The University of Tokyo and **Semiconductor Technology Academic Research Center, Japan

280

26-5 - 15:35

A Fast-Transient DVS-Capable Switching Converter with ΔI_L-Emulated Hysteretic Control, H. Chen and D. Ma, The University of Texas at Dallas, USA

282

SESSION 27 - Signal Processing for Wireline [Suzaku I]

Friday, June 17, 16:15

Chairpersons: R. Kuppuswamy, Intel India
J. Gealow, MediaTek Wireless, Inc.

27-1 - 16:15

A Laser Ranging Radar Transceiver with Modulated Evaluation Clock in 65nm CMOS Technology, W.-L. Lee, K.-C. Wu, J.-Y. Jiang and J. Lee, National Taiwan University, Taiwan

286

27-2 - 16:40

10Gb/s Serial I/O Receiver Based on Variable Reference ADC, E.-H. Chen, R. Yousry, T. Ali and C.-K.K. Yang, University of California, Los Angeles, USA

288

27-3 - 17:05

10 Gbps, 530 fJ/b Optical Transceiver Circuits in 40 nm CMOS, F. Liu*, D. Patil***, J. Lexau*, P. Amberg*, M. Dayringer*, J. Gainsley*, H.F. Moghadam*, X. Zheng*, J.E. Cunningham*, A.V. Krishnamoorthy*, E. Alon** and R. Ho*, *Oracle Labs, **UC-Berkeley and ***Rambus, USA

290

27-4 - 17:30

A Direct Sampling Multi-Channel Receiver for DOCSIS 3.0 in 65nm CMOS, E. Janssen*, K. Doris*, A. Zanicopoulos*, G. van der Weide*, M. Vertregt*, O. Jamin**, F. Courtois**, N. Blard**, M. Kristen**, S. Bertrand**, F. Riviere**, F. Deforeit**, G. Blanc**, Y. Penning**, F. Lefebvre**, D. Viguier**, M. Dubois**, V. Vrignaud**, C. Cazettes**, L. Schaller** and G. Jenvrin**, *NXP Semiconductors Eindhoven, The Netherlands and **NXP Semiconductors Caen, France

292

SESSION 28 - Nonvolatile Memory Applications [Suzaku II]

Friday, June 17, 16:15

Chairpersons: H. Yamauchi, Fukuoka Institute of Technology
O. Jungroth, Intel Corp.

28-1 - 16:15

A 45nm 1Mb Embedded STT-MRAM with Design Techniques to Minimize Read-Disturbance, J.P. Kim, T. Kim, W. Hao, H.M. Rao, K. Lee, X. Zhu, X. Li, W. Hsu, S.H. Kang, N. Matt and N. Yu, Qualcomm Incorporated, USA

296

28-2 - 16:40

Fully Parallel 6T-2MTJ Nonvolatile TCAM with Single-Transistor-Based Self Match-Line Discharge Control, S. Matsunaga*, A. Katsumata*, M. Natsui*, S. Fukami**, T. Endoh*, H. Ohno* and T. Hanyu*, *Tohoku University and **NEC Corporation, Japan

298

28-3 - 17:05

A Content Addressable Memory Using Magnetic Domain Wall Motion Cells, R. Nebashi*, N. Sakimura*, Y. Tsuji*, S. Fukami*, H. Honjo*, S. Saito*, S. Miura*, N. Ishiwata*, K. Kinoshita*, T. Hanyu**, T. Endoh**, N. Kasai**, H. Ohno** and T. Sugibayashi*, *NEC Corporation and **Tohoku University, Japan

300

28-4 - 17:30

A Non-volatile Look-Up Table Design Using PCM (Phase-Change Memory) Cells, C.-Y. Wen*, J. Li**, S. Kim**, M. Breitwisch**, C. Lam**, J. Paramesh* and L.T. Pileggi*, *Carnegie Mellon University and **IBM T. J. Watson Research Center, USA

302

SPECIAL SESSION

Technology Highlights [Shunju I, II]

Wednesday, June 15, 13:55

Chairpersons: S. Takagi, The Univ. of Tokyo
R. Jammy, Sematech

T7-1 - 13:55

ETSOI CMOS for System-on-Chip Applications Featuring 22nm Gate Length, Sub-100nm Gate Pitch, and 0.08μm² SRAM Cell, K. Cheng*, A. Khakifirooz*, P. Kulkarni*, S. Ponoth*, B. Haran*, A. Kumar*****, T. Adam*, A. Reznicek*, N. Loubet**, H. He*, J. Kuss*, M. Wang*, T.M. Levin*, F. Monsieur**, Q. Liu**, R. Sreenivasan*, J. Cai*****, A. Kimball*, S. Mehta*, S. Luning***, Y. Zhu*****, Z. Zhu*****, T. Yamamoto****, A. Bryant*****, C.-H. Lin*****, S. Naczas*, H. Jagannathan*, L.F. Edge*, S. Allegret-Maret**, A. Dube*****, S. Kanakasabapathy*, S. Schmitz*, A. Inada****, S. Seo*, M. Raymond***, Z. Zhang*****, A. Yagishita*****, J. Demarest*, J. Li*, M. Hopstaken*****, N. Berliner*, A. Upham*, R. Johnson*, S. Holmes*, T. Standaert*, M. Smalley*, N. Zamdmer*****, Z. Ren*****, T. Wu*, H. Bu*, V. Paruchuri*, D. Sadana*****, V. Narayanan*****, W. Haensch*****, J. O'Neill*, T. Hook*, M. Khare* and B. Doris*, *IBM, **STMicroelectronics, ***GLOBALFOUNDRIES, ****Renesas, *****Toshiba Albany Nanotech, *****IBM T. J. Watson Research Center and *****IBM SRDC, USA

' \$*

T7-2 - 14:20

Comprehensive SRAM Design Methodology for RTN Reliability, K. Takeuchi, T. Nagumo and T. Hase, Renesas Electronics Corporation, Japan

' \$,

T7-3 - 14:45

Unified Understanding of V_{th} and I_d Variability in Tri-Gate Nanowire MOSFETs, M. Saitoh*, K. Ota*, C. Tanaka*, Y. Nakabayashi*, K. Uchida** and T. Numata*, *Toshiba Corp. and **Tokyo Institute of Technology, Japan

' %\$

T7-4 - 15:10

1ma/um-I_{ON} Strained SiGe_{45%}-IFQW pFETs with Raised and Embedded S/D, J. Mitard*, L. Witters*, G. Hellings*****, R. Krom***, J. Franco***, G. Eneman*****, A. Hikavy*, B. Vincent*, R. Loo*, P. Favia*, H. Dekkers*, E. Altamirano Sanchez*, A. Vanderheyden*, D. Vanhaeren*, P. Eyben*, S. Takeoka*****, S. Yamaguchi*****, M.J.H. Van Dal*****, W.-E. Wang*****, S.-H. Hong*****, W. Vandervorst***, K. De Meyer***, S. Biesemans*, P. Absil*, N. Horiguchi* and T. Hoffmann*, *IMEC, **KULeuven, ***FWO, ****IWT, *****assignee at imec, *****from Panasonic and *****Sony, Belgium

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