2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting

(BCTM 2011)

Atlanta, Georgia, USA
9-11 October 2011

IEEE Catalog Number: CFP11BIP-PRT
ISBN: 978-1-61284-165-6

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2. Microwave and mm-Wave Building Blocks

Room 236

Monday 10:25 AM **J. Rogers**
Session Chair: **H. Knapp**
Co-Chair:

(2.1) 10:25–10:50 AM **A +18dBm, 79-87.5GHz Bandwidth Power Amplifier in 0.13mm SiGe-BiCMOS (Student)** **p. 17**

Y. Zhao, J. R. Long, M. Spirito and A.B. Akhnoukh

A three-stage, 77/79GHz transformer-coupled differential power amplifier is implemented in 130nm SiGe-BiCMOS. Common-base stages maximize output voltage swing and power, while a cascode first stage enhances gain for greater power-added efficiency (PAE). A frequency-scalable, parasitic-compensated balun combines power from the output stages to the 50Ω load with <1.2dB loss and 70x70mm^2 area on-chip. The measured peak small-signal gain is 27dB at 83GHz, and -3dB bandwidth is >8GHz. Maximum output power and peak-PAE are 18dBm and 9%, respectively, at 84GHz. The 0.23mm2 active area PA consumes 395mW from a 2.5V supply.

(2.2) 10:50–11:15 AM **A Fractional-N Synthesizer for Software-Defined Radio with Reduced Level of Spurious Tones (Student)** **p. 21**

S.A. Osmany, F. Herzel and J.C. Scheytt

We present an integrated fractional-N frequency synthesizer providing in-phase/quadrature phase signal over the frequency bands 0.6-4.6 GHz, 5-7 GHz, 10-14 GHz, and in-phase signal over 20-28 GHz for software-defined radio applications. The use of two parallel charge pumps for VCO tuning results in a fairly constant in-band phase noise over a wide range. Phase noise in fractional mode is -100 dBc/Hz and -122 dBc/Hz at 10 kHz and 1 MHz offset, respectively, for an output frequency of 3.644 GHz. The near-integer spurs related to the substrate modulation by the VCO were reduced to below -60 dBc by shielding the reference input buffer. Fabricated in a 0.25 mm SiGe-BiCMOS process, the synthesizer draws 45 mA from a 5 V supply and 140 mA from a 3 V supply and occupies an area of 4.8 mm2.

(2.3) 11:15–11:40AM **A 45-GHz SiGe HBT Amplifier at Greater Than 25 % Efficiency and 30 mW Output Power (Student)** **p. 25**

H.-T. Dabag, J. Kim, L.E. Larson, J. Buckwalter and P. Asbeck

A PA at 45 GHz is demonstrated in a SiGe process. The PA achieves a PAE of 25 % in class-A and 31% in class-B. The maximum output power is 14.8 dBm.

(2.4) 11:40–12:05PM **A Wide-Tuning Range, Amplitude-Locked Test Signal Source for Self-Healing, Mixed-Signal Electronic Systems (Student)** **p. 29**

S. Shankar, S. Horst, P. Saha, D. Howard, R. Diestelhorst, T. England and J. Cressler

An integrated wideband amplitude-locked test signal source for "self-healing" of multiband mixed-signal system-on-a-chip solutions is demonstrated. This work achieves the widest reported tuning range per unit die area compared to the state-of-the-art.

(2.5) 12:05–12:30PM **Fundamental Mode Colpitts VCOs at 115 and 165-GHz** **p. 33**

Y. Zhao, B. Heinemann and U. Pfeiffer

Two fundamental mode voltage controlled oscillators (VCO) at 115 and 165

GHz manufactured in a f_T/f_{max}=280/435-GHz SiGe Bipolar technology are presented. A differential Colpitts topology is used in both VCO designs, and the phase noise optimization is discussed. Without on-chip buffer, the 115-GHz VCO delivers -6.6-dBm output power with a 1.6-GHz tuning range and a -80 dBc/Hz phase noise at 100-kHz offset, and the 165-GHz VCO provides -15 dBm power with a 7.6-GHz tuning range and a -79 dBc/Hz phase noise at 500-kHz offset. Two VCOs consume 30 mW and 46 mW from a 3-V and a 4.6-V power supply respectively.

3. Virtual Technology and High-Level Modeling

Monday 10:25 AM **Room 235**
Session Chair: **J. Victory**
Co-Chair: **A. DiVergilio**

(3.1) 10:25–11:15 AM **Virtual Technology for RF Process and Device Development (Invited)** **p. 37**

T. Vanhoucke, D.B.M. Klaassen, H. Mertens, J. Donkers, G.A.M. Hurkx, H.G.A. Huizing, P. Magnee, E. Hijzen, R. van Dalen, E. Gridelet and J.W. Slotboom

The increasing complexity of modern technologies has made semiconductor process and device development challenging. A reduction in the number of experimental tests and a detailed internal insight opens the way to a more optimized process in a shorter time at reduced costs and development time. This has largely increased the use of virtual technology platforms for technology development and circuit optimization in e.g. RF BiCMOS applications. The capability of accurate predictions and directly linking basic technology parameters to RF circuit performance makes virtual technology a very powerful tool during RF process and device development. Commercially available technology computer-aided design (TCAD) tools are generally used during device fabrication and characterization, process optimization, and circuit design. With three examples we illustrate the evolution of the virtual technology process used for RF BiCMOS development within NXP Semiconductors. In the first two examples, we illustrate device and process optimization while in the third example we describe a new way of combining device and process optimization with circuit simulations by means of a distributed equivalent circuit. It allows to take the interaction between the intrinsic device (i.e. device doping profile) and the parasitic environment (i.e. device architecture) efficiently into account for high-frequency applications and in particular for low-noise circuits.

(3.2) 11:15–11:40 AM **Electro-Thermal Dynamic Simulation and Thermal Spreading Impedance Modeling of Si-Ge HBTs** **p. 45**

A.K. Sahoo, S. Fregonese, M. Weiss, N. Malbert and T. Zimmer

In this paper, a new and simple approach simulating electro-thermal dynamic behaviour of Heterojunction Bipolar Transistors (HBTs) has been demonstrated. Time domain junction temperature variations at different frequency and, therefore, thermal spreading impedance have been obtained numerically by means of 3D device simulations and which has been verified

through low frequency scattering parameter measurements for different geometry of transistors. A physical electro-thermal recursive network has been employed for HICUM compact model simulation and thermal parameters extraction.

(3.3) 11:40–12:05 PM **Improved Lumped Charge Model for High Voltage Power Diode and Automated Extraction Procedure** **p. 49**

M. Bellini, I. Stevanovic and D. Prada

The lumped charge power diode compact model is extended including impact ionization, to reproduce the current peak during reverse recovery for EMI/EMC simulations. The parameter extraction procedure is improved and automated through multi-objective genetic algorithms.

(3.4) 12:05–12:30 PM **Modeling of SiGe spike mono emitter HBT with HICUM in static and dynamic operations** **p. 53**

A. Bhattacharyya, C. Maneux, S. Fregonese and T. Zimmer

In this paper, simulation and modeling results for a npn SiGe spike mono emitter transistor are presented covering both DC and frequency operations. First, the results obtained for a SiGe spike emitter are compared with the conventional HBT. Then model parameter extraction with the help of HICUM model is performed in the simulated data for the new device. The accurate compact modeling introduces a new recombination time constant parameter inside the existing HICUML2.24 model. Modeling results with the extended model indicate good agreement not only in DC characteristics but also in dynamic behavior.

4. Ultra High-Performance SiGe Bipolar/BiCMOS

Monday 3:00 PM **Room 236**
Session Chair: **T. Obata**
Co-Chair: **D. Knoll**

(4.1) 3:00–3:50 PM **Towards THz SiGe HBTs (Invited)** **p. 57**

P. Chevalier, T. Meister, B. Heinemann, S. Van Huylenbroeck, W. Liebl, A. Fox, A. Sibaja-Hernandez and A. Chantre

This paper summarizes the technological developments carried out on SiGe HBTs in the frame of the European project DOTFIVE. The architectures of the different partners and their performances are presented and discussed showing that the project objectives have been met.

(4.2) 3:50–4:15 PM **Pedestal Collector Optimization for High Speed SiGe:C HBT** **p. 66**

S. van Huylenbroeck, A. Sibaja-Hernandez, R. Venegas, S. You, F. Vleugels, D. Radisic, W. Lee, W. Vanherle, K. de Mayer and S. Decoutere

An optimized collector doping profile for high-speed SiGe:C HBT devices is presented. A thin and abrupt collector pedestal is implemented in a fT/fMAX 245GHz/460GHz fully self-aligned HBT architecture.

(4.3) 4:15–4:40 PM **SiGe:C HBT Architecture with Epitaxial External Base** **p. 70**

A. Fox, B. Heinemann, R. Barth, S. Marschmeyer, C. Wipf and Y.

Yamamoto

We present an HBT technology with selective SiGe:C base epitaxy demonstrating fT/fmax values of 310GHz/480GHz. In this novel approach, the external base is formed epitaxially completely after the internal base.

(4.4) 4:40–5:05 PM **A Millimeter-Wave Capable SiGe BiCMOS Process with 270GHz FMAX HBTs Designed for High Volume Manufacturing** **p. 74**

E. Preisler, G. Talor, D. Howard, Z. Yan, R. Booth, J. Zheng, S. Chaudhry and M. Racanelli

A new SiGe BiCMOS process, SBC18H3 is described which features SiGe HBTs with 240GHz FT and 270 GHz FMAX. The HBT devices are described in detail along with several other mm-wave components included in the process. The process is based on a high-volume manufacturing-proven 0.18mm SiGe BiCMOS base platform which has been running at TowerJazz for almost a decade and has been used to produce over 100,000 8 inch wafers. Additional mm-wave enablement devices offered in the process include MOS varactors, P-I-N diodes and sub-10fF MIM capacitors. Additional key metrics for the SiGe HBT device include an NFMIN of 2dB at 40GHz, a BVCEO of 1.6V and a DC current gain of 1200.

5. Analog Circuit Techniques

Monday 3:00 PM **Room 235**
Session Chair: **H. Veenstra**
Co-Chair: **L. Praamsma**

(5.1) 3:00–3:25 PM **High Speed Channel Resistance Sensor Interface with Radiation Hardening by Design for Cryogenic Application from -180°C to 120°C (Student)** **p. 78**

X. Geng, F. Dai, D. Ma, Z. Chen, J. Cressler, J. Yaeger, M. Mojarradi and A. Mantooth

The high speed channel (HSC) is an analog sampling channel that comprises the bulk (2 of the 16 total) of the channels using in the RSI ASIC. The HSC is designed for inputs from sensors of various types with data rates no higher than 5 kHz.

(5.2) 3:25–3:50 PM **A Low-Power, 26-GHz Transformer-Based Regulated Cascode Transimpedance Amplifier in 0.25µm SiGe BiCMOS (Student)** **p. 82**

C. Li Cheng and S. Palermo

A 26GHz differential transimpedance amplifier is implemented in 0.25µm BiCMOS technology. Transimpedance gain is 59dBΩ. Circuit consumes 28.2mW with 2.5V supply voltage. The chip area is 960µmx780µm.

(5.3) 3:50–4:15 PM **Integrated Injection Logic in a High-Speed SiGe Bipolar Technology** **p. 86**

K. Aufinger, H. Knapp, S. Boguth, O. Gerasika and R. Lachner

A device for integrated injection logic circuits is implemented in a high speed bipolar technology without any changes to the underlying production process. Ring oscillator circuits are built with these devices and are

experimentally characterized. A gate delay of 1ns is obtained at a current of approximately 25μA per stage.

(5.4) 4:15–5:05 PM **Advances in RF Power Measurement and Control for Communications (Invited)** **p. 90**

J. Cowles

The accurate measurement of power and other attributes of signals used in communications systems has become a necessary aspect in optimizing power consumption and data throughput. From simple portable, battery-powered devices to large scale base-stations and routers, knowledge of the signal characteristics and its environment enables the system to reconfigure itself and allocate power and bandwidth as needed. A combination of high-speed silicon-based process technologies and an unrelenting focus on precision circuit design have enabled the in-situ analog signal processing of signals to be performed accurately and practically non-invasively. A review of numerous signal measurement techniques developed at Analog Devices reveals an unusual combination of high-speed and precision design techniques.

6. Mixers and LNAs

Monday 3:00 PM **Room 233**
Session Chair: **H. Gul**
Co-Chair: **A. Wang**

(6.1) 3:00–3:25 PM **An Adaptive, Wideband SiGe Image Reject Mixer for a Self-healing Receiver (Student)** **p. 99**

P. Saha, D. Howard, S. Shankar, R. Diestelhorst, T. England and J. Cressler

A SiGe 6-20 GHz adaptive image reject mixer is presented. Automated 'healing' of mixer performance (gain > 15dB, OP1dB > 10dBm and IRR > 35dB) to nullify effects of process variation is demonstrated in measurement.

(6.2) 3:25–3:50 PM **Using Saturated SiGe HBTs to Realize Ultra-Low Voltage/Power X-Band Low Noise Amplifiers (Student)** **p. 103**

S. Seth, C.-H. Poh, T. Thrivikraman, R. Arora and J. Cressler

An ultra-low voltage, monolithic 9 GHz (X-band) low noise amplifier has been implemented in 0.13 mm SiGe BiCMOS technology. The SiGe HBTs were intentionally biased in weak saturation (VCE at 0.5 V). This allows the LNA to operate at 300 K using only 2.4 mW of dc power from a 1 V supply, while delivering 16.7 dB gain and 3.5 dB noise figure at 9 GHz. At 90 K, this SiGe LNA achieves 17.5 dB of gain at only 600 mW of power, record performance for any known X-band LNA operating at sub-ambient temperatures.

(6.3) 3:50–4:15 PM **A Tunable Wideband LNA for Self-Healing Applications (Student)** **p. 107**

D. Ma, F. Dai, C.Stroud and R. Jaeger

The paper presents the design of a wideband low noise amplifier (LNA)

with self-healing technology that can simultaneously adjust both the peak gain frequency and the input matching frequency to the operating frequency. The gain of proposed LNA is also adjustable. The proposed self-healing LNA is implemented in a 0.13um SiGe BiCMOS technology. The operating frequency of the proposed LNA can be adjusted from 4.5GHz to 7.8GHz. The LNA achieves typical gain of 19dB with 14dB continuous tuning range. The measured input matching is below -12dB over the entire frequency band. The measured noise figure of the LNA is 4.2dB at 7.8GHz, and the output 1dB compression point is -9dBm. The LNA dissipates 52mW power.

(6.4) 4:15–4:40 PM **A UWB SiGe LNA for Multi-band Applications with Self-healing Based on DC Extraction of Device Characteristics (Student)** **p. 111**

D. Howard, P. Saha, S. Shankar, R. Diestelhorst, T. England and J. Cressler

We present an ultra-wideband, Low Noise Amplifier (LNA) implemented in a Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT) technology. This SiGe LNA covers a frequency range of 8-18 GHz, and achieves a peak gain of 15.6 dB at nominal bias and a nominal OIP3 of 3 dBm at 13 GHz. The Noise Figure (NF) of the LNA is 3.6-7.9 dB across band and it consumes 7 mA from a 3.3 V supply. This LNA incorporates bias control knobs for circuit "self-healing" to compensate for process-induced (or other) variations in performance metrics. Process variations are detected using a companion source measure unit (SMU) test circuit that gathers DC device information to determine the healing to be applied.

(6.5) 4:40–5:15 PM **A 4dB NF 60GHz-Band Low-Noise Amplifier with Balanced Outputs (Student)** **p. 115**

Y. Jin, J.R. Long and M. Spirito

A 60GHz-band, 2-stage low-noise amplifier with 4-6.5dB measured noise figure (50Ω) and over 9GHz bandwidth is described. Peak gain measured from single-ended input to differential outputs is 13.9dB, and input referred P-1dB and IIP3 are -18dBm and -9.8dBm, respectively. Input return loss exceeds 10dB across 50-67GHz. Implemented in 130nm SiGe-BiCMOS, the 380—240mm^2 IC consumes 6.8mA from a 2V supply.

Tuesday, October 11, 2011

7. Emerging Technologies

Tuesday 8:30 AM **Room 236**
Session Chair: **J. B. Begueret**

(7.1) 8:30–9:10 AM **Is it the End of the Road for Silicon in Power Conversion? (Invited)** **p. 119**

A. Lidow

For the past three decades, power management efficiency and cost have shown steady improvement as innovations in power MOSFET structures, technology, and circuit topologies have paced the growing need for

electrical power in our daily lives. In the last few years, however, the rate of improvement has slowed as the silicon power MOSFET has asymptotically approached its theoretical bounds. We address the new game-changing power management products, available today and planned for the near future, that are built on Gallium Nitride grown on top of a silicon substrate. Enhancement mode devices (eGaN® FETs) are demonstrated in DC-DC conversion applications. Roadmaps for improved device performance and for system-on-chip integration will also be discussed. Performance is only one dimension of the equation leading to the conclusion that eGaN technology is a game-changer. The other dimensions are product reliability, ease of use, and cost. These topics will also be discussed showing that the capability to displace silicon across a significant portion of the power management market is now in hand.

(7.2) 9:10–9:50 AM **Silicon Integrated Nanophotonics for Future Computing Systems (Invited)** **p. 125**

Y.A. Vlasov, S. Assefa, W.M.J. Green, A. Rylyakov, C. Schow, and F. Horst

CMOS Integrated Nanophotonics allows ultra-dense monolithic single-chip integration of optical and electrical functions. This technology can enable future Exaflops supercomputers by connecting racks, modules, and chips together with ultra-low power massively parallel optical interconnects.

(7.3) 9:50–10:30 AM **Microfluidics for Medical Applications (Invited)** **p. 129**

K. Grenier

Advances in microsystems integration are enabling the development of new biological and medical devices. Added to traditional functionalities including sensors, actuators, signal processing and wireless communications, microfluidic implementation to microelectronics opens the door to the elaboration of innovative and complex Lab-On-a-Chip. Various applications are targeted to allow personalized medicine with early diagnostic and therapeutic applications, as well as the monitoring of the living. It mainly involves devices for molecular, cell detection or human activity recording, and components dedicated to chemicals manipulation. This presentation will consequently give a brief overview of the possibilities offered by microfluidics devices. A focus performed on the interests of implementing microfluidics abilities with signal processing and wireless devices will then be addressed, followed by a discussion related to the heterogeneous integration of the associated technologies. Next section will present examples of low frequency based electronic circuits with microfluidic and the actual trend to reach higher frequencies such as microwave and millimeterwave will be justified. Finally, perspectives of microfluidic implementation towards exotic technologies based on flexible materials for better life monitoring and medicine, as well as their interests in genuine electronic applications will complete this status.

8. 4G and mm-Wave PA Design

Tuesday 10:55 AM **Room 236**
Session Chair: **W. Van Noort**

Co-Chair: **G. Hau**

(8.1) 10:55–11:45 AM **Load-Pull Techniques and their Applications in Power Amplifiers Design (Invited)** **p. 133**

F. Ghannouchi and M. Hashmi

This paper reviews and discusses most common load-pull techniques used in the design of power amplifiers (PAs). It also discusses and elaborates on the specific change in load-pull configuration required in order to make them optimally useful for on-wafer device characterization. Finally, distinct case studies for device characterization and PA design that utilizes a load-pull system is reported.

(8.2) 11:45–12:10 PM **A 3x3mm2 LTE/WCDMA Dual-Mode Power Amplifier Module with Integrated High Directivity Coupler** **p. 138**

G. Hau, A. Hussain, J. Turpel and J. Donnenwirth

This paper presents a 1.95GHz LTE/WCDMA GaAs HBT/pHEMT PA module with integrated directional coupler. The PA operates in two power modes, achieving 38/24% PAE at 27.5/16dBm Pout with LTE UTRA ACLR1<-39dBc. The 20dB coupler attains +/-0.06dB coupling variation under VSWR 2.5:1 mismatch.

(8.3) 12:10–12:35 PM **A Highly-Efficient BiCMOS Cascode Class-E Power Amplifier Using Both Envelope-Tracking and Transistor Resizing for LTE-Like Applications (Student)** **p. 142**

Y. Li, R. Wu, J. Lopez and D.Y.C. Lie

This paper presents the design of a SiGe differential cascode power amplifier (PA) to perform the envelope-tracking (ET) along with transistor resizing for efficiency enhancement for the 16QAM LTE. A new parallel-circuit class-E PA model is developed to analyze and design the cascode PA. The analytic results are compared with SPICE simulation and measurement data to provide circuit design insights. Measurement shows the ET-based PA system reaches an overall power-added-efficiency (PAE) of 38% at its 1 dB compression point (P1dB) of 22 dBm for its high power mode. Additionally, at the low power mode, some of the transistor cells can be disabled by the integrated MOSFET switches, and the overall PAE is improved by 4-5% at >4 dB back-off from its P1dB. The ET-based cascode PA satisfies the LTE 16QAM linearity specs without needing predistortions.

(8.4) 12:35–1:00 PM **A Q-Band SiGe Power Amplifier with 17.5 dBm Saturated Output Power and 26% Peak PAE (Student)** **p. 146**

W. Tai, L.R. Carley and D. Ricketts

A Q-band class-B power amplifier implemented in a 0.13 mm SiGe BiCMOS process is presented. At 45 GHz, the PA achieves a 17.5 dBm saturated output power, a 16.6 dB peak power gain, and a 26% peak power-added efficiency (PAE) with a 2.5V supply. A 2-stage, single-ended, inductor matched topology is used. To support envelope modulation transceiver topologies, the output common-emitter stage is optimized for high efficiency under varying supply voltage and maintains a peak PAE of greater than 21% throughout the supply voltage range of 1.3V to 2.5V. The PA occupies a total die area of 0.2 mm^2.

9. Optimization of RF Devices and Process Modules

Tuesday 10:55 AM **Room 233**
Session Chair: **J. Costa**
Co-Chair: **R. Rassel**

(9.1) 10:55–11:20 AM **Trends in GaAs HBTs for Wireless and RF** **p. 150**

M. Fresina

Gallium Arsenide heterojunction bipolar transistors are the preferred technology for cellular power amplifiers and while the basic technology has not changed significantly there have been multiple innovations to optimize performance, increase integration and reduce cost.

(9.2) 11:20–11:45 AM **Modeling of Emitter Resistance of High Speed SiGe HBTs** **p. 154**

P. Cheng, M. Dahlstrom, Q. Liu, P. Gray, J. Adkisson, B. Zetterlund, J. Pekarik, R. Camillo-Castillo, L. Cadic, J. Ellis-Monaghan and D. Harame

In this paper, we have investigated the emitter resistance Re in high speed SiGe HBTs with speeds up to 280GHz. We observed that Re increased with lateral scaling, thereby degrading fT. Although a negligible component in the past, Re * Ccb transit time delay is now playing a more significant role in achieving high fT. Re was modeled to explain the increase due to lateral scaling, and it was caused by plugging of the emitter opening by the emitter poly. Furthermore, process experiments were conducted to investigate the effect of emitter poly thickness, sidewall height, and emitter i-layer thickness.

(9.3) 11:45 AM–12:10 PM **Extended High Voltage HBTs in a High-Performance BiCMOS Process** **p. 158**

H. Mertens, P. Magnee, J. Donkers, E. Gridelet, P. Huiskamp, D. Klaassen and T. Vanhoucke

An approach to integrate extended high voltage npn SiGe heterojunction bipolar transitors in a high-performance BiCMOS process is presented. The device specifications are tunable across a wide range by the subcollector implantation energy and dose.

(9.4) 12:10–12:35 PM **Integration of Isolated RF-LDMOS Transistors in a 0.25 µm SiGe:C BICMOS Process** **p. 162**

R. Sorge, A. Fischer, J. Schmidt, C. Wipf, R. Barth and R. Pliquett

We demonstrate the modular integration of isolated NLDMOS and PLDMOS focusing on maximal RF performance into an advanced industrial 0.25 µm SiGe:C BICMOS process. A boundary condition for device construction was a maximum deep n-well implantation energy of 750keV. The achieved values BVDSS/fT/fMAX of -21V/10GHz/35GHz for the PLDMOS and 16V/30GHz/53GHz for the isolated NLDMOS, respectively, reflect the excellent RF performance obtained.

(9.5) 12:35–1:00 PM **SiGe:C profile optimization for low noise performance** **p. 166**

P.H.C. Magnee, R. van Dalen, H. Mertens, T. Vanhoucke, B. van Velzen, P. Huiskamp, I. Brunets, J.J.T.M. Donkers and D.B.M. Klaassen

Today's state-of-the-art SiGe BiCMOS processes show impressive

high-frequency performance, with fT and fMAX exceeding 500GHz. However, SiGe can also offer significant performance gain at more moderate application frequencies. In this paper we discuss the optimization of SiGe heterojunction bipolar transistors (HBTs) for very low noise applications in the 2-10GHz range. By careful tuning of the base-profile, minimum noise figures below 0.55dB and 0.35dB are obtained at 10GHz and 2GHz respectively.

10. Advanced Noise Modeling and Characterization

Tuesday 10:55 AM **Room 235**
Session Chair: **B. Ardouin**
Co-Chair: **A. Rumiantsev**

(10.1) 10:55–11:20 AM **A new technique for characterizing very low frequency noise of bipolar junction transistors** **p. 170**

H. Tuinhout, A. Zegers-van Duijnhoven, H. Mertens and A. Heringa

Using time sampled DC measurements on standard bench top semiconductor parameter analyzers it proves possible to characterize very low frequency noise of BJT's down to sub-mHz frequencies without using additional hardware such as low-noise amplifiers and low-pass filters.

(10.2) 11:20–11:45 AM **Characterization and Modeling of SiGe HBT Low-Frequency Noise in Inverse Operating Condition** **p. 174**

J. Tang, J. Babcock, T. Krakowski, L. Smith and G. Cestra

Inverse model low-frequency noise is characterized for SiGe HBTs from an advanced SiGe RF SOI technology. Impact of SIC on low-frequency noise is investigated. A methodology to model the dominating inverse mode noise source in compact models is proposed.

(10.3) 11:45–12:10 PM **Compact Noise Modeling of SiGe Heterojunction Bipolar Transistors: Relevance of Base-Collector Shot Noise Correlation and Non-Quasi Static Effects in the Quasi-Neutral Emitter (Student)** **p. 178**

F. Vitale, R. Pijper and R. van der Toorn

In this paper we address the challenge of compact model based noise prediction for present state-of-the-art and upcoming generations industrial SiGe Heterojunction Bipolar Transistors (HBTs). Firstly, we verify the paradigm of compact model based prediction of noise characteristics, from exclusively dc-and ac data. As part of this, secondly, we verify relevant modeling capabilities of the present generation standard compact model Mextram. Thirdly, by careful interpretation of remaining systematic deviations, we identify upcoming challenges in noise modeling with respect to future applications of SiGe HBT technology. We discuss the relevance of the emitter diffusion charge and of the non quasi-static (NQS) effects in the quasi-neutral (QN) emitter to noise modeling.

(10.4) 12:10–12:35 PM **Modeling High-Frequency Noise in SiGe HBTs Using Delayed Minority Charge** **p. 183**

K. Kumar and A. Chakravorty

Using delayed minority charge high-frequency correlated noise in SiGe HBT is modeled. Following system theory, the formulated model equations are accurately implemented in Verilog-A. Results show excellent agreement with numerically simulated data.

11. Characterization and Model Parameter Extraction

Tuesday 2:30 PM **Room 233**
Session Chair: **D. Weiser**
Co-Chair: **P. Tounsi**

(11.1) 2:30–2:55 PM **Experimental extraction of the base resistance of SiGe:C HBTs beyond BVCEO: An improved technique** **p. 187**

M. Costagliola, V. d'Alessandro, D. Cali, A. Chantre, P. Chevalier, T. Meister, K. Aufinger and N. Rinaldi

An improved technique based on simple dc measurements is proposed to accurately extract the base resistance dependence on biasing in advanced bipolar transistors. The method has been employed for the monitoring of the base resistance increase with collector voltage in state-of-the-art SiGe:C HBTs operated in the impact-ionization regime up to pinch-in.

(11.2) 2:55–3:20 APM **Improving Parasitic Emitter Resistance Determination Methods for Advanced SiGe:C HBT transistors** **p. 191**

B. Ardouin, C. Raya and Z. Huszka

A new parameter extraction procedure for the determination of parasitic emitter resistance of bipolar transistors is presented and compared to existing solutions . A procedure for self-heating correction is proposed to increases the accuracy of the method.

(11.3) 3:20–3:45 PM **HICUM/2 v2.3 Parameter Extraction for Advanced SiGe-Heterojunction Bipolar Transistors (Student)** **p. 195**

A. Pawlak, M. Schroter, J. Krause, D. Céli and N. Derrier

This paper presents extraction methodologies for advanced SiGe heterojunction bipolar transistors. Demonstrated methods focus on extracting the transfer current related parameters over a large temperature range for the version 2.3 of the compact HBT model HICUM Level 2.

(11.4) 3:45–4:10 PM **Method for Verification of Inductor De-embedding Accuracy by Cross-Check of Measurements with a LC Circuit** **p. 199**

C. Andrei and D. Pasquet

An innovative method for verification of de-embedding errors after inductor on-wafer measurements is presented. This first de-embedding verification method, there were no references found in literature, is easy to implement by designing a LC circuit with a Metal Insulator Metal (MIM) capacitor inside the Ground-Signal-Ground (GSG) test structure used for inductor characterization. The S parameter measurements of LC circuit (L-inductor under test, C-MIM) and of an ”open dummy” including the MIM, are used to cross-check the inductor measurements in order to verify the de-embedding accuracy. This verification allows an easy identification of S-parameter measurement issues and of de-embedding in-accuracies, and futures an

important gain of time for small signal equivalent circuit extraction. The method has been validated in the case of an ”8-shaped” inductor fabricated in QuBiC (Quality Bipolar CMOS) process by measurements up to 50 GHz.

(11.5) 4:10–4:35 PM **Influence of Probe Tip Calibration on Measurement Accuracy of Small-Signal Parameters of Advanced BiCMOS HBTs** **p. 203**

A. Rumiantsev, P. Sakalas, N. Derrier, D. Celi and M. Schroter

This paper presents investigation results of the probe-tip calibration impact on the BiCMOS HBT small-signal parameter measurement accuracy. Three popular calibration procedures were applied on the same data set and followed by the two-step de-embedding from the device dedicated Compete-Open and Complete-Short dummy elements. Experimental results showed that the observed difference in cold HBT parameters and parameters of passive devices was minimized by the de-embedding step. The fT and fMAX demonstrated higher sensitivity to the probe-tip calibration residual errors.

12. Front End ICs for Radar and Mobile Applications

Tuesday 2:30 PM **Room 236**
Session Chair: **F. Dai**
Co-Chair: **Y. Xu**

(12.1) 2:30–2:55 PM **Single-Chip Receiver Front-End for 79GHz Automotive Radar (Student)** **p. 207**

R. Severino, A. Mariano, C. Ameziane, Y. Deval, D. Belot, J.B. Begueret and T. Taris

A 79GHz receiver front-end for automotive applications has been implemented in a 130nm SiGe technology supporting millimeter wave design. The receiver consists of a two-stage LNA, a double-balanced down-conversion Mixer and a synchronized VCO. Design and test results for each RF circuit block are presented, followed by a characterization of the integrated receiver.

(12.2) 2:55–3:20 PM **A Low Power 9.75/10.6GHz Down-Converter IC in SiGe:C BiCMOS for Ku-Band Satellite LNBs** **p. 211**

P. Philippe, L. Praamsma, R. Breunisse, E. van der Heijden, F. Meng, S. Bardy, F. Moreau, S. Wane and E. Thomas

A low cost / low power BiCMOS Ku-band down-converter IC with integrated LO-PLL for satellite TV is presented. The down-converter section shows 43dB conversion gain, with 6.5dB noise figure and output IP3 of 16dBm. The LO-PLL section achieves state-of-art integrated phase noise performance of 1Â° rms. The down-converter operates from the 5V supply.

(12.3) 3:20–3:45 PM **A Low-Power 80GHz FMCW Radar Transmitter with Integrated 23GHz Downconverter VCO** **p. 215**

N. Pohl, T. Klein, K. Aufinger and H.M. Rein

A Low-Power FMCW 80 GHz Radar transmitter chip is presented, which was fabricated in a SiGe bipolar production technology (fT = 180 GHz, fmax = 250 GHz).Additionally to the fundamental 80 GHz VCO (voltage controlled

oscillator), a Ã·4-frequency divider (65 mW), a 23 GHz local oscillator (60 mW) with a low phase noise of -112 dBc/Hz (1 MHz offset), a PLL-mixer and a static frequency divider is integrated. The chip generates a high output power of > 10 dBm in a 24.5 GHz wide frequency band around 80 GHz with an overall power consumption of only 0.5 W.

(12.4) 3:45–4:10 PM **An Integrated 77-GHz Six-Port Receiver Front End for Angle-of-Arrival Detection (Student)** **p. 219**

B. Laemmle, G. Vinci, L. Maurer, A. Koelpin and R. Weigel

In this paper an integrated six-port receiver frontend for angle-of-arrival detection of 77-GHz signals is presented. Application of the circuit is direction finding, automotive radar calibration, or high precision industrial radar. The measurement principle is based on superposition of two incident signals and power detection. The circuit has two input amplifiers, a broadband passive six-port network, and four power detectors. The integrated circuit has a power consumption of 95mW from a 5V supply. It is fabricated in a 200-GHz fT SiGe bipolar technology and occupies only 1028x1128 mm². Functionality is demonstrated by applying two different frequencies at the input ports. A simple calibration method is proposed and all calibration parameters are calculated.

(12.5) 4:10–4:35 PM **A Compact BiFET Front-End Module for 802.11a/b/g/n TX/RX and 802.16e RX Using a Triplexer Filter** **p. 223**

W. Williams, T. Cho, O. Mustafa, A. Patel, R. Ribafeita and M. Trippe

Compact front-end module (FEM) incorporating WiFi TX/RX paths and WiMAX RX paths is presented. The FEM is dual-band-transmit/tri-band-receive. By integrating InGaP HBT power amplifiers and pHEMT T/R switches on a single die, this functionality is achieved in a 1.4 X 4 X 5.4 mm surface mount module. Assembly involves only one wire-bonded GaAs die and three SMD components on a 4-layer FR-4 laminate. On Transmit, the FEM covers 2.4 – 2.484 GHz and 5.15 – 5.875 GHz with 10% EVM at +17 dBm output. Receive bands are 2.3-2.69 GHz, 3.4 – 3.8 GHz and 5.15 – 5.875 GHz. All receive bands are passive. Through the use of a triplexer filter, switches are eliminated from the 3.4 – 3.8 GHz receive path, achieving a typical insertion loss of 1.5 dB in that band. Design and performance of the key subcomponents are presented, as well as top level FEM performance.

13. Power Devices & ESD

Tuesday 2:30 PM **Room 235**
Session Chair: **P. Magnee**
Co-Chair: **H. C. Wu**

(13.1) 2:30–3:20 PM **SiC Bipolar Devices for High Power and Integrated Drivers (Invited)** **p. 227**

M. Östling, R. Ghandi, B. Buono, L. Lanni, B. G. Malm and C.M. Zetterling

Silicon carbide (SiC) semiconductor devices for high power applications are now commercially available as discrete devices. The first SiC device to

reach the market was the unipolar Schottky diode. Active switching devices such as bipolar junction transistors (BJTs), field effect transistors (JFETs and MOSFETs) are now being offered in the voltage range up to 1.2 kV. SiC material quality and epitaxy processes have greatly improved and degradation free 100 mm wafers are readily available, which has removed one obstacle for the introduction of bipolar devices. The SiC wafer roadmap looks very favorable as volume production takes off. Other advantages of SiC is the possibility of high temperature operation (> 300 °C) and in radiation hard environments, which could offer considerable system advantages. Thanks to the mature SiC process technology, low-power integrated circuits are now also viable. Such circuits could find use in integrated drivers operating at elevated temperatures.

(13.2) 3:20–3:45 PM **Design of SCR Devices for SiGe BiCMOS Applications** **p. 235**

S. Parthasarathy, J. Salcedo and J.J. Hajjar

An optimum vertical SiGe SCR design is presented for on-chip electrostatic discharge (ESD) protection. The device response to fast transients, emulating ESD CDM-type events, is compared with standard clamp structures having similar footprint-area, loading-capacitance and current handling ability. SCR designs include variation in the device's anode construction, anode geometry and triggering mechanism.

(13.3) 3:45–4:10 PM **Characterizing Phase Switching Structures for ESD Protection (Student)** **p. 239**

J. Liu, L. Zhang, Z. Shi, X. Wang, L. Lin, L. Wang, C. Zhang, A. Wang, Y. Cheng, R. Huang, B. Zhao and G. Zhang

We propose a non-traditional nano phase switching ESD protection mechanism and systematic characterization of a set of prototype nano crossbar phase switching ESD structures. Experimental results using transmission line pulse (TLP) and very-fast TLP (VF-TLP) testing confirm the new ESD protection concept and reveal critical ESD protection properties related to device structures, sizes and material compositions. Sample structures demonstrated very fast response to 100pS ESD transient, extremely low leakage of pA level, varying ESD triggering voltage and robust HBM ESD protection capability of at least 215V/mm^2. This comprehensive characterization shall lead to design optimization of the new nano crossbar ESD protection structures for advanced ICs.