

2011 IEEE/ACM International Conference on Computer-Aided Design

(ICCAD 2011)

**San Jose, California, USA
7 – 10 November 2011**



IEEE Catalog Number: CFP11CAD-PRT
ISBN: 978-1-4577-139; -6

TABLE OF CONTENTS

Session 1-A Beyond Printing Single

Moderator: Andres Torres – Mentor Graphics Corp.

1A.1	Layout Decomposition for Triple Patterning Lithography	1
	<i>Bei Yu, Kun Yuan, Boyang Zhang, Duo Ding, David Z. Pan</i>	
1A.2	Optimal Layout Decomposition for Double Patterning Technology	9
	<i>Xiaoping Tang, Minsik Cho</i>	
1A.3	A Framework for Double Patterning-Enabled Design	14
	<i>Rani S. Ghaida, Kanak B. Agarwal, Sani R. Nassif, Xin Yuan, Lars W. Liebmann, Puneet Gupta</i>	

Session 1-B Memory and Delay Test

Moderator: Haralampos Stratigopoulos – TIMA Laboratory/CNRS

1B.1	Unequal-Error-Protection Codes in SRAMs for Mobile Multimedia Applications	21
	<i>Xuebei Yang, Kartik Mohanram</i>	
1B.2	Detecting Stability Faults in Sub-Threshold SRAMs	28
	<i>Chen-Wei Lin, Hao-Yu Yang, Chin-Yuan Huang, Hung-Hsin Chen, Mango C.-T. Chao</i>	
1B.3	Pseudo-Functional Testing for Small Delay Defects Considering Power Supply Noise Effects	34
	<i>Feng Yuan, Xiao Liu, Qiang Xu</i>	

Session 1-C Manufacturing-Aware Optimizing Power, Performance and Reliability of the Memory Hierarchy of Embedded Systems

Moderator: Puneet Gupta – Univ. of California, Los Angeles

1C.1	A Low-Power Memory Architecture with Application-Aware Power Management for Motion and Disparity Estimation in Multiview Video Coding	40
	<i>Bruno Zatt, Muhammad Shafique, Sergio Bampi, Jörg Henkel</i>	
1C.2	Bandwidth-Aware Reconfigurable Cache Design with Hybrid Memory Technologies	48
	<i>Jishen Zhao, Cong Xu, Yuan Xie</i>	
1C.3	Feedback Control based Cache Reliability Enhancement for Emerging Multicores	56
	<i>Hui Zhao, Akbar Sharifi, Shekhar Srikantaiah, Mahmut Kandemir</i>	

Session 1-S The ABCs of Formal Verification: Models, Algorithms, and Methodologies in RTL- and ESL-Based Design Flows

Moderator: Robert Brayton – Univ. of California, Berkeley

1S.1	The First Taste of Formal Verification	n/a
	<i>Alan Mishchenko</i>	

1S.2	Methodologies of System-on-Chip Property Checking	n/a
	<i>Wolfgang Kunz</i>	
1S.3	Measuring Verification Progress and Quality	n/a
	<i>Raik Brinkmann</i>	
1S.4	System-Level to RTL Equivalence Checking	n/a
	<i>Alfred Koelbl</i>	

Session 1-T GPU Programming for EDA with OpenCL

1T.1	GPU Programming for EDA with OpenCL	63
	<i>Rasit O. Topaloglu, Benedict Gaster</i>	

Session 2-A Placement and Clocking

Moderators: *Joe Shinnerl – Mentor Graphics Corp.*
Saurabh Adya – Magma Design Automation, Inc.

2A.1	A SimPLR Method for Routability-Driven Placement	67
	<i>Myung-Chul Kim, Jin Hu, Dong-Jin Lee, Igor L. Markov</i>	
2A.2	Ripple: An Effective Routability-Driven Placer by Iterative Cell Movement	74
	<i>Xu He, Tao Huang, Linfu Xiao, Haitong Tian, Guxin Cui, Evangeline F.Y. Young</i>	
2A.3	Routability-Driven Analytical Placement for Mixed-Size Circuit Designs	80
	<i>Meng-Kai Hsu, Sheng Chou, Tzu-Hen Lin, Yao-Wen Chang</i>	
2A.4	PRICE: Power Reduction by Placement and Clock-Network Co-Synthesis for Pulsed-Latch Designs	85
	<i>Yi-Lin Chuang, Hong-Ting Lin, Tsung-Yi Ho, Yao-Wen Chang, Diana Marculescu</i>	

Session 2-B Recent Advances in Behavioral Modeling and Timing Analysis

Moderators: *Xin Li – Carnegie Mellon Univ.*
Tao Lin – Magma Design Automation, Inc.

2B.1	Efficient Analytical Macromodeling of Large Analog Circuits by Transfer Function Trajectories	91
	<i>Dimitri De Jonghe, Georges Gielen</i>	
2B.2	Optimal Statistical Chip Disposition	95
	<i>Vladimir Zolotov, Jinjun Xiong</i>	
2B.3	Temperature Aware Statistical Static Timing Analysis	103
	<i>Artem Rogachev, Lu Wan, Deming Chen</i>	
2B.4	Fast Statistical Timing Analysis for Circuits with Post-Silicon Tunable Clock Buffers	111
	<i>Bing Li, Ning Chen, Ulf Schlichtmann</i>	

Session 2-C Caches and Parallel Embedded Software*Moderator: Nalini Vasudenvan – Intel Corp.*

2C.1	Improving Shared Cache Behavior of Multithreaded Object-Oriented Applications in Multicores	118
	<i>Mahmut Kandemir, Shekhar Srikantaiah, Seung Woo Son</i>	
2C.2	CIPARSim: Cache Intersection Property Assisted Rapid Single-Pass FIFO Cache Simulation Technique	126
	<i>Mohammad Shihabul Haque, Jorgen Peddersen, Sri Parameswaran</i>	
2C.3	Cooperative Parallelization	134
	<i>Praveen Yedlapalli, Emre Kultursay, Mahmut T. Kandemir</i>	
2C.4	Optimizing Data Locality using Array Tiling	142
	<i>Wei Ding, Yuanrui Zhang, Jun Liu, Mahmut Kandemir</i>	
2C.5	Assuring Application-Level Correctness Against Soft Errors	150
	<i>Jason Cong, Karthik Gururaj</i>	

Session 2-S The Role of EDA in Digital Print Automation and Infrastructure Optimization*Moderator: Mehdi Tahoori – Karlsruhe Institute of Technology*

2S.0	The Role of EDA in Digital Print Automation and Infrastructure Optimization	158
	<i>Krishnendu Chakrabarty, Rick Bellamy, Gary Dispoto, Jun Zeng</i>	

Session 3-A DFM: From Test Structures to Computation*Moderator: Rasit Topaloglu – GLOBALFOUNDRIES*

3A.1	Toward Efficient Spatial Variation Decomposition via Sparse Regression	162
	<i>Wangyang Zhang, Karthik Balakrishnan, Xin Li, Duane Boning, Rob Rutenbar</i>	
3A.2	REBEL and TDC: Two Embedded Test Structures for On-Chip Measurements of Within-Die Path Delay Variations	170
	<i>Charles Lamech, James Aarestad, Jim Plusquellec, Reza Rad, Kanak Agarwal</i>	
3A.3	Accelerating Aerial Image Simulation with GPU	178
	<i>Hongbo Zhang, Tan Yan, Martin D.F. Wong, Sanjay J. Patel</i>	

Session 3-B High-Level and Sequential Synthesis*Moderator: Forrest Brewer – Univ. of California, Santa Barbara*

3B.1	Combined Loop Transformation and Hierarchy Allocation for Data Reuse Optimization	185
	<i>Jason Cong, Peng Zhang, Yi Zou</i>	
3B.2	High-Level Synthesis with Distributed Controllers for Fast Timing Closure	193
	<i>Seokhyun Lee, Kiyoung Choi</i>	
3B.3	Synthesis of Parallel Binary Machines	200
	<i>Elena Dubrova</i>	

Session 3-C Addressing the Physical Challenges of NoC Design*Moderator: Sherief Reda – Brown Univ.*

- 3C.1 Chemical-Mechanical Polishing Aware Application-Specific 3D NoC Design** 207
Wooyoung Jang, Ou He, Jae-Seok Yang, David Z. Pan
- 3C.2 Application-Aware Deadlock-Free Oblivious Routing based on Extended Turn-Model** 213
Ali Shafiee, Mahdy Zolghadr, Mohammad Arjomand, Hamid Sarbazi-Aazad
- 3C.3 Co-Design of Channel Buffers and Crossbar Organizations in NoCs Architectures** 219
Avinash Kodi, Randy Morris, Dominic DiTomaso, Ashwini Sarathy, Ahmed Louri

Session 3-S Emerging Technologies: The Next Logic Switch

- 3S.1 Carbon Nanotube Imperfection-Immune Digital VLSI: Frequently Asked Questions Updated** 227
Hai Wei, Jie Zhang, Lan Wei, Nishant Patil, Albert Lin, Max M. Shulaker, Hong-Yu Chen, H.-S. Philip Wong, Subhasish Mitra
- 3S.2 Alternative Design Methodologies for the Next Generation Logic Switch** 231
Davide Sacchetto, Michele De Marchi, Giovanni DeMicheli, Yusuf Leblebici
- 3S.3 A Proposed Novel Graphene Switch: Bilayer Pseudospin Field Effect Transistor** n/a
Sanjay Banerjee, Frank Register, Emanuel Tutuc

Session 3-T Emerging Nonvolatile Memory and Memristors*Moderator: Yiran Chen – Univ. of Pittsburgh*

- 3T.1 Progress and Outlook for STT-MRAM** 235
Yiming Huai, Yuchen Zhou, Ioan Tudosa, Roger Malmhall, Rajiv Ranjan, Jing Zhang
- 3T.2 Universal Statistical Cure for Predicting Memory Loss** 236
Rajiv Joshi, Rouwaida Kanj, Peiyuan Wang, Hai Li
- 3T.3 Hybrid CMOS/Magnetic Process Design Kit and Application to the Design of High-Performances Non-Volatile Logic Circuits** 240
Guillaume Prenat, Bernard Dieny, Jean-Pierre Nozieres, Gregory DiPendina, Khaldoun Torki
- 3T.4 Progress in CMOS-Memristor Integration** 246
Gilberto Medeiros-Ribeiro, Janice H. Nickel, J. Joshua Yang

Session 4-A Advances in Global Routing*Moderators: Zhuo Li – IBM Corp.**Yi-Kan Cheng – Taiwan Semiconductor Manufacturing Co., Ltd.*

- 4A.1 MGR: Multi-Level Global Router** 250
Yue Xu, Chris Chu
- 4A.2 Congestion Analysis for Global Routing via Integer Programming** 256
Hamid Shojaei, Azadeh Davoodi, Jeffrey T. Linderoth
- 4A.3 High-Quality Global Routing for Multiple Dynamic Supply Voltage Designs** 263
Wen-Hao Liu, Yih-Lang Li, Kai-Yuan Chao

**Session 4-B Analog/Mixed-Signal Design Challenges:
Temperature, Verification and the Human Factor**
Moderator: *Lei He – Univ. of California, Los Angeles*

- 4B.1 **Assessing the Impact of Steep Temperature Gradients within Automotive Power SoCs** n/a
Volker Meyer zu Bexten, Christian Funke, Jens Bargfrede
- 4B.2 **Gaps in the Verification of Automotive Mixed-Signal Systems** n/a
Achim Graupner
- 4B.3 **The Human Factor in Mixed-Signal Design and its Consequences for EDA** n/a
Ralf Brederlow

Session 4-S The Future of Clock Network Synthesis
Moderator: *Andrew B. Kahng – Univ. of California at San Diego*

- 4S.0 **The Future of Clock Network Synthesis** 270
Cliff Sze
- 4S.1 **Myth Busters: Microprocessor Clocking is from Mars, ASICs Clocking is from Venus** 271
Joseph Kozhaya, Philip Restle, Haifeng Qian
- 4S.2 **Clocking Design Automation in Intel's Core i7 and Future Designs** 276
Ali M. El-Husseini, Matthew Morrissey
- 4S.3 **Algorithmic Tuning of Clock Trees and Derived Non-Tree Structures** 279
Igor L. Markov, Dong-Jin Lee

Session 5-A Routing Optimization Techniques
Moderators: *Mustafa Ozdal – Intel Corp.*
Dwight Hill – Synopsys, Inc.

- 5A.1 **DOPPLER: DPL-Aware and OPC-Friendly Gridless Detailed Routing with Mask Density Balancing** 283
Yen-Hung Lin, Yong-Chan Ban, David Z. Pan, Yih-Lang Li
- 5A.2 **A Jumper Insertion Algorithm under Antenna Ratio and Timing Constraints** 290
Xin Gao, Luca Macchiarulo
- 5A.3 **Exploring High Throughput Computing Paradigm for Global Routing** 298
Yiding Han, Dean Michael Ancajas, Koushik Chakraborty, Sanghamitra Roy
- 5A.4 **Escape Routing for Staggered-Pin-Array PCBs** 306
Yuan-Kai Ho, Hsu-Chieh Lee, Yao-Wen Chang

Session 5-B Let's Gap Together! Urgent ToDo's for EDA from Industry Point of View**Moderator:** *Yiyu Shi – Missouri Univ. of Science and Technology*

- 5B.1 Joint Industry Effort to Address Gaps in Functional Verification and Digital Implementation Tools** n/a

Matthias Bauer, Jay Bhadra, David Crohn, Thomas Dillinger, Björn Fjellborg, Joonyoung Kim, David Lacey, Jing Li, Hassan Naser, Bart Martinec, Werner May, Khankap Mounarath, Arjun Rajagopal, Shyam Ramji, Bill Read, Ramond Rodriguez, Christopher Spandikow, Robert Titus, Helen Xia, James You, Thomas Harms, Martin Foltin

- 5B.2 Uniting to Overcome a Mounting BEOL Electromigration Reliability Challenge** n/a

Leon Sigal, C.K. Hu, C. Xu, H. Smith, J. Wanock, S. Nassif

- 5B.3 Handling Variability in Block-Level Design – Challenges & Solutions** n/a

Frank Schenkel

Session 5-C System Level Modeling for Early Design Space Exploration, Simulation, and Synthesis**Moderators:** *Mahmut Kandemir – Pennsylvania State Univ.*

Ken Stevens – Univ. of Utah

- 5C.1 Modeling the Computational Efficiency of 2-D and 3-D Silicon Processors for Early-Chip Planning** 310

Matthew Grange, Axel Jantsch, Roshan Weerasekera, Dinesh Pamunuwa

- 5C.2 The STeTSiMS STT-RAM Simulation and Modeling System** 318

Clinton W. Smullen, IV, Anurag Nigam, Sudhanva Gurumurthi, Mircea R. Stan

- 5C.3 Massively Parallel Programming Models used as Hardware Description Languages: The OpenCL Case** 326

Muhsen Owaida, Nikolaos Bellas, Christos D. Antonopoulos, Konstantis Daloukas, Charalambos Antoniadis

Session 5-S Brain-Inspired Architectures: Abstractions to Accelerators

- 5S.1 Neuromorphic Modeling Abstractions and Simulation of Large-Scale Cortical Networks** 334

Jeffrey L. Krichmar, Nikil Dutt, Jayram M. Nageswaran, Micah Richert

- 5S.2 A Framework for Accelerating Neuromorphic-Vision Algorithms on FPGAs** 810

M. DeBole, A. Al Maashri, M. Cotter, C-L. Yu, C. Chakrabarti, V. Narayanan

- 5S.3 A Heterogeneous Accelerator Platform for Multi-Subject Voxel-Based Brain Networks Analysis** 339

Yu Wang, Mo Xu, Ling Ren, Xiaorui Zhang, Di Wu, Yong He, Ningyi Xu, Huazhong Yang

Session 6-A Modeling of Devices and Analog Systems**Moderators:** *Amith Singhee – IBM T.J. Watson Research Ctr.*

Luca Daniel – Massachusetts Institute of Technology

- 6A.1 Fast Statistical Model of TiO₂ Thin-Film Memristor and Design Implication** 345

Miao Hu, Hai Li, Robinson E. Pino

- 6A.2 Accelerated Statistical Simulation via On-Demand Hermite Spline Interpolations** 353

Rouwaida Kanj, Tong Li, Rajiv Joshi, Kanak Agarwal, Ali Sadigh, David Winston, Sani Nassif

6A.3	Structure Preserving Reduced-Order Modeling of Linear Periodic Time-Varying Systems	361
	<i>Ting Mei, Heidi Thornquist, Eric Keiter, Scott Hutchinson</i>	
6A.4	ModSpec: An Open, Flexible Specification Framework for Multi-Domain Device Modelling	367
	<i>David Amsallem, Jaijeet Roychowdhury</i>	
 Session 6-B Logic Level Synthesis		
<i>Moderator:</i>	<i>Barry Pangrle – Mentor Graphics Corp.</i>	
6B.1	Delay Optimization using SOP Balancing	375
	<i>Alan Mishchenko, Robert Brayton, Stephen Jang, Victor Kravets</i>	
6B.2	Match and Replace – A Functional ECO Engine for Multi-Error Circuit Rectification	383
	<i>Shao-Lun Huang, Wei-Hsun Lin, Chung-Yang Huang</i>	
6B.3	Towards Completely Automatic Decoder Synthesis	389
	<i>Hsiou-Yuan Liu, Yen-Cheng Chou, Chen-Hsuan Lin, Jie-Hong R. Jiang</i>	
6B.4	On Rewiring and Simplification for Canonicity in Threshold Logic Circuits	396
	<i>Pin-Yi Kuo, Chun-Yao Wang, Ching-Yi Huang</i>	
6B.5	Inferring Assertion for Complementary Synthesis	404
	<i>ShengYu Shen, Ying Qin, JianMin Zhang</i>	
 Session 6-C Robustness and Variability		
<i>Moderators:</i>	<i>Arijit Raychowdhury – Intel Corp.</i>	
	<i>Miroslav Velev – Aries Design Automation, LLC</i>	
6C.1	Statistical Aging Analysis with Process Variation Consideration	412
	<i>Sangwoo Han, Joohee Choung, Byung-Su Kim, Bong Hyun Lee, Hungbok Choi, Juho Kim</i>	
6C.2	A New Method for Multiparameter Robust Stability Distribution Analysis of Linear Analog Circuits	420
	<i>Changhao Yan, Sheng-Guo Wang, Xuan Zeng</i>	
6C.3	Failure Diagnosis of Asymmetric Aging under NBTI	428
	<i>Jyothi Bhaskarr Velamala, Venkatesa Ravi, Yu Cao</i>	
6C.4	In-System and On-the-Fly Clock Tuning Mechanism to Combat Lifetime Performance Degradation	434
	<i>Zahra Lak, Nicola Nicolici</i>	
6C.5	Online Clock Skew Tuning for Timing Speculation	442
	<i>Rong Ye, Feng Yuan, Qiang Xu</i>	
 Session 6-D CAD for Bio/Nano/Post-CMOS Systems		
<i>Moderator:</i>	<i>Deming Chen – Univ. of Illinois at Urbana-Champaign</i>	
6D.1	Reliability-Oriented Broadcast Electrode-Addressing for Pin-Constrained Digital Microfluidic Biochips	448
	<i>Tsung-Wei Huang, Tsung-Yi Ho, Krishnendu Chakrabarty</i>	

6D.2	Defect-Tolerant Logic Implementation onto Nanocrossbars by Exploiting Mapping and Morphing Simultaneously	456
	<i>Yehua Su, Wenjing Rao</i>	
6D.3	Device-Architecture Co-Optimization of STT-RAM based Memory for Low Power Embedded Systems	463
	<i>Cong Xu, Dimin Niu, Xiaochun Zhu, Seung H. Kang, Matt Nowak, Yuan Xie</i>	
6D.4	STT-RAM Cell Design Optimization for Persistent and Non-Persistent Error Rate Reduction: A Statistical Design View	471
	<i>Yaojun Zhang, Xiaobin Wang, Yiran Chen</i>	
Session 6-S	2011 TAU Power Grid Simulation Contest	
<i>Moderator:</i>	<i>Sani Nassif – IBM Corp.</i>	
6S.1	2011 TAU Power Grid Simulation Contest: Benchmark Suite and Results	478
	<i>Zhuo Li, Raju Balasubramanian, Frank Liu, Sani Nassif</i>	
6S.2	PowerRush: A Linear Simulator for Power Grid	482
	<i>Jianlei Yang, Zuowei Li, Yici Cai, Qiang Zhou</i>	
6S.3	Fast Static Analysis of Power Grids: Algorithms and Implementations	488
	<i>Zhiyu Zeng, Tong Xu, Zhuo Feng, Peng Li</i>	
6S.4	On the Preconditioner of Conjugate Gradient Method – A Power Grid Simulation Perspective	494
	<i>Chung-Han Chou, Nien-Yu Tsai, Hao Yu, Che-Rung Lee, Yiyu Shi, Shih-Chieh Chang</i>	
Session 7-A	Analog Circuit Sizing and Layout Optimization	
<i>Moderator:</i>	<i>Lars Hedrich – Frankfurt Univ.</i>	
7A.1	PTrace: Derivative-Free Local Tracing of Bicriterial Design Tradeoffs	498
	<i>Amith Singhee</i>	
7A.2	A Methodology for Local Resonant Clock Synthesis using LC-Assisted Local Clock Buffers	503
	<i>Walter J. Condley, II, Xuchu Hu, Matthew R. Guthaus</i>	
7A.3	A Corner Stitching Compliant B*-Tree Representation and Its Applications to Analog Placement	507
	<i>Hui-Fang Tsao, Pang-Yen Chou, Shih-Lun Huang, Yao-Wen Chang, Mark Po-Hung Lin, Duan-Ping Chen, Dick Liu</i>	
7A.4	Heterogeneous B*-Trees for Analog Placement with Symmetry and Regularity Considerations	512
	<i>Pang-Yen Chou, Hung-Chih Ou, Yao-Wen Chang</i>	
7A.5	Fast Analog Layout Prototyping for Nanometer Design Migration	517
	<i>Yi-Peng Weng, Hung-Ming Chen, Tung-Chieh Chen, Po-Cheng Pan, Chien-Hung Chen, Wei-Zen Chen</i>	

Session 7-B Modeling and Simulation of Interconnect and Power Networks
Moderator: *Ibrahim (Abe) M. Elfadel – Masdar Institute of Science and Tech.*

7B.1	Model Order Reduction of Fully Parameterized Systems by Recursive Least Square Optimization	523
	<i>Zheng Zhang, Ibrahim (Abe) M. Elfadel, Luca Daniel</i>	
7B.2	Fast Poisson Solver Preconditioned Method for Robust Power Grid Analysis	531
	<i>Jianlei Yang, Yici Cai, Qiang Zhou, Jin Shi</i>	
7B.3	Modeling and Estimation of Power Supply Noise using Linear Programming	537
	<i>Farshad Firouzi, Saman Kiamehr, Mehdi B. Tahoori</i>	
7B.4	Power Grid Analysis with Hierarchical Support Graphs	543
	<i>Xueqian Zhao, Jia Wang, Zhuo Feng, Shiyuan Hu</i>	
7B.5	Vectorless Verification of RLC Power Grids with Transient Current Constraints	548
	<i>Xuanxing Xiong, Jia Wang</i>	

Session 7-C Stress, Electromigration, and Soft Error Mitigation
Moderators: *Qiang Xu – The Chinese Univ. of Hong Kong*
Yuan Xie – Pennsylvania State Univ.

7C.1	Electromigration Modeling and Full-Chip Reliability Analysis for BEOL Interconnect in TSV-Based 3D ICs	555
	<i>Mohit Pathak, Jiwoo Pak, David Z. Pan, Sung Kyu Lim</i>	
7C.2	Full-Chip Through-Silicon-Via Interfacial Crack Analysis and Optimization for 3D IC	563
	<i>Moongon Jung, Xi Liu, Suresh K. Sitaraman, David Z. Pan, Sung Kyu Lim</i>	
7C.3	Variation-Aware Electromigration Analysis of Power/Ground Networks	571
	<i>Di-An Li, Małgorzata Marek-Sadowska</i>	
7C.4	Low-Power Multiple-Bit Upset Tolerant Memory Optimization	577
	<i>Seokjoong Kim, Matthew R. Guthaus</i>	
7C.5	Mitigating FPGA Interconnect Soft Errors by In-Place LUT Inversion	582
	<i>Naifeng Jing, Ju-Yueh Lee, Weifeng He, Zhigang Mao, Lei He</i>	

Session 8-B Advances in Debugging and Simulation
Moderators: *Pankaj Chauhan – Calypto Design Systems, Inc.*
Sanjit Seshia – Univ. of California, Berkeley

8B.1	Debugging with Dominance: On-the-Fly RTL Debug Solution Implications	587
	<i>Hratch Mangassarian, Duncan Exon Smith, Andreas Veneris, Sean Safarpour</i>	
8B.2	Simulation-Based Signal Selection for State Restoration in Silicon Debug	595
	<i>Debapriya Chatterjee, Calvin McCarter, Valeria Bertacco</i>	
8B.3	Toward an Extremely-High-Throughput and Even-Distribution Pattern Generator for the Constrained Random Simulation Techniques	602
	<i>Bo-Han Wu, Chun-Ju Yang, Chia-Cheng Tso, Chung-Yang (Ric) Huang</i>	

Session 8-C System-Level Power Management*Moderator: Sheldon Tan – Univ. of California, Riverside*

8C.1	Identifying the Optimal Energy-Efficient Operating Points of Parallel Workloads	608
	<i>Ryan Cochran, Can Hankendi, Ayse Coskun, Sherief Reda</i>	
8C.2	System-Level Application-Aware Dynamic Power Management in Adaptive Pipelined MPSoCs for Multimedia	616
	<i>Haris Javaid, Muhammad Shafique, Jörg Henkel, Sri Parameswaran</i>	
8C.3	Balanced Reconfiguration of Storage Banks in a Hybrid Electrical Energy Storage System	624
	<i>Younghyun Kim, Sangyoung Park, Yanzhi Wang, Qing Xie, Naehyuck Chang, Massimo Poncino, Massoud Pedram</i>	

Session 9-A Advances in Clocking and Routing for ASIC and On-Chip Communication*Moderators: Shiyan Hu – Michigan Technological Univ.**Evangeline Young – The Chinese Univ. of Hong Kong*

9A.1	Multilevel Tree Fusion for Robust Clock Networks	632
	<i>Dong-Jin Lee, Igor L. Markov</i>	
9A.2	Implementation of Pulsed-Latch and Pulsed-Register Circuits to Minimize Clocking Power	640
	<i>Seungwhun Paik, Gi-Joon Nam, Youngsoo Shin</i>	
9A.3	Useful-Skew Clock Optimization for Multi-Power Mode Designs	647
	<i>Hsuan-Ming Chou, Hao Yu, Shih-Chieh Chang</i>	
9A.4	A Tree-Based Topology Synthesis for On-Chip Network	651
	<i>Jason Cong, Yuhui Huang, Bo Yuan</i>	

Session 9-B Frontiers in Verification*Moderators: Sanjit Seshia – Univ. of California, Berkeley**Pankaj Chauhan – Calypto Design Systems, Inc.*

9B.1	Formal Verification of Phase-Locked Loops using Reachability Analysis and Continuation	659
	<i>Matthias Althoff, Akshay Rajhans, Bruce H. Krogh, Soner Yaldiz, Xin Li, Larry Pileggi</i>	
9B.2	MACACO: Modeling and Analysis of Circuits for Approximate Computing	667
	<i>Rangharajan Venkatesan, Amit Agarwal, Kaushik Roy, Anand Raghunathan</i>	
9B.3	Property-Specific Sequential Invariant Extraction for SAT-Based Unbounded Model Checking	674
	<i>Hu-Hsi Yeh, Cheng-Yin Wu, Chung-Yang (Ric) Huang</i>	
9B.4	Automatic Formal Verification of Multithreaded Pipelined Microprocessors	679
	<i>Miroslav N. Velev, Ping Gao</i>	
9B.5	Accelerating RTL Simulation with GPUs	687
	<i>Hao Qian, Yangdong Deng</i>	

Session 9-C System-Level Power and Thermal Estimation
Moderators: *Jörg Henkel – Karlsruher Institut für Technologie*
Sri Parameswaran – Univ. of New South Wales

9C.1	CACTI-P: Architecture-Level Modeling for SRAM-Based Structures with Advanced Leakage Reduction Techniques	694
	<i>Sheng Li, Ke Chen, Jung Ho Ahn, Jay B. Brockman, Norman P. Jouppi</i>	
9C.2	A Trace Compression Algorithm Targeting Power Estimation of Long Benchmarks	702
	<i>Andrey Ayupov, Steven Burns</i>	
9C.3	A Theoretical Probabilistic Simulation Framework for Dynamic Power Estimation	708
	<i>L. Wang, M. Olbrich, E. Barke, T. Büchner, M. Bühler, P. Panitz</i>	
9C.4	Full-Chip Runtime Error-Tolerant Thermal Estimation and Prediction for Practical Thermal Management	716
	<i>Hai Wang, Sheldon X.-D. Tan, Guangdeng Liao, Rafael Quintanilla, Ashish Gupta</i>	

Session 10-A Advanced Timing and Power Optimizations in Physical Design

Moderators: *Tsung-Yi Ho – National Cheng Kung Univ.*
Masanori Hashimoto – Osaka Univ.

10A.1	Gate Sizing and Device Technology Selection Algorithms for High-Performance Industrial Designs	724
	<i>Muhammet Mustafa Ozdal, Steven Burns, Jiang Hu</i>	
10A.2	Improving Dual Vt Technology by Simultaneous Gate Sizing and Mechanical Stress Optimization	729
	<i>Junjun Gu, Lin Yuan, Cheng Zhuo, Gang Qu</i>	
10A.3	The Approximation Scheme for Peak Power Driven Voltage Partitioning	736
	<i>Jia Wang, Xiaodao Chen, Chen Liao, Shiyan Hu</i>	
10A.4	Timing ECO Optimization via Bézier Curve Smoothing and Fixability Identification	742
	<i>Hua-Yu Chang, Iris Hui-Ru Jiang, Yao-Wen Chang</i>	

Session 10-B Test Cost and Quality

Moderator: *Mango Chia-Tso Chao – National Chiao Tung Univ.*

10B.1	Test-Data Volume and Scan-Power Reduction with Low ATE Interface for Multi-Core SoCs	747
	<i>Vasileios Tenentes, Xrysovalantis Kavousianos</i>	
10B.2	Post-Silicon Bug Diagnosis with Inconsistent Executions	755
	<i>Andrew Deorio, Daya Shanker Khudia, Valeria Bertacco</i>	
10B.3	On Proving the Efficiency of Alternative RF Tests	762
	<i>Nathan Kupp, Haralampos Stratigopoulos, Petros Drineas, Yiorgos Makris</i>	
10B.4	Statistical Defect-Detection Analysis of Test Sets using Readily-Available Tester Data	768
	<i>Xiaochun Yu, R.D. (Shawn) Blanton</i>	
10B.5	A Robust Architecture for Post-Silicon Skew Tuning	774
	<i>Mac Y.C. Kao, Kun-Ting Tsai, Shih-Chieh Chang</i>	

Session 10-C New Techniques for System-Level Communication**Synthesis and Hardware Metering***Moderator: Prabhat Mishra – Univ. of Florida*

10C.1	A Low-Swing Crossbar and Link Generator for Low-Power Networks-on-Chip	779
	<i>Chia-Hsin Owen Chen, Sunghyun Park, Tushar Krishna, Li-Shiuan Peh</i>	
10C.2	Exploring Heterogeneous NoC Design Space	787
	<i>Hui Zhao, Mahmut Kandemir, Wei Ding, Mary Jane Irwin</i>	
10C.3	Synchronous Elasticization at a Reduced Cost: Utilizing the Ultra Simple Fork and Controller Merging	794
	<i>Eliyah Kilada, Kenneth S. Stevens</i>	
10C.4	Robust Passive Hardware Metering	802
	<i>Sheng Wei, Ani Nahapetian, Miodrag Potkonjak</i>	