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Session 1

Monday, November 7, 2011

11:00 am – 12:30 pm:

SESSION 1:

Measurement and modelling of IC susceptibility- Part 1
(Main Hall – Violet)
Session chairs: Franco Fiori and Adrijan Baric

EMC Immunity of an Integrated Low Side Driver Circuit under Varying RF Loads
S1P1 – pp. 1-6
Hermann Nzalli[1], Christian Lautensack[2], Wolfgang Wilkening[1], Rolf Jansen[2]
[1]*Robert Bosch GmbH, Germany*
[2]*Chair of EM Theory (RWTH Aachen University), Germany*

We present EMC immunity investigations for an integrated low side driver circuit in Smart Power technology. The output (drain) voltage is monitored while it is subjected to direct power injection (DPI). DPI immunity is characterized for different load conditions. The results show that robustness significantly differs for different types of RF loads and provide a quantification. Control of the load dependence of immunity is relevant especially for IC-Pins which are connected directly to external circuitry or wiring.

Pages 1-6

Construction and Evaluation of the Susceptibility Model of an Integrated Phase-Locked Loop
S1P2 – pp. 7-12
Alexandre Boyer[1], Binhong Li[1], Sonia Ben-Dhia[1], Christophe Lemoine[1], Bertrand Vrignon[2]
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[2]*Freescale Semiconductor, Toulouse, France*

Developing integrated circuit immunity models has become one of the major concerns of integrated circuits suppliers to predict whether a chip will pass susceptibility tests before fabrication and avoid redesign process. This paper presents the development process of the susceptibility model an integrated phase-locked loop to harmonic disturbances up to 1 GHz.. The model construction is based on basic circuit information and S parameter measurements. An evaluation of the model accuracy is ensured by the characterization of internal voltage fluctuations with an on-chip sensor.

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Measurements of EMI susceptibility in ultra-low-voltage OpAmps
S1P3 – pp. 13-17
Anna Richelli
University of Brescia, Italy

With the increasing use of low voltage portable devices, analog circuits with low power consumption and ultra low voltage supply are needed. In this circuits the susceptibility to electromagnetic interferences has not deeply investigated. In this paper, the effects of interferences in an ultra low voltage CMOS amplifier designed to have high EMI immunity has been measured and the results are compared to that of an ultra low voltage commercial amplifier.

Pages 13-17

Assessment of the Radiated Immunity of Integrated Circuits in the 3 - 40 GHz Range
S1P4 – pp. 18-23
Richard Perdriau[1], Olivier Maurice[2], Soizic Dubois[2], Mohamed Ramdani[1], Etienne Sicard[3]
[1]*ESEO, France*
[2]*GERAC, France*
[3]*INSA de Toulouse, France*

This paper investigates the effects of pulsed local radiated electromagnetic injection on a custom digital integrated circuit from 3 to 40 GHz. The influence of several parameters (carrier frequency, amplitude, pulse width and period) is illustrated, discussed and compared with available results from the literature on different technologies. These experiments highlight that electromagnetic immunity weaknesses can appear in this frequency range for a relatively low injection power. Finally,some interpretations of these susceptibility phenomena are given.

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Information Leakage from the Unintentional Emissions of an Integrated RC Oscillator
S1P5 – pp. 24-28
Masahiro Kinugawa, Yu-ichi Hayashi, Takaaki Mizuki, Hideaki Sone
Tohoku University, Japan

Recently, it has been shown that electromagnetic radiation from electrical device leaks internal information. A number of studies have been conducted on measurement methods for information leakage, countermeasure technologies, and the propagation mechanism and acquisition of information via electromagnetic fields. Some investigations have shown that information leaks through the clock frequency and higher harmonic waves. Thus, previous studies have focused on the acquisition of information from the change in the amplitude of the clock signal or its harmonic signal. However, there has been little discussion about the acquisition of information by using fluctuations of the clock in the frequency domain. In this paper, we focus on the clock frequency of the integrated RC oscillators that is changed by phase noise and clarify the impact of the frequency shift on the acquisition of information.

Pages 24-28

Effects of CW interferences on a 5 GHz Monolithic VCO
S1P6 – pp. 29-34
Amable Blain[1], Jeremy Raoult[1], Adrien Doridant[1], Sylvie Jarrix[1], Tristan Dubois[2]
[1]Institut d'Electronique du Sud (IES), France
[2]Poly-Grames research center - Ecole polytechnique de Montreal, Canada;

The paper presented here is part of the electromagnetic susceptibility studies conducted on active circuits. An electromagnetic interference (EMI) is injected on an integrated voltage controlled oscillator (VCO). We describe the different effects observed on its operation mode when the circuit is subject to an EMI or high frequency signal. Three operating modes are observed. Some of them are confronted with Razavi's theory. Others highlight new phenomena in function of the aggression power.

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Session 2

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SESSION 2:

Measurement and modelling of IC susceptibility- Part 2
(Main Hall – Violet)
Session chairs: Sonia Ben-Dhia and Wolfgang Wilkening

Vertical Noise Coupling on Wideband Low Noise Amplifier from On-chip Swithing-Mode DC-DC Converter in 3D-IC
S2P1 – pp. 35-40
Kyoungchoul Koo, Sanrok Lee, Joungho Kim KAIST,
Korea, South (Republic of)

3D-IC mixed-signal systems introduce vertical noise coupling which is a new noise coupling path by near-field coupling between logic ICs and RF, analog ICs. To guarantee the performance of the system, we should be aware of the amount of the vertical noise coupling during the system design stage. This paper reports the frequency domain and time-domain measurement result of the vertical noise coupling on wideband low noise amplifier (LNA) from 200MHz on-chip switching-mode DC-DC converter in 3D-IC configuration. In the measurements from test vehicles with variations in stacking position and stack-up of the silicon substrate of the LNA, the vertically coupled noise is very serious enough to obstruct the RF receiver operation; up to 80mVpp and 500mVpp of noise are vertically coupled across each inductor
and at signal output of the LNA, respectively. The vertical noise coupling measurement results of this paper awake the seriousness of the vertical noise coupling issue in 3D-IC mixed-signal systems and can be a reference for the estimation of amount of vertical noise coupling in 3D-IC mixed-signal system design.

Pages 35-40

Novel Modeling Strategy for a BCI Set-up Applied in an Automotive Application
S2P2 – pp. 41-46
Andre Durier[1], Hugo Pues[2], Dries Vande Ginste[3]
[1]Continental Automotive France, France
[2]Melexis Technology, Belgium
[3]Ghent University, Belgium

Electronics suppliers of automotive industry use BCI (Bulk Current Injection) measurements to qualify immunity robustness of their equipment whereas electronics components manufacturers use DPI (Direct Power Injection) to qualify immunity of their component. Due to harness resonances, levels obtained during a BCI test exceed standard DPI requirements imposed by automotive suppliers onto components' manufacturers. We propose to use BCI set-up modeling to calculate the equivalent DPI level obtained at the component level during equipment testing and to compare results with DPI measurements realized at IC level.

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Internal IC Protection Structures in Relation to New Automotive Transient Requirements

S2P3 – pp. 47-52

Bernd Deutschmann, Filippo Magrini, Frank Klotz
Infineon Technologies, Germany

A huge number of complex integrated circuits can nowadays be found in modern vehicles. The undisturbed operation of the electronic control modules and systems is of vital importance for safety and reliability. Among the variety of possible interferences that can affect the normal operation of a vehicle, electrical transient disturbances are the most threatening ones. The new pulse immunity requirements defined in the latest edition of the ISO7637 standard show significant increases of pulse amplitudes. This paper briefly describes the current transient disturbance requirements for electronic systems used in the automotive environment and compares them to the current possibilities for the semiconductor industry to meet these requirements.

Pages 47-52

Accurate Prediction of EMI Induced Rectification Effects in Nonlinear Analog Circuits using Behavioral Modeling

S2P4 – pp. 53-58

Dimitri De Jonghe, Georges Gielen
K.U. Leuven, Belgium

The effects of Electromagnetic Interference (EMI) on the DC quiescent point of a circuit require expensive transient simulations due to long settling times. This paper applies behavioral modeling to accurately predict EMI induced rectification on a wide range of analog circuits. Analytical models are derived for predicting the DC voltage shifts, introduced by the interaction with EMI, over a large range of amplitudes and frequencies. The proposed methodology can be applied to numerous analog circuits that need exhaustive EM susceptibility verification using a minimal amount of measurements to extract the model parameters. The approach is validated on some basic analog building blocks.

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Comparability of RF Immunity Test Methods for IC Design Purposes

S2P5 – pp. 59-64

Sergey Miropolsky, Stephan Frei
AG Bordsysteme, TU Dortmund, Germany

In this paper the differences between DPI and BCI tests and a method, how to overcome them, are shown on the example of a simple analogue IC. An approach is shown, where comparing the test setup transfer functions is avoided, and high conformity of the results for two different tests (DPI and BCI) is observed. A virtual RF immunity test approach is proposed, which can be fast and simply implemented during IC design phase. Steady-State analysis of Mentor Graphics ELDO RF is used to model the IC under external sinusoidal RF excitation. The virtual test results show good correlation with measurements in RF range. The proposed virtual RF immunity test can easily be implemented for the IC analysis during design stage. Thus the possible failures can be found early, and IC redesign can be avoided.

Pages 59-64

Immunity Evaluation of SRAM Core Using DPI with On-Chip Diagnosis Structures

S2P6 – pp. 65-70

Takuya Sawada[1], Taku Toshikawa[1], Kumpei Yoshikawa[1], Hidehiro Takata[2], Koji Nii[2], Makoto Nagata[1]
[1]*Kobe University, Japan*
[2]*Renesas Elecronics Corporation, Japan*

A direct power injection (DPI) method evaluates the immunity of a static random access memory (SRAM) core in a 90 nm CMOS technology, with on-chip diagnosis structures of memory built-in self test (MBIST) and on-chip voltage waveform monitoring (OCM). The magnitudes of sinusoidal voltage variation introduced by DPI is quantified by OCM. The number of resultant erroneous bits as well as their distribution in the cell array are given by MBIST. The DPI, OCM, and MBIST co-operate for the immunity diagnosis of an SRAM core, as a function of power and frequency of injection. The frequency-dependent sensitivity reflects the highly capacitive nature of densely integrated memory cells.

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Session 3

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Measurement and modelling of IC emission
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Session chairs: Hugo Pues and Mohamed Ramdani

Automotive RF immunity test set-up analysis

S3P1 – pp. 71-75

Mart Coenen[1], Hugo Pues[2], Thierry Bousquet[3]
[1]*EMCMCC, The Netherlands*
[2]*Melexis NV, Belgium*
[3]*Continental, France*

Though the automotive RF emission and RF immunity requirements are highly justified, the application of those requirements in an non-intended manner lead to false conclusions and unnecessary redesigns for the electronics involved. When the test results become too dependent upon the test set-up itself, inter-laboratory comparison as well as the search for design solutions and possible correlation with other measurement methods looses ground. In this paper, the ISO bulk-current injection (BCI) and radiated immunity (RI) module-level tests are discussed together with possible relation to the DPI and TEM cell methods used at the IC level.

Pages 71-75

Measurements and Co-Simulation of On-Chip and On-Board AC Power Noise in Digital Integrated Circuits

S3P2 – pp. 76-81

Kumpei Yoshikawa[1], Yuta Sasaki[1], Kouji Ichikawa[2], Yoshiyuki Saito[3], Makoto Nagata[1,4]
[1]*Kobe University, Japan*
[2]*DENSO CORPORATION, Japan*
[3]*Panasonic Corporation, Japan*
[4]*CREST, JST, Japan*

Power noise of an integrated circuit (IC) chip is dominantly characterized by the frequency-domain impedance of a chip-package-board integrated power delivery network (PDN) and the operating frequency of circuits. A 65 nm CMOS chip embedding a high precision on-chip waveform capture clearly exhibits the relation of AC power noise components with the parallel resonation seen from on-chip digital circuits. On-chip voltage noise measured by the capturer and on-board current noise by a near-field magnetic probing technique are also experimentally related to each other, in the context of the resonance. In addition, fast power current analysis uses a capacitor charging model of digital circuits and embodies accurate co-simulation of AC power noise, along with a chip-package-board integrated PDN impedance model. A predictive measure in the design of IC chips is provided toward on-chip power supply integrity (PSI) as well as off-chip electromagnetic compatibility (EMC).

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Design and Modelling of IC-Stripline Having Improved VSWR Performance

S3P3 – pp. 82-87

Tvrtko Mandic[1,2], Renaud Gillon[2], Bart Nauwelaers[3], Adrijan Baric[1]
[1]*University of Zagreb, Croatia*
[2]*ON Semiconductors, Belgium*
[3]*K.U. Leuven, Belgium*

This paper presents models for the non-shielded IC-Stripline constructed on the FR-4 substrate. The IC-Stripline is connected through the fixture consisted of the endlaunch SMA connector and MS line. The modelling is performed with respect to the frequency and time domain measurements and lumped element model for the ICStripline is proposed. Special attention is given to the modelling of the SMA connector. The modelling of the IC-Stripline is also performed in 3D EM simulator. By changing the geometrical parameters of the IC-Stripline optimization of its RF performance is carried out. The IC-Stripline having the VSWR less than 1,2 over the frequency range of 3 GHz is presented.

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An alternative approach to model the Internal Activity of integrated circuits

S3P4 – pp. 88-92

Néstor Berbel[1], Raúl Fernández-García[1], Ignacio Gil[1], Binhong Li[2], Sonia Ben-Dhia[2], Alexandre Boyer[2]
[1]*UPC Barcelona Tech, Spain*
[2]*INSA Toulouse, France*

This paper deals with the EMC modeling of integrated circuits and the standardized model IEC 62433-2 (Integrated Circuit Emission Model – Conducted Emission).This standardized model has been applied into a basic digital circuit: a ring oscillator. This work presents an alternative approach to model the Internal Activity of any digital or analog integrated circuit, and its use has been applied on the ring oscillator. This model can be useful for modeling the effects of the power supply, electrical stress and aging in the internal activity which describes the integrated circuit conducted emissions.

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Power Supply Current Analysis of Micro-controller with Considering the Program Dependency
S3P5 – pp. 93-98
Osami Wada, Yoshiyuki Saito, Katsuya Nomura, Yukishige Sugimoto, Tohlu Matsushima
Kyoto University, Japan

To simulate power supply noise of an LSI, an EMC macro–model, LECCS-core, is under development. The LECCS-core model consists of a linear equivalent circuit and equivalent current sources. In this paper, program-dependent internal equivalent current sources are extracted for functional blocks of a microcontroller. By combining these component current sources with considering the program sequence, the power supply current is simulated both in time domain and frequency domain.Even when the LSI runs different programs with different clock frequencies, noise spectra consisting of harmonics and sub-harmonics are reproduced in good agreement with measured data.

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Session 4

On the effect of amplitude modulated EMI injected on a PLL active filter

S4P1 – pp. 170-175

Tristan Dubois[1], Jean-Jacques Laurin[1], Jérémy Raoult[2], Sylvie Jarrix[2]
[1]*Poly-Grames, Canada*
[2]*IES, France*

In this paper, the effect of an Electromagnetic Interference (EMI) modulated in amplitude on an Operational Amplifier (Op. Amp.), first as a standalone circuit and then integrated in a microwave Phase-Locked Loop (PLL) is studied. In both cases, the EMI is injected through a magnetic near field probe. First, a CW sinusoidal EMI is injected on the input tracks of the Op. Amp. alone in order to determine resonance frequencies. Then, these resonance frequencies are used as carriers to inject amplitude modulated EMI. Then, the Op. Amp. is integrated into a PLL. The susceptibility of the PLL when an EMI modulated in amplitude is injected on the Op. Amp. is carried out. Parameters of the modulated signal leading to the most sensitive perturbation effects are presented.

Pages 170-175

Low-Jitter Frequency-Modulated PLL

S4P2 – pp. 176-181

Thomas Steinecke
Infineon Technologies, Germany

Frequency modulation of a clock is a well-known and efficient way to spread clock harmonics around a center frequency, thus reducing emitted narrow-band RF energy. While smoothly changing the clock periods, modulation continuously shifts the clock edges back and forth over a time interval determined by the modulation frequency. The resulting time interval error compared to an unmodulated clock may get so large that it violates the specification of commonly used asynchronous data protocols. This paper describes a modulation technique which manages to minimize the time interval error using a single modulated PLL clock. As a prove of concept, measurement results for jitter, electromagnetic emission and CAN communication are added and discussed.

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Session 4

Tuesday, November 8, 2011

9:00 am – 10:30 am:

SESSION 4:

EMC issues in System-on-Chip, System-in-Package, smart power and wireless communications ICs
(Main Hall – Violet)
Session chairs: Georges Gielen and Jean-Michel Redouté

Improving the Immunity of Automotive ICs by Controlling RF Substrate Coupling
S4P3 – pp. 182-187
Philipp Schroeter, Stefan Jahn, Frank Klotz
Infineon, Germany

This paper discusses RF substrate coupling in automotive integrated circuits. Analyses have been accomplished by measurements on wafer level. For this purpose test structures have been designed using a technology with partial dielectric isolation for automotive applications. The determining parameters to RF substrate coupling have been evaluated by measuring passive structures. The findings are applied to an integrated circuit. It results in controlling RF substrate coupling and a circuit with a high degree of immunity against electromagnetic interferences (EMI). The paper finishes with appropriate layout recommendations.

Pages 182-187

Modeling of Simultaneous Switching Noise Effects on Jitter Characteristics of Delay Locked Loop in a Hierarchical System of Chip-Package-PCB
S4P4 – pp. 188-193
Yujeong Shim, Bumhee Bae, Koungchoul Koo, Joungho Kim
Advanced Institute of Science and Technology, Korea, South (Republic of)
A new modeling method is proposed to estimate simultaneous switching noises (SSNs) effects on clock jitter of delay locked loop (DLL) in a hierarchical system of chip, package and PCB. This method is to investigate the SSN coupling paths and effects on the clock jitter. It combines an analytical model of the circuit with a power distributed network (PDN) and interconnection models at the chip and package substrate. To validate the proposed model, DLL was fabricated using TSMC 0.18 um. It was successfully demonstrated that the experimental results are consistent with the predictions generated using the proposed model. It is confirmed that the jitter transfer function is strongly dependent on the SSN frequency and the PDN impedance profile of the chip-package hierarchical PDN.

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Investigation of Noise Coupling in Mixed-signal System-in-Packages (SiPs)

S4P5 – pp. 194-197

Hideki Sasaki[1], Tatsuaki Tsukuda[1], Yuki Fujimura[2], Tomoo Murakami[2], Hiroyuki Terai[2]
[1]*Renesas Electronics Corporation, Japan*
[2]*NEC Corporation, Japan*

Noise coupling in mixed-signal system-in-packages (SiPs) has been investigated experimentally. Four BGA types of mixed-signal SiPs consisting of a sound source LSI chip (victim) and a speaker amplifier LSI chip (aggressor) have been designed and fabricated for investigating noise coupling from a Class-D amplifier and a DCDC converter of the speaker LSI to a PLL of the sound source LSI. The two types of the SiPs stack the sound source LSI on the speaker LSI, while the other two stack the speaker LSI on the sound source LSI. The measurements of signal-to-noise ratio (SNR) for the PLL signals have demonstrated that a mixed-signal SiP stacking the noise aggressor chip on the noise victim chip is a better package configuration for avoiding noise coupling.

Pages 194-197

Modeling and Analysis of Power Supply Noise Effects on Analog-to-Digital Converter in 3DIC

S4P6 – pp. 198-202

Bumhee Bae, Yujeong Shim, Jonghyun Cho, Joungho Kim
KAIST, Korea, South (Republic of)

In this paper, the hybrid modeling and analysis of power supply noise effects on analog-to-digital converter (ADC) with chip-PCB hierarchical power distribution network (PDN) is proposed. Especially, the PDN structure, which includes power/ground Through-Silicon-Via (TSV) is modeled and analyzed for the case study of various PDN structures. The analysis was progressed with a frequency range from 1MHz to 3GHz. Analysis results indicate that ADC performance is degraded by power supply noise and it depends on PDN structures.

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Session 5

Tuesday, November 8, 2011

11:45 am – 12:30 pm:

SESSION 5:

Signal integrity and Power Integrity on PCB level
(Main Hall – Violet)
Session chairs: Davy Pissoort and Adrijan Baric

Simulation of Multiconductor Transmission Lines Using Block-Latency Insertion Method and Model Order Reduction Technique
S5P1 – pp. 203-206
Tadatoshi Sekine[1], Hideki Asai[2]
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[2]*Shizuoka University, Japan*

This paper describes a fast circuit simulation technique based on the block-latency insertion method (block-LIM) and a model order reduction (MOR) technique. The block-LIM is one of the efficient transient analysis methods adopting an explicit leapfrog finite difference method. In the block-LIM, due to duality of voltage and current variables, they are successfully separated from each other by using a staggered time step placement. Thus, each of them can be updated individually within a local block through a time stepping procedure. In this work, we build a reduced order model of the partitioned local block to improve the efficiency of the block-LIM. Compared to other circuit partitioning techniques coupled with the MOR, the order-reduced block-LIM can easily decrease whole computational costs of the transient simulation. Numerical results show that our approach is adequate for the fast simulation of tightly coupled multiconductor transmission lines.

Pages 203-206

Resonant Free PDN design®
S5P2 – pp. 207-212
Mart Coenen[1], Arthur van Roermund[2]
[1]*EMCMCC, The Netherlands*
[2]*TUE, The Netherlands*

The design of power distribution networks (PDNs) on printed circuit board (PCB) structures, or even in IC packages, typically results, with or without multilayer ceramic decoupling capacitors added, in a network which is full of resonances. By utilizing the RF terminated characteristic impedance of the adjacent supply and ground layers in parallel, a resonant free supply PDN can be achieved with a very low impedance which is flat over a extreme broad frequency range.This PDN topology in combination with “Kelvin contact” decoupled ICs, the low impedance of the PDN can be maintained as decoupling capacitors are no longer needed near to the IC pins.This has a great advantage w.r.t PCB space allocation and opens the opportunity to route signals more effectively on all layers as all decoupling elements now need to mounted at the edge of the board.By routing freedom gained, less board space and surface area required, power integrity, signal integrity and the EMC performance of the PCB application is improved at least by an order of magnitude.

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Signal integrity and Power Integrity on PCB level
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SI/PI Degradation Due to Package-Common-Mode Resonance Caused by Parasitic Capacitance between Package and PCB
S5P3 – pp. 213-218
Tohlu Matsushima, Nobuo Hirayama, Takashi Hisakado, Osami Wada
Kyoto university, Japan

Package-common-mode resonance which is caused by a parasitic capacitance and parasitic inductances between package and PCB grounds makes degradation of signal and power integrity. A parasitic capacitance between a package ground and a PCB ground anti-resonates with a parasitic inductance at ground connections such as solder balls in a BGA package. The package-common-mode resonance causes the power and/or ground bounce and increase of jitter of the output signal. According to measurement results of test boards, the resonance frequency is depend on the number of ground connection because the parasitic inductance is decreased by increasing ground connection.

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Session 6

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SESSION 6:

EMC-aware IC design and guidelines
(Main Hall – Violet)
Session chairs: Thomas Steinecke and Etienne Sicard

Evaluation of Power Supply Noise Reduction by Implementing On-Chip Capacitance
S6P1 – pp. 219-223
Hideyuki Fujii, Yoshinori Kobayashi, Toshio Sudo
Shibaura Institute of Technology, Japan

On-chip decoupling capacitor works to reduce on-chip power supply fluctuation by localizing switching current inside chip. This results in the reduction of electromagnetic interference (EMI) by preventing switching current with high frequency components flowing out from the chip. In this paper, a test chip with on-chip decoupling capacitance and noise generating circuits has been reported using CMOS 0.18 µm process. Shoot-through current generator was designed to excite impulse type noise generation. Effects of on-chip capacitance on noise reduction was evaluated by measuring the test chip as well as by using power supply noise analysis tool. Power supply noise reduction has been quantitatively evaluated by both experiment and analysis.

Pages 219-223

Impact of ESD strategy on EMC performances - Conducted Emission and DPI Immunity
S6P2 – pp. 224-229
Kamel Abouda, Patrice Besse
FREESCALE, France

In particular cases, system level stresses such as EMC stress (direct power injection, bulk current injection, and radiated field) and ESD gun stress are directly applied to the integrated circuits with no external protections [1]. Consequently, the integrated circuits have to be optimized to survive against severe external aggressions but also to ensure normal operations during the electromagnetic stress. The ESD strategy as well as the architecture of the ESD protections can significantly impact on the EMC performances. Unfortunately, the simulation of functional performances during EMC and ESD events remains very challenging for analogue products due the frequency domain and to the high injection mechanisms. This paper describes two case studies where the ESD protections significantly impact the conducted emission (CE 150ohm: first case study) and the conducted immunity (DPI: second case study) performances. Failure mechanisms will be explained and several design optimizations to overcome EMC issues will be presented. Benefits of the new design solutions will be established with the EMC test measurements.

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EMI Modeling of a 32-bit microcontroller

S6P3 – pp. 230-234

Jean-Pierre Leca[1,2], Nicolas Froidevaux[1], Henri Braquet[2], Gilles Jacquemod[2]
[1]*STMicroelectronics, France*
[2]*LEAT, France*

This paper presents a predictive SPICE model for the radiated ElectroMagnetic Interferences (EMI) of a 32-bit microcontroller. The aim of this work is to be able to predict, during the design stage, the level of electromagnetic emissions in order to establish pinout, design or layout rules. This model is intended to represent the EMI behavior of a microcontroller when it is running in a noisy mode (reading accesses to the eNVM Flash memory and CPU running). The simulated results have then been correlated with radiated emission measurements. The model has been simulated with the Eldo simulator while the measurements have been done on a 32-bit STMicroelectronics© microcontroller, following the IEC 61967-2 standard.

Pages 230-234

Intentional Electromagnetic Interference for Fault Analysis on AES Block Cipher IC

S6P4 – pp. 235-240

Yu-ichi Hayashi[1], Shigeto Gomisawa[2], Yang Li[2], Naofumi Homma[1], Kazuo Sakiyama[2], Takafumi Aoki[1], Kazuo Ohta[2]
[1]*Tohoku University*
[2]*The University of Electro-Communications*

This paper presents a new type of intentional electromagnetic interference (IEMI) which causes information leakage from cryptographic ICs (Integrated Circuits). As a recent threat, it is known that faults in cryptographic ICs such as Advanced Encryption Standard (AES) have significant influence on leakage of sensitive information. AES is a block cipher standardized by NIST (National Institute of Standards and Technology of the United States) that is a de-facto standard of smart card ICs and used for many security devices. In order to guarantee the tamper-resistance of AES hardware, this paper discusses the potential vulnerability against faults induced by IEMI via power cables. The contribution of the paper is twofold. (1) We find that, different from previous work of fault analysis, the electromagnetic (EM) faults from power cables are remotelycontrollable and lead to the leakage of the secret key. (2) We show that the random EM faults can be managed with reasonable amount of measurements and its risk to the key leakage is high enough to be a real-life threat.

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Investigation on the Susceptibility of Two-Stage Voltage Comparators to EMI
S6P5 – pp. 241-244
Franco Fiori
Politecnico di Torino, Italy

This paper deals with the susceptibility of a common CMOS voltage comparators to radio frequency interference. Specifically, the circuit topology that comprise a differential stage cascaded with a common source gain stage is considered. The detrimental effect of the RFI superimposed onto the nominal input signals is investigated through time domain computer simulations and through experiments carried out on a test chip.

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Session 7

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4:00 pm – 5:30 pm:

SESSION 7:

Tools to handle EMC at IC level
(Main Hall – Violet)
Session chairs: Bernd Deutschmann and Osami Wada

Statistical Analysis of EMI Noise Measurement for Flash Memory

S7P1 – pp. 245-250

Han-Nien Lin, Chung-Wei Kuo, Jia-Li Chang
Feng-Chia University, Taiwan, Republic of China

In this paper, we will utilize the IC-EMI measurement standards IEC 61967-2 (TEM cell method) and IEC 61967-3 (Surface scan method) with miniaturized magnetic probe to investigate the statistical behavior of EMI noise generated from Flash Memory. We will then analyze the EMI noise radiated from Flash under different operating voltages, command instructions, operating frequencies, and capacities. As to the Flash controlling mechanism, we use Microchip PIC to control Flash data access execution and then try to establish the noise budget of Flash with different measuring methods. The IC manufacturers and their customers for system applications will benefit from provision of the noise budget to realize the IC EMI characteristics in early design stage.

Pages 245-250

An On-Chip Sensor for Time Domain Characterization of Electromagnetic Interferences

S7P2 – pp. 251-256

Alexandre Boyer[1], Sonia Ben-Dhia[1], Christophe Lemoine[1], Bertrand Vrignon[2]
[1]*INSA, France*
[2]*Freescale Semiconductor, France*

With the growing concerns about susceptibility of integrated circuits to electromagnetic interferences, the need for accurate prediction tools and models to reduce risks of non-compliance becomes critical for circuit designers. However, on-chip characterization of noise is still necessary for model validation. This paper presents an on-chip noise sensor dedicated to the time-domain measurement of voltage fluctuations induced by interference coupling.

Pages 251-256

Session 7

Tuesday, November 8, 2011

4:00 pm – 5:30 pm:

SESSION 7:

Tools to handle EMC at IC level
(Main Hall – Violet)
Session chairs: Bernd Deutschmann and Osami Wada

On the Route to Full-Wave Electromagnetic Modeling with Active Circuit Element Inclusion
S7P3 – pp. 257-262
Sohrab Safavi, Jonas Ekman
Luleå University of Technology, Sweden

The possibility to combine circuit and electromagnetic modeling in one program enable new problems to be solved and more efficient simulations to be done. In this paper, the inclusion of passive and active lumped circuit elements in the Partial Element Equivalent Circuit (PEEC) method has been studied and a combined solver has been developed. The solver uses PEEC to provide an equivalent circuit for a structure, then the external passive and active lumped elements are added, and then solves the combined system providing the potential and current distributions in the structure. To demonstrate the capability of the solver, two structures are examined. Both examples include a transmission line-PEEC model and active components. Results are compared with those from OrCAD, where an analytical model for the transmission line is used. Good agreement between the results shows the feasibility of using PEEC to solve this type of mixed problems.

Pages 257-262

Poster Session

Monday, November 7, 2011

9:15am - 5:30pm:

POSTER SESSION (CAAS)
Session chairs: Vladimir Ceperic and Georges Gielen

Impact of GND-PTH Stitches in DDR3/GDDR3/GDDR5 Memory Controller Packages

PP1 – pp. 99-104

Hany Hussein Ahmad, Amolak Badesha
Agilent Technologies Inc., United States of America

DDR3 and GDDR3/5 memory technology running in the Giga-bit range require 3D EM accurate modeling of RF phenomena such as the impact of GND-PTH stitches (Ground Plated Through Hole) used to connect reference ground-planes in the Memory controller packages (MCH-PKG). Cost-reduction requires minimizing the number of layers and vias on MCH-PKG (micro-vias and PTH). Layout-Designers usually revert to reduce the GND-PTH without studying the impact on the performance. In this paper, Method of Moments (MoM) is used to study the impact of GND-PTH on data eye-opening as well as on Radiated-Emission of a DDR3 two-SODIMMs/channel running at 1.33GB/s.

Pages 99-104

Electromagnetic Susceptibility of low frequency bipolar transistors subject to the total ionizing dose effect

PP2 – pp. 105-110

Adrien Doridant[1,2], Jeremy Raoult[1], Amable Blain[1], Patrick Hoffmann[3], Nathalie Chatry[2], Phillipe Calvel4, Sylvie Jarrix[1], Laurent Dusseau[1]
[1]*Institut d'Electronique du Sud (IES), France*
[2]*TRAD, France*
[3]*CEA / DAM/CEG, France*
[4]*Thales Alenia Space, France*

Space or military electronic devices are subject to both electromagnetic fields and total ionizing dose. The reliability of a discrete low frequency transistor is addressed by means of electromagnetic susceptibility measurements after total ionizing dose. The bipolar transistors under test are subject to high frequency interferences in the near-field zone with 100 MHz – 1.5 GHz signals. For comparison, the electromagnetic susceptibility is investigated on both non-irradiated and irradiated transistors mounted in a common emitter configuration. The goal is to predict the reliability of simple devices on a mission time scale.

Pages 105-110

Poster Session

Monday, November 7, 2011

9:15am - 5:30pm:

POSTER SESSION (CAAS)
Session chairs: Vladimir Ceperic and Georges Gielen

Automated Decoupling Capacitor Analysis for Analog/Digital Printed Circuit Boards

PP3 – pp. 111-114

Denis Soldo, Steven, G Pytel Jr
ANSYS, Inc, United States of America

With faster switching, lower supply voltages and the need for portable products are placing new demands for signal, power integrity and EMI. This paper discuses the challenges with advanced printed circuit board design and describes an automated decoupling capacitor analysis for analog and digital printed circuitry boards. The genetic algorithm (GA) will be used in optimization and selection of the appropriate number and types of decoupling capacitors for pre-defined power/ground noise printed circuit board specification. This automatic technique provides an innovative simulation strategy that significantly improves engineering productivity by automating decoupling capacitor selection, placement and optimization for printed circuit boards.

Pages 111-114

Enhancing Engineers Skills in EMC of Integrated Circuits

PP4 – pp. 115-118

Etienne Sicard, Alexandre Boyer
INSA, France

This paper presents the strategies used for effective training of engineers in integrated circuit (IC) design under Electromagnetic Compatibility (EMC) constraints. It presents the general context of EMC of ICs and details the EMC-aware IC design course given in companies and several institutes in France. Collaborations with industry have produced a set of learning resources and design tools to support the development of industry relevant EMC skills and lifelong learning skills. The courses enable students to learn about EMC measurements and modeling at IC level and their implications using a set of user friendly tools. The courses taught in university and in industry have consistently produced high levels of student/engineer satisfaction.

Pages 115-118

Poster Session

Monday, November 7, 2011

9:15am - 5:30pm:

POSTER SESSION (CAAS)
Session chairs: Vladimir Ceperic and Georges Gielen

IP Core to Leverage RTOS-Based Embedded Systems Reliability to Electromagnetic Interference
PP5 – pp. 119-124
Fabian Vargas[1], Dhiego Silva[1], Letícia Poehls[1], Jorge Semião[2], Isabel Teixeira[3], João Paulo Teixeira[3], María Valdés[4], Judit Freijedo[4], Juan-José Rodríguez-Andina[4]
[1]*Catholic University - PUCRS, Brazil*
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[3]*INESC-ID Lisboa,Portugal*
[4]*University of Vigo, Spain*

The use of Real-Time Operating Systems (RTOSs) became an attractive solution to simplify the design of safety-critical real-time embedded systems. Due to their stringent constraints such as battery-powered, high-speed and low-voltage operation, these systems are often subject to transient faults originated from a large spectrum of noisy sources, among them, the conducted and radiated Electromagnetic Interference (EMI). As the major consequence, the system's reliability degrades. In this paper, we present a hardware-based intellectual property (IP) core, namely RTOS-Guardian (RTOS-G) able to monitor the RTOS' execution in order to detect faults that corrupt the tasks' execution flow in embedded systems based on preemptive RTOS. Experimental results based on the Plasma microprocessor IP core running different test programs that exploit several RTOS resources have been developed. During test execution, the proposed system was exposed to conducted EMI according to the international standard IEC 61.000-4-29 for voltage dips, short interruptions and voltage transients on the power supply lines of electronic systems. The obtained results demonstrate that the proposed approach is able to provide higher fault coverage and reduced fault latency when compared to the native fault detection mechanisms embedded in the kernel of the RTOS.

Pages 119-124

Poster Session

Monday, November 7, 2011

9:15am - 5:30pm:

POSTER SESSION (CAAS)
Session chairs: Vladimir Ceperic and Georges Gielen

Towards Nonlinearity Measurement and Simulation Using Common EMC Equipment

PP6 – pp. 125-130

Sjoerd Op 't Land[1], Richard Perdriau[1], Mohamed Ramdani[1], Frédéric Lafon[2]
[1]*Groupe ESEO, France*
[2]*VALEO GEEDS, France*

Integrated circuit (IC) models that predict functional failure are necessary for predicting the immunity of systems to electromagnetic interference (EMI). The integrated circuit immunity model for conducted immunity (ICIM-CI) of IEC 62433-4 assumes that the IC terminals still behave linearly at injection power levels that cause susceptibility. This hypothesis should be systematically verified when modelling integrated circuits for EMC, but this is not always straightforward. A simple measurement set-up using a directional coupler and a spectrum analyser is demonstrated to verify this linearity hypothesis using commonly available equipment. The measured reflected spectrum can be transformed into the X11 parameter, which is the non-linear extension of the S11 parameter. X-parameters may be the key to predict susceptibility by simulation when the linearity hypothesis is invalid.

Pages 125-130

High speed electronics on Printed Circuit Board Characterisation of embedded capacitors and resistors

PP7 – pp. 131-136

Serpaud Sebastien[1], Séreirath Tran[2], Yannick Poiré[1], Thomas Cotxet[3]
[1]*Nexio, France*
[2]*Airbus Operations SAS, France*
[3]*CIREP, France*

This article deals with evaluating complex high speed electronic board whose Printed Circuit Board (PCB) implements embedded capacitors and resistors. Electrical performance of embedded and discrete components is compared thanks to measurements and simulations. Several test boards will be developed in order to analyze functional and non-functional electrical performances.

Pages 131-136

Poster Session

Monday, November 7, 2011

9:15am - 5:30pm:

POSTER SESSION (CAAS)
Session chairs: Vladimir Ceperic and Georges Gielen

Local ElectroMagnetic Coupling with CMOS Integrated Circuits

PP8 – pp. 137-141

Francois Poucheret[1,3], Laurent Chusseau[2], Bruno Robisson[3], Philippe Maurine[1]
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[2]*IES, France*
[3]*CEA, France*

This paper gives experimental evidences of how a local electromagnetic coupling can be created between a micro-antenna and the buried Power Ground Network (PGN) of a 350nm VLSI circuit; the PGN being integrated in Metal 1, the deepest metal layer available in the considered technology. The local EM injection method applied to create this coupling is introduced in this paper even if it presents some similarities with direct power injection.

Pages 137-141

Conducted EMI of Integrated Switching Audio Amplifier for Mobile Phone Applications

PP9 – pp. 142-147

Salah-Eddine Adami[1], Roberto Mrad[1], Florent Morel[1], Christian Vollaire[1], Gaël Pillonnet[2], Rémy Cellier[2]
[1]*University of Lyon, Ecole Centrale de Lyon, Ampere Laboratory*
[2]*University of Lyon, CPE Lyon, Lyon Institute of Nanotechnology*

In this paper, conducted EMI measurements of two integrated Class D audio amplifiers are realized using the EN55022 standard, in order to compare the EMI behavior of two modulation techniques. The first circuit uses a carrier-based pulse-width modulation (PWM) and the second uses a self-oscillating modulation based on slidingmode (SM) control. Measurement results show that SM circuit has better EMI behavior compared to PWM circuit, thanks to spread spectrum effect of the SM circuit. Spice simulations using full transistor circuit model are realized to evaluate the range of validity of the used model in large frequencies. Simulation results are very closed to the measurement ones, especially for low and medium frequencies (up to 10 MHz).

Pages 142-147

Poster Session

Monday, November 7, 2011

9:15am - 5:30pm:

POSTER SESSION (CAAS)
Session chairs: Vladimir Ceperic and Georges Gielen

EMC-signatures of microcontrollers under thermal stress analyzed by FSV
PP10 – pp. 148-152
Jos Knockaert[1], Davy Pissoort[2], Mohamed Ramdani[3], Mohamed Malki[4], David Baudry[4]
[1]*University College of West Flanders, Belgium*
[2]*FMEC - KHBO, Belgium*
[3]*Groupe ESEO, France*
[4]*IRSEEM, France*

The EMC-signature of devices containing microcontrollers can differ due to thermal or mechanical stress. Research is presented to prove the feature selective validation method (FSV) to be sensitive enough to analyze differences in signatures.

Pages 148-152

Investigation on DPI Effects in a Low Dropout Voltage Regulator
PP11 – pp. 153-158
Jianfei Wu[1], Etienne Sicard[2], Amadou Cissé Ndoye[2], Frédéric Lafon[3], Jiancheng Li[1], Rongjun Shen[1]
[1]*School of Electronic Science and Engineering, China*
[2]*INSA, France*
[3]*VALEO VECS, France*

In this paper, the susceptibility of a low dropout voltage regulator (LDO) in direct RF power injection (DPI) is analyzed by measurements and simulation. The measurements highlight the offset in the output induced by the conducted RF disturbances and various failure modes. Discrete components used in the injection path and test board are modeled based on impedance measurements. DPI simulations using simple and complex models are presented, which highlight the strongly nonlinear behavior of the circuit even at low levels of power injection. The relationship between DPI results and the structure of the bandgap circuits and operational amplifier are also analyzed.

Pages 153-158

Poster Session

Monday, November 7, 2011

9:15am - 5:30pm:

POSTER SESSION (CAAS)
Session chairs: Vladimir Ceperic and Georges Gielen

Fast Conducted EMI Prediction Models for Smart High-Side switches

PP12 – pp. 159-164

Wim Teulings, Bertrand Vrignon
Freescale semiconductors, France

Fast frequency domain models are presented allowing prediction of conducted EMI levels generated by a smart High-Side Switch on Printed Circuit Board in a typical automotive lighting application. The influence of design parameters such as switching speed, wiring length and decoupling capacitors can be evaluated without having to perform a Fast Fourier Transform (FFT). Thanks to the high execution speed of these models, insight in a particular design layout can be gained. Moreover, the design can be optimized by performing simulations under various conditions.

Pages 159-164

On-chip Power Integrity Evaluation System

PP13 – pp. 165-169

Yoshitaka Nabeshima, Yoshiaki Oizono, Toshio Sudo
Shibaura Institute of Technology, Japan

Power supply disturbance excited by simultaneous switching output (SSO) circuits or core circuits is a serious issue in a system-in-package (SIP), especially in 3D stacked die package, because much more I/O circuits and core circuits excited simultaneously in synchronized with clock edges than the case of single die package.Therefore, decoupling schemes in such SiP's must be carefully designed including on-chip capacitance as well as off-chip capacitance so as to reduce the impedance of power distribution network (PDN) as low as possible up to high frequency range. In this paper, an on-chip power integrity evaluation system has been established using a test chip with both noise generating circuits and monitoring circuits for on-chip power supply noise. On-chip power integrity has been examined and compared for the cases with and without on-chip capacitance and for the various embedded capacitors inside an interposer.

Pages 165-169