# 2011 International SoC Design Conference

# (ISOCC 2011)

## Jeju, South Korea
## 17 – 18 November 2011

IEEE

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with amplitude and phase imbalance less than 0.1dB and 0.34 degrees respectively over the 55-66GHz frequency band.



## Session 2 High-Speed and Power-Aware Circuit Techniques for Future Integrated Systems

13:30-15:00 / Room A

Special Session

**Chair** Tetsuya Iizuka (University of Tokyo, Japan)

### Abstract

High-speed communication techniques continue to demand advances in CMOS technologies for both wireless and wireline applications. At the same time, the power challenge is another concern especially for the mobile and medical applications and the energy-efficient systems must be optimized to maintain low-energy and high-throughput operations simultaneously. This special session presents several state-of-the-art circuit components and systems for high-speed communications and robust

power-aware circuits. The first paper presents a 60-GHz direct-conversion transceiver which realizes IEEE802.15.3c compliant full-rate wireless communication, and the second paper proposes a low-phase-noise ring-VCO-based frequency multiplier with a new sub-harmonic direct injection locking technique. Then, a 16Gbps laser-diode driver based on a bandwidth enhancement technique with mutually-coupled inductor is presented in the third paper. The fourth paper introduces the ultra-low power reference circuit design techniques to realize energy-efficient robust low-voltage sub-threshold digital circuit, and the last paper proposes a novel charge pump circuit that can generate higher output voltage than the breakdown voltage to enable an integration of the MEMS and CMOS technologies.

## Session 3 Implementation of Low-Density Parity-Check Code

13:30-15:00 / Room B

Special Session

**Chair** Jin Sha (Nanjing University, China)


### Abstract

In digital communication and information theory, forward error correction (FEC) is a system of error control for data transmission, whereby the sender adds systematically generated redundant data to its messages, also known as an error-correcting code (ECC). Recently, there has been a great research activity in the field of FEC achitectures. Some near-optimal (near-Shannon limit) error correction codes, such as Low-Density Parity-Check (LDPC) codes, have become one of the most attractive topics of interest in both academia and industry. The study on efficient Very Large Scale Integration (VLSI) design for LDPC decoding is a hot research filed and is essential for practical applications. The Special Invited Session on ISOCC aims to present latest's advances in LDPC architectures.

## Session 4 Data converter

13:30-15:00 / Room C

Regular Session

**Chair** Kwang Hyun Baek (Chung-Ang Unviersity, Korea)
**Co-Chair** Tae Wook Kim (Yonsei University, Korea)

## Session 5 SoC Design Methodology

13:30-15:00 / Room D

Regular Session

**Chair** Sang Bock Cho (Ulsan Unviersity, Korea)
**Co-Chair** Tae Hwan Kim (Seoul National Unviersity, Korea)

## Session 6 RF Front-end Circuits for SOC and SIP

15:30-17:00 / Room A

Special Session

**Chair** Shawn S. H. Hsu (National Tsing Hua University, Taiwan)


### Abstract

The RF front-end circuits are of extreme importance to the overall system performance of wireless communication ICs. Continuous innovation of technology makes it possible to realize a wireless communication transceiver with a small form factor, low cost, and under low power consumption. In this special session, the design techniques and considerations of several critical RF circuit blocks in typical RF transceivers are reported and discussed, including the low-noise amplifier (LNA), frequency multiplier, mixer, and voltage-controlled oscillator (VCO). These circuits are implemented in a wide variety of advanced technologies such as CMOS, III-V heterojunction bipolar transistors (HBT), and integrated passive device (IPD). With the general design goals for achieving low power operation within a compact chip area, the design concepts are suitable for both system-on-chip (SOC) and system-in-package (SIP) applications.

## Session 7 Three-dimensional Stacking: Theories, Tools and Tapeouts

15:30-17:00 / Room B

Special Session

**Chair** Yiyu Shi (Missouri University of Science and Technology, USA)
**Co-Chair** Shih-Chieh Chang (National Tsing Hua University, Taiwan)

### Abstract

Three-dimensional integrated circuits have generally considered to be the most promising technique beyond the limit of device scaling. They provide smaller footprint, higher integration density and compatibility with current CMOS technology, and they allow heterogeneous integration. Yet many design challenges need to be addressed to attain those benefits. The first talk in the session presents the early design planning and exploration for 3D ICs based on virtual 3D placement. The second and third talks present the TSV reliability in various physical design stages, and its enhancement through different techniques, The fourth talk discusses about the lower power design, an essential component to reduce thermal stress in 3D ICs. The session is concluded with a real 3D design presented by industry experts for 3D stacking study.

## Session 8 SoC Testing/Verification/Signal Integrity

15:30-17:00 / Room C

Regular Session

**Chair** Young Hwan Kim (Pohang University of Science and Technology, Korea)
**Co-Chair** Byeong Min (Samsung Electronics)

## Session 9 Low Power Design Techniques

15:30-17:00 / Room D

Regular Session

**Chair** Kyung Ki Kim (Daegu University, Korea)

# Friday, November 18, 2011

## Session 10 Architectural Reconfiguration and Customization for Embedded Systems

08:20-09:50 / Room A

Special Session

**Chair** Hiroyuki Tomiyama (Ritsumeikan University, Japan)


### Abstract

Reconfigurable/customizable architectures are attracting great interesting the embedded systems industry for their high energy/performance efficiency and flexibility. This special session focuses on reconfiguration/customization of processor architectures and accelerators for embedded systems. The session starts with a brief review of research trends in this field. The second talk presents a reconfigurable processor which enables easy optimization of the performance/cost trade-off. The third talk describes a vector co-processor architecture which was customized for embedded applications. The fourth talk presents a design exploration methodology for reconfigurable address generation units of embedded processors. Finally, hardware multitasking techniques are presented for dynamically partially reconfigurable devices.

## Session 11 Microprocessor and DSP Architectures

08:20-09:50 / Room B

Regular Session

**Chair** Hanho Lee (Inha University, Korea)

## Session 12 RF Techniques

08:20-09:50 / Room C

Regular Session

**Chair** Yun Seong Eo (Kwangwoon University)

## Session 13 mm Wave Circuits and Systems

08:20-09:50 / Room D

Regular Session

**Chair** Jinwook Burm (Sogang University)

## Session 14 Display Drivers and Multimedia SoCs

13:30-14:30 / Room A

Regular Session

**Chair** Hi Seok Kim (Chongju University, Korea)

## Session 15 Analog Techniques

13:00-14:30 / Room B

Regular Session

**Chair** Yong Moon (Soongsil University, Korea)

## Session 16 Design, Analysis and Tools for Integrated Circuits and System

13:00-14:30 / Room C

Special Session

**Chair** Ka Lok Man (Xi'an Jiaotong-Liverpool University, China)


### Abstract

DATICS Workshops were initially created by a network of researchers and engineers both from academia and industry in the areas of Design, Analysis and Tools for Integrated Circuits and Systems. The proposed 11th DATICS workshop/special session, DATICS-ISOCC'11, will focus on emerging Circuits and Systems (CAS) topics that will strongly lead human life revolutions, especially in CMOS technologies, communication technologies and biomedical technologies. Human life revolutions come along with economic opportunities. The market for these emerging topics is also forecast to grow to a multi-billion dollar market in the coming decade.The workshop/special session will highlight the potential and current developments of these CAS topics, along with pressing challenges. The proposed workshop/special session is coherent and complementary to the conference theme ("SoC Design for Future Living") and areas of interest of ISOCC. The main target of DATICS-ISOCC'11 is to bring together engineering researchers and people from industry to exchange theories, ideas, techniques and experiences.

## Session 17 Advances in CMOS Circuits and Carbon-Based Electronics

13:00-14:30 / Room D

Special Session

**Chair** Volkan Kursun (Hong Kong University of Science and Technology, Hong Kong)


### Abstract

Transistor made with individual single walled carbon nanotubes (SWNTs) exhibit impressive characteristics. However, although carbon nanotubes have been actively studied for electronics applications (particularly for CMOS replacement) during the past 2 decades, practical applications are still very limited because SWNT technologies are plagued by a number of problems, such as separation of semiconductor specimens from the metallicones, alignment and organization with high densities, contact reproducibility for transistors, etc. The field of carbon nanotubes is progressively evolving towards gas sensing and flexible electronics applications which are much less demanding than advanced integrated circuits (ICs) in terms of device characteristics and integration density. On the other hand, graphene which has been isolated only 7 years ago seems to be more promising, in particular for ICs, as well as for large area transparent conducting film applications. In this session, we shall briefly review some basic properties of these two emblematic materials and present some recent advances concerning their use. In particular, we will show how the two fields are entangled, i.e., how graphene can improve some of the properties of carbon nanotube devices, and how carbon nanotubes can be employed as precursors for the fabrication of graphene nanoribbons. Future carbon-based devices and circuits will probably make extensive use of combinations of these two exceptional materials.

## Session 18 Communication SoCs

15:00-16:30 / Room C

Regular Session

**Chair** Sang Hoon Hong (Kyung Hee University, Korea)
**Co-Chair** Norbert When (University of Kaiserslautern, Germany)

## Session 19 Power Management and Energy Harvesting

15:00-16:30 / Room D

Regular Session

**Chair** Hyunchol Shin (Kwangwoon University, Korea)

# Poster Session

ISOCC2011

Nov. 18, 2011 / 13:00-16:30 / Lobby

**Chair** Kee-Won Kwon (Sungkyunkwan University)