2011 IEEE 9th International Conference on ASIC

(ASICON 2011)

Xiamen, China 25 – 28 October 2011

Pages 1-550



IEEE Catalog Number: CFP11442-PRT **ISBN:**

978-1-61284-192-2

Technical Session Index

SESSION 1A

VLSI Design and Circuits (I)

1A-2	A Behavior-based Reconfigurable Cache for the Low-power Embedded Processor Jiongyao Ye, Jiannan Jin, Tabkahiro Watanabe (Waseda University, Japan)	1
1A-3	A Novel Method for Storage Architecture of Pipeline FFT Processor Ting Zhang, Lan Chen, Yan Feng (Chinese Academy of Sciences, China)	6
1A-4	Design of Resistant DPA Three-valued Counter Based on SABL Yuejun Zhang (Ningbo University, China), Pengjun Wang(Fudan University, China), Lipeng Hao(Ningbo University, China)	9
1A-5	Improvement of Adiabatic Domino Circuits and its Application in Multi-valued Circuits Qiankun Yang ,Pengjun Wang, Fengna Mei (Ningbo University, China),	13
1A-6	Low Power Shift Registers for Megabits CMOS Image Sensors Jinn-Shyan Wang, Tsung-Han Hsieh, Keng-Jui Chang, and Chingwei Yeh (Chung-Cheng University, Taiwan)	17
1A-7	High-parallel LDPC decoder with power gating design Ying Cui1, Xiao Peng, Yu Jin, Peilin Liu, Shinji Kimura, Satoshi Goto (Waseda University)	21
1A-8	A Reconfigurable Macro-Pipelined DCT/IDCT Accelerator Wenqi Bao, Jiang Jiang, Qing Sun, Yuzhuo Fu (Shanghai Jiao Tong University, China)	25

SESSION 2A

VLSI Design and Circuits (II)

2 A-1	Scheduling to Timing Optimization for a Novel High-level Synthesis Approach	29
	Ling Li, Teng Wang, Ziyi Hu Xin'an Wang, Xu Zhang(Peking University Shenzhen	
	Graduate School, China)	

2A-2	High Reliable Digital Signal Processor for Automotive Application Yimiao Zhao, Zhigang Ni (Beijing Design Center, Analog Devices, China)	33
2A-3	A Novel Differential Fault Analysis on AES-128 Pengjun Wang(Fundan University, Shanghai 201203, China, Ningbo University, China), Lipeng Hao (Ningbo University, China)	35
2A-4	Saving 78.11% Dhrystone power consumption in FPU by clock gating while still keeping co-operation with CPU Minh Thien Trieu, Huong Thien Hoang, Phong The Vo, Hung Bao Vo(Renesas Design Vietnam Company Ltd., Vietnam, Renesas Electronic Corporation Tokyo, Japan),Yoichi Yuyama(Renesas Electronic Corporation Tokyo, Japan)	39
2A-5	A hardware/software co-design approach for multiple-standard video bitstream parsing Sha Shen, Huibo Zhong, Yibo Fan, Xiaoyang Zeng(Fudan University, China)	43
2A-6	ADDLL/VDD-Biasing Co-design for Process Characterization, Performance Calibration, and Clock Synchronization in Variation-Tolerant Designs Jinn-Shyan Wang, Yung-Chen Chien, Jia-Hong Lin, Chun-Yuan Cheng, Ying-Ting Ma, Chung-Hsun Huang(Chung-Cheng University, Taiwan)	47
2A-7	Analysis of Adaptive Support-Weight Based Stereo Matching for Hardware Realization Junbao Liu, Shuai Wang, Yang Li, Jun Han, Xiaoyang Zeng(FudanUniversity, China)	51
2A-8	A High Performance Sound Source Localization System based on Macro-pipelined Architecture Qing Sun, Yuzhuo Fu, Wenqi Bao, Jiang Jiang(Shanghai Jiao Tong University, China)	55

SESSION 3A

VLSI Design and Circuits (III)

3 A-1	Research on Design of A Reconfigurable Parallel Structure Targeted at LFSR	59
	Wei Li(the Information Engineering University, China), Xuan	
	Yang(Jiangnan Institute of Computing Technology, China), Zibin Dai(the	
	Information Engineering University, China)	
3A-2	Using NOC technology to improve Photoelectric Encoder system for LAMOST	65
3A-2	spectroscopes	
	Zhongyi Han(Chinese Academy of Sciences, China, Chinese Academy of	

	Sciences, China, Graduate University of Chinese Academy of Sciences, China), Jianing Wang(Chinese Academy of Sciences, China, Chinese Academy of Sciences, China), Yizhong Zeng(Chinese Academy of Sciences, China, Chinese Academy of Sciences, China), Zhongwen Hu(Chinese Academy of Sciences, China, Chinese Academy of Sciences, China)	
3A-3	A New Configurable Logic Block with 4/5-input Configurable LUT and Fast/Slow-Path Carry Chain Zhidong Mao, Liguang Chen, Yuan Wang, Jinmei Lai(Fudan University,	67
3A-4	China) A 768 Megapixels/sec Inverse Transform With Hybrid Architecture For Multi-Standard Decoder Tuan Minh Phan Ho, Thang Minh Le, Khanh Duy Vu(Renesas Design Vietnam Company, Ltd, Vietnam) Seiji Mochizuki, Kenichi Iwata, Keisuke Matsumoto, Hiroshi Ueda(Renesas Electronics Corporation, Japan)	71
3A-5	A Two-way Parallel CAVLC Encoder for 4Kx2K H.264/AVC Huibo Zhong, Sha Shen, Yibo Fan, Xiaoyang Zeng(Fudan University, China)	75
3A-6	Multi-Stage Power Gating Based on Controlling Values of Logic Gates Yu JIN(Waseda University, Japan), Shinji KIMURA	79
3A-7	A High Speed Reconfigurable Face Detection Architecture Weina Zhou(Fudan University, China, Shanghai Maritime University, China), Yao Zou, Lin Dai, Xiaoyang Zeng((Fudan University, China)	83
3A-8	A Coarse-grained Reconfigurable Computing Unit Kanwen Wang, Shuai Chen, Wei Cao, Lingli Wang(Fudan University, China)	87

SESSION 1B

Power Management ICs

1 B- 1	Battery State of Charge Estimation using Adaptive Subspace Identification					
	Method(invited paper)					
	Sahana Swarup, Sheldon X. – D. Tan, Zao Liu, Hai Wang(University of					
	California, Riverside, USA), Zhigang Hao, Guoyong Shi (Shanghai Jiao Tong					
	University, China)					

1B-3	A New Frequency Compensation Scheme for Current-Mode DC/DC Converter Jiake Wang, Jinguang Jiang, Shanshan Li, Xu Gong, Xifeng Zhou ,Qingyun Li(Wuhan University , China)	95
1B-4	A High-Performance PWM Controller with Adjustable Current Limit Zekun Zhou, Huifang Wang, Xin Ming, Bo Zhang(University of Electronics Science and Technology of China, China), Yue Shi(Chengdu University of Information Technology, China, University of Electronics Science and Technology of China, China)	100
1B-5	A Capacitor-Free, Fast Transient Response CMOS Low-Dropout Regulator with Multiple-Loop Control Xiao Tang, Lenian He(Zhejiang University, China)	104
1B-6	A High Efficiency Current Mode Step-Up/Step-Down DC-DC Converter With Smooth Transition Yanzhao Ma, Jun Cheng, Guican Chen(Xi'an Jiaotong University, China)	108
1 B-7	A Non-Rectifier Wireless Power Transmission System Using On-Chip Inductor Yimeng Zhang, Mengshu Huang, Tsutomu Yoshihara (Waseda University, Japan)	112

SESSION 2B

Analog Techniques (I)

3D 1	An Overview of Charge Pumping Circuits for Flash Memory Applications(invited	116
2B-1	paper)	
	Oi-Ying Wong, Hei Wong, Wing-Shan Tam, and Chi-Wah Kok(City	
	University of Hong Kong, Hong Kong)	
a D a	Charles A.D. CMOS Is (free 1/4 (free)) and A.D. southed	130

2B-2Class-AB CMOS buffer with floating class-AB control120Peng Zhang, Fan Ye,Junyan Ren(Fudan University, China)

2B-4	A New Topology for Fully Differential Amplifiers that Enhances Their Tolerance to							124					
2D-4	External D	Disturbar	ıces										
	Guoyuan	Fu1*,	Н.	Alan	Mantooth1,	Jia	Di(University	of	Arkansas,				
	Fayettevil	le, USA)										

- 2B-6
 Double charge pump circuit with triple charge sharing clock scheme
 128

 Mengshu Huang, Yimeng Zhang, Hao Zhang ,Tsutomu Yoshihara(Waseda University, Japan)
 128
- 2B-7CMOS Charge Pump with Separated Charge Sharing for Improved Boosting133Ratio and Relaxed Timing RestrictionSeung-Jae Choi(Sungkyunkwan University, Korea, Samsung Electronics,
Korea) Young-Hyun Jun(Samsung Electronics, Korea), Bai-Sun
Kong(Sungkyunkwan University, Korea)

SESSION 3B

Analog Techniques for Sensor Signal Conditioning

3B-2	ROIC with Adaptive Reset Control for Improving Dynamic Range of IR FPAs(invited paper) Doohyung Woo(The Catholic University of Korea, Korea), Ilku Nam, Joonwoo Choi(Pusan National University, Korea)	137
3B-3	A Signal Conditioner IC for Inductive Proximity Sensors Huang Wengang(SISC, China, UESTC, China), Wang Chenghe, Liu Luncai, Huang Xiaozong, and Wang Guoqiang(SISC, China)	141
3B-4	A Low-power Low-noise Amplifier for EEG/ECG Signal Recording Applications Jinghao Feng,Na Yan,Hao Min(Fudan University, China)	145

3B-6	A TIA-based Interface for MEMS Capacitive Gyroscope						
	Tao Yin, Huanming Wu, Qisong Wu, Haigang Yang(Chinese Academy of						

SESSION 1C

Application-Specific SoCs (I)

1C-1	A Multi-level Arbitration and Topology Free Streaming Network for Chip Multiprocessor(invited paper) Jian Wang, Andreas Karlsson, Joar Sohl, Magnus Pettersson , Dake Liu(Department of Electrical Engineering Link [°] oping University, Sweden)	153
1C-2	Design and Verification of an Application-Specific PLD Using VHDL and SystemVerilog(invited paper) Jae-Jin Lee(Electrionics and Telecommunications Reaserch Institute, Deajeon, Korea), Young-Jin Oh, Gi-Yong Song(School of Electronics engineering College of Electrical and Computer Engineering, Korea)	159
1C-3	Evaluation of Deflection Routing on Various NoC Topologies Chaochao Feng, Jinwen Li, Minxuan Zhang(School of Computer, National University of Defense Technology, China) ,Zhonghai Lu, Axel Jantsch(Department of Electronic Systems, Royal Institute of Technology, Sweden)	163
1C-4	ASIC Implementation of an OFDM Baseband Transceiver for HINOC Hongming Chen(Shanghai Research Institute of Microelectronics (SHRIME), Peking University, China), Xiaoyuan Chen, Tie Liu , Yuhua Cheng(Shanghai Bwave Technology Co., Ltd Shanghai, China)	167
1C-5	Design of Four-Transistor Pixel for High Speed CMOS Image Zhou Yangfan, Cao Zhongxiang, Li Quanliang, Qin Qi, Wu Nanjian(State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, China)	171
1C-6	A Network-on-Chip Simulation Framework for Homogeneous Multi-Processor System-on-Chip Yuan Wen Hau, M. N. Marsono, Chia Yee Ooi, M. Khalil-Hani(VeCAD Research Laboratory Faculty of Electrical Engineering, Universiti Teknologi Malaysia.Malaysia.)	175

SESSION 2C

Application-Specific SoCs (II)

2C-1	Design of a Signal Processing Circuit for Quartz Crystal Microbalance Biosensors(invited paper)	180
	Shih-Chang Chang(Department of Electrical Engineering, National University of Tainan, Taiwan), I-Jen Chao, Bin-Da Lin(Department of Electrical Engineering, National Cheng Kung University, Taiwan), Chun-Yueh Huang(Department of Electrical Engineering, National University of Tainan, Taiwan), Mei-Hwa Lee(Department of Materials Science and Engineering, I-Shou University, Taiwan), Hung-Yin	
	Lin(Department of Chemical and Materials Engineering, National University of Kaohsiung, Taiwan)	
2C-2	A Low-power 433MHz Transmitter for Battery-less Tire Pressure Monitoring System	184
	inyu Zhu, Liji Wu, Xiangmin Zhang, Chen Jia, Chun Zhang(Tsinghua National Laboratory for Information Science and Technology Institute of Microelectronics, Tsinghua University, Beijing. China)	
2C-3	A High Performance and Low Cost Video Processing SoC for Digital HDTV Systems Longjun Liu, Hongbin Sun, Wenzhe Zhao, Zuoxun Hou, Jingmin Xin, Nanning Zheng(School of Electronics and Information Engineering, Xi'an Jiaotong University, China)	188
2C-4	A Novel Hardware Prefetching Scheme Exploiting 2-D Spatial Locality in Multimedia Applications Jin Huang, Jing Xie, Zhigang Mao(School of Microelectronics, Shanghai Jiao Tong University, China Building of Microelectronics, China)	192
2C-5	A NoC-based Multi-core Architecture for IEEE 802.11i CCMP Yang Li, Jun Han, Shuai Wang, Junbao Liu and Xiaoyang Zeng(State-Key Lab of ASIC and System, Fudan University, China)	196
2C-6	A Method of Quadratic Programming for Mapping on NoC Architecture Jiayi Sheng, Liulin Zhong, Ming'e Jing, Zhiyi Yu, Xiaoyang Zeng(State Key Laboratory of ASIC & System, Fudan University, Shanghai, China)	200
2C-7	A Channel Estimator for LTE Downlink Mapped on a Multi-Core Processor Platform	204
	Maofei He, Jiajie Zhang, Wenhua Fan, Zhiyi Yu, Xiaoyang Zeng(State Key Lab of ASIC and System, Fudan University, P.R.China)	

SESSION 1D

Circuits and Systems for Wireless Communications (I)

1D-1	Wideband Spectrum Sensing using the All-phase FFT(invited paper) Lian Huai, Gerald E. Sobelman(Department of Electrical and Computer Engineering, University of Minnesota, USA),Xiaofang Zhou(State Key Lab of ASIC and System, Fudan University, Shanghai, China)	208
1D-3	A Robust Frame Synchronization Scheme For Broadband Power-line Communication Chen Chen, Yuebin Huang, Yizhi Wang, Yun Chen, Xiaoyang Zeng(State Key Lab. of ASIC and System, Dept. of Microelectronics, Fudan University Shanghai, China)	212
1D-4	FFT Implementation with Multi-Operand Floating Point Units Zhang Zhang1, Dongge Wang1, Yuteng Pan1, Dan Wang1, Xiaofang Zhou1, Gerald E. Sobelman2 (1State Key Lab of ASIC and System, Fudan University, Shanghai 200433, China 2Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis 55455, USA)	216
1D-5	General Lattice Wave Digital Filter with Phase Compensation Scheme Yan Zhao, Jinyuan Zhou, Xiaofang Zhou(State Key Lab of ASIC and System, Fudan University, Shanghai China), Gerald E. Sobelman(Dept. of Electrical and Computer Engineering, University of Minnesota, Minneapolis, USA)	220
1D-6	A High Efficient Baseband Transceiver for IEEE 802.15.4 LR-WPAN Systems Shouyi Yin, Jianwei Cui, Ao Luo, Leibo Liu and Shaojun Wei(Institute of Microelectronics, Tsinghua University National Laboratory for Information Science and Technology Beijing, P.R.China)	224
1 D-7	System Modeling and Analysis of the IEEE 802.15.4 Physical Layer Design Jikang Xia, Lan Chen, Ying Li, Yinhao Zhou(Institute of Microelectronics, Chinese Academy of Sciences, China)	228

SESSION 1E

Testing, Reliability, Fault-Tolerance (I)

1E-1	Towards the Next Generation of Low-Power Test Technologies(invited paper) Xiaoqing Wen(Department of Computer Systems and Engineering Kyushu Institute of Technology Japan)	232
1E-2	Word Error Control Algorithm through Multi-reading for NAND Flash Memories Chong Zhang(Graduate School of Information, Production and Systems), Tsutomu Yoshihara(Waseda University, Fukuoka, Japan)	236
1E-3	A New Scheme for Testability Improvement of ECC Incorporated Memory Lei Wang, Jianhua Jiang , Yumei Zhou, Gaofeng Ren(Institute of Microelectronic Chinese Academy Sciences)	240
1E-4	A BIST Scheme for High-speed Gain Cell Edram Bing Yan, Yufeng Xie, Rui Yuan, Yinyin Lin(ASIC & System State Key Lab, Dept. of Microelectronics, Fudan University, Shanghai, China)	244
1E-5	Variation-Resilient Voltage Generation for SRAM Weak Cell Testing Chingwei Yeh, Yan-Nan Liu, Jinn-Shyan Wang, Pei-Yao Chang(Department of Electrical Engineering, National Chung-Cheng University, Taiwan)	248
1E-6	Single Event Upset Immune Latch Circuit Design Using C-Element Ramin Rajaei, Mahmoud Tabandeh , Bizhan Rashidian(Department of Electrical Engineering, Sharif University of Technology, Tehran, IRAN)	252

SESSION 2E

Testing, Reliability, Fault-Tolerance ($\rm II$)

2E-1	Challenges of Electrostatic Discharge (ESD) Protection in Emerging Silicon	256
	Nanowire Technology(invited paper)	
	Juin J. Liou(Pegasus Distinguished Professor, University of Central Florida, Orlando,	
	Florida, USA), Chang Jiang (Scholar Endowed Professor, Ministry of Education,	
	China), Cao Guang-Biao (Endowed Professor, Zhejiang University, China)	
	Chang Gung (Endowed Professor, Chang Gung University, Taiwan)	
	Feng Chia(Endowed Professor, Feng Chia University, Taiwan)	

2E-2	A Software/Hardware Co-Debug Platform for Multi-Core Systems(invited paper) Kuen-Jong Lee, Long-Feng Chen, Jia-Wei Jhou(Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan), Alan Su ,Jiff Kuo, Mark Liu(Global UniChip Corporation, HsinChu, Taiwan)	259
2E-3	HV CMOS Orientated Variation-aware Layout and Robust Solution Gu Cong, Chen Hong(Design Enable Group, RASG, Freescale Semiconductor Ltd , Beijing, China)	263
2E-4	Modified Minimal-Connected-Component Fault Block Model to Deal with Defective Links and Nodes for 2D-Mesh NoCs Yueming Yang, Heng Quan, Zewen Shi, Xiaoyang Zeng, Zhiyi Yu(State Key Laboratory of ASIC & System, Fudan University, Shanghai, China)	267
2E-5	Addressing Fault Tolerance in 4-PAM Signaling by Using Block Codes for On-chip Communication Arash Abtahi Forooshani, Fakhrul Zaman Rokhani(Department of CCSE, University Putra Malaysia, Serdang Malaysia)	271
2E-6	A Novel Multi-finger Layout Strategy for GGnMOS ESD Protection Device Peng Zhang, Yuan Wang, Song Jia, Xing Zhang(Key Laboratory of Microelectronic Devices and Circuits, Peking University, China)	275

SESSION 1F

Advanced Memory (I)

1F-1	Current Status and Future Prospect of Phase Change Memory(invited paper) Byeungchul Kim(Semiconductor R&D Center, Samsung Electronics Co., Korea), Yoonjong Song, Sujin Ahn, Younseon Kang, Hoon Jeong, Dongho Ahn, Seokwoo Nam, Gitae Jeong, Chilhee Chung	279
1F-2	Memristor Models and Circuits for Controlling Process-VDD-Temperature Variations(invited paper) Kwan-Hee Jo, Chul-Moon Jung, and Kyeong-Sik Min(School of Electrical Engineering, Kookmin University, Korea)	283
1F-3	The Design of Low Leakage SRAM Cell with High SNM Hao YAN(Digital System Integration Lab, Institute of Acoustics, Chinese Academy of Sciences, and Graduate University of Chinese Academy of Sciences	287

Beijing, China),*, Donghui WANG, Chaohuan HOU(Digital System Integration Lab, Institute of Acoustics, Chinese Academy of Sciences)

1F-4	Novel RRAM Programming Technology for Instant-on and High-security FPGAs	291
	Xiaoyong Xue, Wenxiang Jian, Yufeng Xie, Qing Dong, Rui Yuan, Yinyin Lin(Fudan	
	University, China)	

1F-5 A Study of Dual-Vt Configurations of an 8T SRAM Cell in 45nm Wenbin Liu, Jinhui Wang,Wuchen Wu, Xiaohong Peng, Ligang Hou(Beijing University of Technology, Beijing China)

SESSION 2F

Advanced Memory (II)

3E 1	Challenges and Trends in Low-Power 3D Die-Stacked IC Designs Using RAM,	299
2F-1	Memristor Logic, and Resistive Memory (ReRAM)(invited paper)	
	Meng-Fan Chang Wei-Cheng Wu, Ching-Hao Chuang(Department of Electrical	
	Engineering, National Tsing Hua University, Hsinchu, Taiwan), Pi-Feng Chiu,	
	Shyh-Shyuan Sheu(EOL, ITRI, Hsinchu, Taiwan)	
2F-2	A 55nm ultra high density two-port register file compiler with improved write	303
21-2	replica technique	
	Zhao-Yong Zhang, Yi-Ping Zhang, Rui-Feng Huang, Shou-Dao Wu, Jian-Bin Zheng	
	(Department of Memory Design, AiceStar Technology Corporation, China), Li-Jun	
	Zhang(School of Urban Rail Transportation, Soochow University, China)	
AE A	Word Line Boost and Read SA PMOS Compensation (SAPC) for ROM in 55nm	307
2F-3	CMOS	
	Ruifeng Huang1, Jianbin Zheng, Zhaoyong Zhang, Hao Wu, Yue Yu (Aicestar	
	Technology Corp. China), Lijun Zhang (School of Urban Rail Transportation, Soochow	
	University, China)	
2F-4	Design of A Single-Ended Cell Based 65nm 32x32b 4R2W Register File	311
	Baoyu Xiong, Xingxing Zhang, Jun Han, Zhiyi Yu, Xiaoyang Zeng(State Key	
	Laboratory of ASIC & System, Fudan University, China)	

2F-5 A 90 nm 16Mb Embedded Phase-Change Memory

295

Hongwei Hong, Zheng Li, Qin Li, Ruizhe Wang(BAMC-BJ Corporation, China), and Charlie Hwang(BAMC, Texas, USA)

SESSION 1G

Circuits Simulation, Synthesis, Verification and Physical design (I)

1G-1	Separate Projection and Extended Cauer Method for Circuit Reduction(invited paper)	319
	Goro Suzuki(University of Kitakyushu JAPAN)	
1G-2	VLSI Interconnect Delay Analysis Method for Ramp Input Signal(invited paper)	324
	Nobuyuki Mihara, Goro Suzuki (University of Kitakyushu JAPAN)	
1G-3	RRA-Based Multi-Objective Optimization to Mitigate the Worst Cases of Placement	329
	Yiqiang Sheng, Shuichi Ueno(Department of Communication and Integrated Systems	
	Tokyo Institute of Technology, Japan), Atsushi Takahashi (Division of Electrical,	
	Electronic and Information Engineering Osaka UniversityJapan)	
1G-4	Numerical Characterization of Multi-Dielectric Green's Function for Floating	333
16-4	Random Walk Based Capacitance Extraction	
	Hao Zhuang(Department of Computer Science and Technology, Tsinghua	
	University, China, and School of Electronics Engineering and Computer	
	Science, Peking University, China), Wenjian Yu, Gang Hu(Department of	
	Computer Science and Technology, Tsinghua University, China), Zuochang	
	Ye(Institute of Microelectronics, Tsinghua University, China)	
1G-5	Power Grid Sizing via Convex Programming	337
	Peng Du, Shih-Hung Weng, Chung-Kuan Cheng(CSE Dept.), Xiang Hu(ECE Dept.,	
	University of California, San Diego, CA)	
10.6	Polarity optimization of XNOR/OR circuit area and power based on weighted sum	341
1G-6	method	
	Huihong Zhang(Institute of Circuits and Systems, Ningbo University, China), Pengjun	

Wang(Institute of Circuits and Systems, Ningbo University, China ,and State Key Laboratory of ASIC & System, Fudan University, China)

SESSION 2G

Circuits Simulation, Synthesis, Verification and Physical design (${\rm II}$)

2G-1	Don't Let the X-Bugs Bite: Conquer Elusive X-Propagation Issues Early!Get Them	345
2 G -1	Before They Get You!(invited paper)	
	Lisa Piper, Jin Zhang(Real Intent, Inc, Sunnyvale, CA)	
2G-2	Meshim: A High-Level Performance Simulation Platform for Three-Dimensional Network-on-Chip	349
	Menwang Xie(University of Science and Technology of China, China), Duoli Zhang(Hefei University of Technology, China), Yao Li(University of Science and Technology of China, China)	
2G-3	Through-Silicon-Via Assignment for 3D ICs	353
	Jianchang Ao, Sheqin Dong(Department of Computer Science and Technology, Tsinghua University, Beijing, China), Song Chen, Satoshi Goto(Graduate School of IPS, Waseda University, Kitakyushu-shi, Japan)	
2G-4	Incremental layout optimization for NoC Designs Based on MILP Formulation Jia Liu, Yuchun Ma(Department of Computer Science and Technology, Tsinghua University, China) Ning Xu(School of Computer Science and Technology, WuHan University of Technology, China), Yu Wang(Department of Electronic Engineering, Tsinghua University, China)	357
2G-5	Standard Cell Design of a Low-Leakage Flip-Flop Jianping Hu,Jun Wang(Faculty of Information Science and Technology, Ningbo University, China)	361
2G-6	Debugging Methodology and Timing Analysis in CDC Solution Akitoshi Matsuda(Kyushu Embedded Forum,Japan), Jin Zhang(Technical Marketing, Real Intent, USA)	365
2G-7	Circuit Simulation by Matrix Exponential Method Shih-Hung Weng, Quan Chen, Chung-Kuan Cheng(Department of Computer Science and Engineering, University of California, San Diego, CA)	369

SESSION 1H

CAD for system, Design for Manufacturing and Testing (I)

1H-1	A New Event Driven Testbench Synthesis Engine for FPGA Emulation	373
	Haocheng Huang, Aiwu Ruan, Yongbo Liao, Jianhua Zhu, Lin Wang, Chuanyin Xiang,	
	Pin Li(State key Laboratory of Electronic Thin Films and Integrated Device, University	
	of Electronic Science & Technology of China, China)	
1H-2	An Improved Packing Tool Based on a Dual-Output Basic Logic Element	377
	Xianyang Jiang(Institute of Microelectronics and Information Technology, Wuhan	
	University, China), Ying Liu (School of Physics and Technology, Wuhan University,	
	China), Shilei Sun, Gaofeng Wang(Institute of Microelectronics and Information	
	Technology, Wuhan University, China)	
111.2	A Test Approach of Combining Partial Scan with Functional Testing for High	381
1H-3	Performance Processors	
	Quanquan Li(Digital System Integration Lab, Institute of Acoustics, Chinese Academy	
	of Sciences, China, and Graduate University of Chinese Academy of Sciences, , China),	
	Yingke Gao, Tiejun Zhang, Chaohuan Hou(Digital System Integration Lab, Institute of	
	Acoustics, Chinese Academy of Sciences, China)	
1H-4	Automatic Layout Generator For Embedded FPGA Cores	385
	Chaofan Yu, Lingli Wang, Xuegong Zhou (State-Key-Lab of ASIC and System, Fudan	
	University, Shanghai, China)s	
111 5	An Optimized Mapping Algorithm Based on Simulated Annealing for Regular	389
1H-5	NoC Architecture	
	Liulin Zhong, Jiayi Sheng, Ming'e Jing, Zhiyi Yu, Xiaoyang Zeng, Dian	
	Zhou(State Key Laboratory of ASIC&System,Fudan University, Shanghai,	
	China)	
1H-6	The Buildup of FPGA Interconnect Timing Library	393
	Xiangzhi Meng, Liguang Chen, Hao Zhou, Jian Wang, Meng Yang, Jinmei Lai(The	
	State Key Lab of ASIC & System, Fudan University, China)	

CAD for system, Design for Manufacturing and Testing ($\rm II$)

2H-1	Robustness and Performance analysis on High Speed ASIC design with canonical statistical timing model	397
	Suoming Pu, Bo Yu, Xuan Zou(China Design Center, IBM Microelectronics, China)	
2H-2	Optimization of Mixed Polarity Reed-Muller Expressions Based on Whole Annealing Genetic Algorithm	401
	Meng Yang(State Key Lab of ASIC & System, Fudan University, China), Hongying Xu(Tianjin Vocational College of Mechanics and Electricity, China)	
2H-3	CPIPQ: A Common Platform for Silicon IP Qualification	405
	Mark P. C. Mok, Kenneth C. K. Lo, Yuzhong Jiao, Yiu Kei Li(IC Design Group,	
	Hong Kong Applied Science and Technology Research Institute (ASTRI), Hong Kong)	
2H-4	Comprehensive Electro-Thermal(ET) Analysis with Considering ET coupling	409
	Huang Kun, Zhao Guoxing, Yang Xu, Luo Zuying(College of Information Science	
	and Technology, Beijing Normal University, China)	
2H-5	Latency-Aware Mapping for 3D NoC Using Rank-Based Multi-Objective Genetic Algorithm	413
	Jiawen Wang, Li Li*, Hongbing Pan, Shuzhuan He, Rong Zhang(Institute of VLSI Design, Nanjing University, China	
	Key Laboratory of Advanced Photonic and Electronic Materials, Nanjing University,	
	China)	
2H-6	Mobility Overlap-Removal Based Timing-Constrained Scheduling	417
	Song Chen, Yuan Yao, and Takeshi Yoshimura(Graduate School of Information,	
	Production, and Systems, Waseda University, Japan)	
2H-7	An Effecient Level-shifter Floorplanning Method for Multi-Voltage Design	421
	Xiaolin Zhang, Zhi Lin, Song Chen, Takeshi Yoshimura	

SESSION 1I

MEMS technology, device and circuits

1 I-2	The Manufacturing of Si Base Thin Film Solar Cell Modules(invited paper)	425
	Tingkai Li(Hunan Gongchuang Photovoltaic Science & Technology Co., Ltd., China)	
1 I-3	Challenges and Strategies in Advanced CMOS Technology Development(invited paper)	430
	Xiaomeng Chen(Semiconductor Research and Development Center, Microelectronics	
	Division, IBM, USA)	
1I-4	Research on electromechanical model of micro-accelerometer based on SOI technology	433
	Keqiang Qian, Wen Luo, Qi Yu(State Key Lab of Electronic Thin Films and Integrated	
	Devices, Univ. of Electronics Science & Technology of China China)	
11 5	CMOS Compatible MEMs Process for Post Interconnect Single Chip Integration	437
1I-5	Application	
	Xiaoxu Kang, Qingyun Zuo, Jiaqing Li, Chao Yuan, Yuhang Zhao(Process Technology	
	Department, Shanghai IC R&D Center, China)	

SESSION 1J

Analog Filters and Oversampling Data Converters

1J-1	Cascadable Current-Mode Multifunction Filter Configuration Using Minimum Number of CCTAs and Grounded Capacitors Xifeng Zhou,Jinguang Jiang , Shanshan Li(Wuhan University,China)	441
1J-2	A matrix approach to low-voltage low-power log-domain CMOS current-mode adjustable-bandwidth step-gain filter design Xiaoyu Wang, Haigang Yang, Tao Yin, Fei Liu(Chinese Academy of Sciences, China)	445
1J-3	A Sigma-Delta Modulator with a Novel Chopper Correlated Double Sampled Integrator Luo Wang, Huihui Ji(Beihang University, China), Quan Sun(Chinese Academy of Sciences, China)	449
1 J-4	VLSI Implementation of High-Speed Low Power Decimation Filter for LTE	453

	Sigma-Delta A/D Converter Application Jing Li, Ran Li, Ting Yi, Zhiliang Hong(Fudan University, China), Bill Yang Liu(Analog Devices, China)	
1J-5	A Continuous Time Sigma-Delta Modulator Using Time-Domain Quantizer and Feedback Element Siliang Hua, Hao Yan, Yan Liu, Donghui Wang, Chaohuan Hou(Chinese Academy of Sciences, China)	457
1 J-6	An Analysis on a Pseudo-Differential Dynamic Comparator with Load Capacitance Calibration Daehwa Paik, Masaya Miyahara, and Akira Matsuzawa(Tokyo Institute of Technology, Japan)	461
1 J-7	Modeling of a Double-Sampling Switched-Capacitor Bandpass Delta-Sigma Modulator for Multi-Standard Applications Hong Chang*, Wenxian Lu, Xu Cheng*, Yawei Guo, Xiaoyang Zeng(Fudan University, China)	465

SESSION 2J

Nyquist Analog-to-Digital Converters (1)

2J-1	A Time-Domain Flash ADC Immune to Voltage Controlled Delay Line Non-Linearity(invited paper) Young-Hwa Kim, and SeongHwan Cho(Korea Advanced Institute of Science and Technology , Korea)	469
2J-2	A 10-Bit, 50 MS/s, 55 fJ/conversion-step SAR ADC with Split Capacitor Array Seong-Jin Cho, Yohan Hong, Taegeun Yoo, and Kwang-Hyun Baek (Chung-Ang University, Seoul, Korea)	472
2J-3	A 1.8V 100MS/s 10-bit Pipelined Folding A/D Converter With 9.49 ENOB at Nyquist Frequency Xiaojuan Li, Yintang Yang, Zhangming Zhu(Xidian University, China)	476
2J-4	A sample-and-hold circuit for 10-bit 100MS/s Pipelined ADC Haitao Wang, Hui Hong, Lingling Sun, and Zhiping Yu(Key Laboratory for RF Circuits and Systems of Ministry of Education and Hangzhou Dianzi University, China)	480

2J-6 A Low Power 10-bit 100-MS/s SAR ADC in 65nm CMOS Jun Ma, Yawei Guo, Li Li, Yue Wu, Xu Cheng, Xiaoyang Zeng (Fudan University, China)

SESSION 3J

Nyquist Digital-to-Analog Converters

3J-1	A Dual 12bit 80MSPS 3.3V Current-Steering DAC for HINOC Application	488
	Hongming Chen , Yuhua Cheng (Shanghai Research Institute of Microelectronics,	
	Peking University, China), Xiaoyuan Chen(Shanghai Bwave Technology Co., Ltd)	
3J-2	A 4-Channel 8-bit 650-MSample/s DAC with Interpolation Filter for Embedded	492
30 1	Application	
	Qianqian Ha, Fan Ye, Chixiao Chen, Xiaoshi Zhu, Mingshuo Wang, Yujing	
	Lin, Ning Li, Junyan Ren(Fudan University, China)	
3J-3	A New Current Switch Driver with Improved Dynamic Performance Used for	496
21-2	500MS/s, 12-bit Nyquist Current-Steering DAC	
	Guojia Liu, Lenian He, Xiaobo Xue, Qifeng Shi(Zhejiang University, China)	
3J-4	A 14-Bit 2-GSs DAC with SFDR 70dB up to 1-GHz in 65-nm CMOS	500
	Ran Li, Qi Zhao, Ting Yi, Zhiliang Hong(Fudan University, China)	
3J-5	A Multi-mode 1-V DAC+filter in 65-nm CMOS for Reconfigurable (GSM,	504
21-2	TD-SCDMA and WCDMA) Transmitters	
	Li Li, Jun Ma, Yawei Guo, Xu Cheng, Xiaoyang Zeng(Fudan University, China)	

SESSION 4J

Reference & Nyquist Analog-to-Digital Converters (II)		
4J-1	Energy efficient ADC design with low voltage operation(invited paper)	508
	Akira Matsuzawa(Tokyo Institute of Technology,Japan)	
4J-2	A low-power 4.224GS/s Sampler in 0.13-µm CMOS for IR UWB Receiver	512
	Yi Zhao, Jun Jiang, Ke Shao, Yajie Qin, Zhiliang Hong(Fudan University, China)	

4J-3	CMOS low-power subthreshold reference voltage utilizing self-biased body effect	516
	Zhang Hao, Zhang Yimeng, Huang Mengshu, Yoshihara Tsutomu(Waseda University,	
	Japan)	
4J-4	A Precision 2.5V Bandgap Voltage Reference with Excellent Initial Accuracy of	520
4J-4	0.25% for High Resolution ADCs	
	Xiaozong Huang, Jing Zhang, Luncai Liu, Wengang Huang, Yanlin Zhang ,Lei Yu(Sichuan	
	Institute of Solid-state Circuits, China)	
4J-5	A High-Performance Bandgap Reference with Advanced Curvature-Compensation	524
	Zekun Zhou, Xiangzhu Xu, Yue Shi, Xin Ming, Bo Zhang(University of Electronics Science	

and Technology of China, China)

SESSION 1K

New Processing & Devices, Hetro-integration, 3-D integration (I)

1K-1	Novel Flash Ion Sensitive Field Effect Transistor for Chemical Sensor	528
112-1	Applications(invited paper)	
	Chao-Sung Lai(Department of Electronic Engineering, Chang Gung	
	University, Taiwan, and Biosensor Group, Biomedical Engineering Center, Chang Gung	
	University, Taiwan), Tseng-Fu Lu(Department of Electronic Engineering, Chang Gung	
	University, Taiwan), Jer-Chyi Wang (Department of Electronic Engineering, Chang Gung	
	University, Taiwan, and Biosensor Group, Biomedical Engineering Center, Chang Gung	
	University, Taiwan)	
1K-2	A Model for Energy Quantization of Single-electron Transistor Below 10nm	531
	Xiaobao Chen, Zuocheng Xing, Bingcai Sui(School of Computer, National University	
	of Defense Technology, China)	
	An Efficient Design Algorithm for Exploring Flexible Topologies in Custom	535
1K-3	Adaptive 3D NoCs for High Performance and Low Power	
	Xin Jiang, Ran Zhang and Takahiro Watanabe(Graduate School of Information,	
	Production & Systems, Waseda University, Japan)	
	LDO based Design and Optimization of Power Distribution under Worst	539
1K-4	Performance	
	Amirali Shayan, Xiang Hu, Chung-Kuan Cheng(epartment of Computer Science and	

SESSION 2K

New Processing & Devices, Hetro-integration, 3-D integration (II)

2K-1		
	Jyi-Tsong Lin, Hsuan-Hsu Chen, Kuan-Yu Lu, Chih-Hung Sun(Department of electrical	
	engineering, National Sun Yat Sen University, Taiwan ROC) Tung-Yen Lai, Fu-Liang	
	Yang(National Nano Device Laboratories, Taiwan)	
2K-2	An analytical model for SOI triple RESURF devices	547
	Haimeng Huang, Yongwei Wang, Xingbi Chen(State Key Laboratory of Electronic Thin	
	Films and Integrated Devices University of Electronic Science and Technology of China, China)	
2K-3	A Study of Second Saturation Effect of OPTVLD NMOS	551
2 K- 3	Wenfang Du, Xingbi Chen(State Key Laboratories of Electronic Thin Films and	551
	Integrated Devices University of electronic science and technology of China, Chengdu,	
	China)	
2K-4	Quantum Mechanical Effects on the Threshold Voltage of the Evenly Doped	555
2 N -4	Surrounding-Gate MOSFETs	
	Guanghui Mei, Peicheng Li, Guangxi Hu, Ran Liu, Tingao Tang(State Key Lab of ASIC	
	and System, School of Information Science and Technology, Fudan University, China)	
	Effect of Structural Parameters on the Performance and Variations of Nanosizes	558
2K-5	PNIN Tunneling Field Effect Transistor	
	S. Q. Cheng, C. J. Yao, D. M. Huang(State Key Laboratory of ASIC and System,	
	Department of Microelectronics, Fudan University, China)	
2K-6	Exploring 3D Power Distribution Network Physics	562
211 0	Xiang Hu(ECE Dept). , Peng Du, Chung-Kuan Cheng(CSE Dept., University of	502
	California, La Jolla, CA)	
2K-7	An Efficient Solver for Statistical Capacitance Extraction Considering Random	566
2 K- /	Process Variations	
	Rubing Bai(Department of Computer Science and Technology, Tsinghua	
	University, China), Shan Zeng(School of Software, China University of	
	Geosciences, Beijing, China), Qingqing Zhang(Department of Computer	

Science and Technology, Tsinghua University, China, and College of Information Science and Technology, Beijing Normal University, China), Wenjian Yu(Department of Computer Science and Technology, Tsinghua University, China)

SESSION 1N

Other VLSI Device and Design related topics

 IN-1
 Physics-Based Compact Variability/Reliability Modeling for Emerging No paper

 Double-Gate/Nanowire MOSFETs(invited paper)

 Xing Zhou (Nanyang Technological University, Singapore)

1N-5	Performance Evaluation Modeling for Reconfigurable Processor	570
	Shuang Liang*, Shouyi Yin, Chongyong Yin, Leibo Liu, Shaojun Wei(Tsinghua	
	University, China)	

1N-7	A High Performance Clock Precharge SEU Hardened Flip-flop	574
	Riadul Islam, S.E. Esmaeili(Department of Electrical & Computer Engineering,	
	Canada), Thouhidul Islam(Department of Electrical & Electronic Engineering,	
	Bangladesh University of Engineering & Technology, Bangladesh)	
1N-8	Design of 2-3 mixed-valued/six-valued adiabatic asynchronous up-down counter	578
	Fengna Mei(Institute of Circuits and Systems, Ningbo University, China), Pengjun	

Wang(State Key Laboratory of ASIC & System, Fudan University, China)

SESSION 10

Clock Synthesizer and Building Blocks (\boldsymbol{I})

10-1	A Study of Frequency Synthesizer for AT-DMB Applications(invited paper) Jun Cheng, Yong Moon(Soongsil University, South Korea)	582
10-3	A New Figure of Merit of LC Oscillators Considering Frequency Tuning Range Takahiro Sato, Kenichi Okada and Akira Matsuzawa(Tokyo Institute of Technology, Japan)	586
10-4	Low Noise Low Power Two-Stage Modulator With Injection Locked LO Divider in 65nm CMOS Wufeng Wang, Peichen Jiang, Tingting Mo, Jianjun Zhou(Shanghai Jiao Tong University, China)	590
10-5	Design of a Low-Power Low-Phase-Noise Multi-Mode Divider With 25%-Duty-Cycle Output in 0.13um CMOS Song Hu, Weinan Li, Yumei Huang, Zhiliang Hong(Fudan University, China)	594

SESSION 20

Clock Synthesizer and Building Blocks (${\rm I\hspace{-0.5mm}I}$)

20-2	A Noise Rejective VCO with Build-in Active LC Filter	598
	Ma Zhuo, Guo yang, Xie Lunguo, Liu Rongrong and Zuo Hongjian(National	
	University of Defense Technology, China)	
20-3	A 0.8ps Minimum-Resolution Sub-Exponent TDC for ADPLL in 0.13µm CMOS Xiaolu Liu, Na Yan, Xi Tan, Hao Min(Fudan University)	602
20-4	0.5 VDD Digitally Controlled Oscillators Design with Compensation Techniques	606

for PVT Variations

Chia-Wen Chang,Shyh-Jye Jou (National Chiao Tung University, Taiwan)Yuan-Hua Chu(Industrial Technology Research Institute, Taiwan)

20-5	Digitally-Controlled Cell-Based Oscillator with Multi-Phase Differential Outputs	610
	Ming-Chiuan Su and Shyh-Jye Jou(National Chiao Tung University, Taiwan R.O.C)	

20-7	A Low Phase Noise Injection-Locked Doubler-based Quadrature CMOS VCO	614
	Chen Lian, Wei Li, Haipeng Fu, Ning Li, Junyan Ren (Fudan University, China)	

SESSION PA

Poster Session (I)

PA01	A Thermal Model for the Top Layer of 3D Integrated Circuits Considering Through Silicon Vias Fengjuan Wang, Zhangming Zhu, Yintang Yang, Ning Wang (Xidian University, China)	618
PA02	Novel High Uniformity Readout Circuit Allowing Microbolometer to Operate with Low Noise Jian Lv*, Yun Zhou, Baobin Liao, Yadong Jiang(University of Electronic Science and Technology of China, China)	621
PA04	Integration of information security chips based on System-in-Package Tong Ran , Guoqiang Bai(Tsinghua University, China)	625
PA05	A New Asynchronous Delay-Insensitive Link based on a 1-of-4 LETS Code Can Wang, Qin Wang, Jianfei Jiang (Shanghai Jiao Tong University, China)	629
PA06	A High-speed Asynchronous Array Multiplier based on Multi-threshold Semi-Static NULL Convention Logic Pipeline Yanfei Yang, Yintang Yang, Zhangming Zhu, Duan Zhou (XiDian University, China)	633
PA07	An Ultra Low Power ASK Demodulator for Passive UHF RFID Tag Hongqiang Zong, Jinpeng Shen, Shan Liu, Mei Jiang, Qingyuan Ban, Ling Tang, Fanyu	637

	Meng, and Xin'an Wang(Peking University Shenzhen Graduate School, China)	
PA08	Improvement and Parallel Implementation of Canny Edge Detection Algorithm Based on GPU	641
	Shengxiao Niu, Jingjing Yang, Sheng Wang, Gengsheng Chen(Fudan University, China)	
PA09	A New Full Current Mode Sense Amplifier with Compensation Circuit Yiqi Wang, Fazhao Zhao, Mengxin Liu, Zhengsheng Han (Chinese Academy of Sciences, China)	645
PA10	An Efficient 90nm Technology-Node GHz Transceiver of On-Chip Global Interconnect Zaixiao Zheng, Zhigang Mao, Jianfei Jiang (Shanghai JiaoTong University, China)	649
	Zaixiao Zheng, Zhigang Mao, Jiamei Jiang (Shanghai Jiao long University, China)	
PA11	Electrochemical Biosensor Based on Modified Graphene Oxide for Tuberculosis Diagnosis	653
	Pei Zhang, Xiaosen Chai, Chun Xu, Jia Zhou(Fudan University, China)	
PA12	Digital Quadrature IF modulator using single-bit DACs RuiminHuang,ChaodongLing,JiaxianWang(HuaqiaoUniversity, China)	657
PA13	Zero-Crossing Distortion Analysis in One Cycle Controlled Boost PFC for Low THD Yani LI, Yintang YANG , Zhangming ZHU (Xidian University, China), Wei Qiang (Xi'an Longtium Microelectronics Technology Developing Co., Ltd, China)	661
	(At an Eonglium Wherefeleuromes reembiology Developing Co., Ed., China)	
PA14	A Simulation Study of Vertical Tunnel Field Effect Transistors	665
	Zhong-Fang Han, Guo-Ping Ru*, Gang Ruan(Fudan University, China)	
PA15	Determination of the trap states distribution in Poly-Si films using the OEMS modulation	669
	Xiyue Li, Wanling Deng, Junkai Huang(Jinan University, China)	
PA16	High efficiency and low power multi-rate LDPC decoder design for CMMB Jiang xiaobo, li hongyuan (South China University of Technology, Chain)	673
PA17	Area efficient LDPC decoder design for parallel layered decoding Yuan Yao, Fan Ye, and Junyan Ren(Fudan University, China)	679
PA19	Accelerating the Data Shuffle Operations for FFT Algorithms on SIMD DSPs	683
	Kai Zhang1*, Shuming Chen1, Sheng Liu1, Yaohua Wang1, Junhui Huang1	
	(1 School of Computer, National University of Defense Technology, Changsha 410073, China)	
PA20	Automatic Compilation Flow for a Coarse-grained Reconfigurable Processor	687
	Hao Wang, Weiguang Sheng, Weifeng He (Shanghai Jiao Tong University, China)	

PA21	Origin of High On-State Current For Dopant-Segregated Schottky MOSFET Yang Tang, Liu-Lin Zhong, and Yu-Long Jiang (Fudan University, China)	691
PA22	System Level Performance Evaluation of Three-Dimensional Integrated Circuit Libo Qian*, Zhangming Zhu, Yintang Yang(Xidian University, China)	694
PA23	An Energy Efficiency Task Scheduling Algorithm for Streaming Applications on Multiprocessor SoC Shan Cao*, Zhaolin Li, and Shaojun Wei(Tsinghua University, China)	698
PA24	Analysis and Architecture Design of Aggregation in BM3D Wenjiang Liu1*, Yue Zhu, Tao Liu, Mengtian Rong, Hao Zhang (Shanghai Jiao Tong University, China)	703
PA25	A JTAG-based Configuration Circuit applied in SerDes Chip Xun Jiang, Xiaoxin Cui*, Dunshan Yu(Peking University, China)	707
PA26	An Automated Design Flow for Image Processing Filter in Embedded Systems Akitoshi Matsuda(Kyushu University, Japan), Shinichi Baba(Kyushu Embedded Forum, Japan)	711
PA27	A Novel Channel Estimation Algorithm in OFDM Power Line Communication System Huidong Zhao*, Yong Hei, Shushan Qiao(Institute of Microelectronics of Chinese Academy of Sciences, China) *Email:hdzhao2003@126.com	715
PA28	Low Power Design for SoC with Power Management Unit Daying Sun, Shen Xu, Weifeng Sun, Shengli Lu, Longxing Shi (Southeast University, China)	719
PA29	Improvement on Branch Scheduling for VLIW Architecture Lidan Bao, Hongmei Wang, Tiejun Zhang, Donghui Wang, Chaohuan Hou (Chinese Academy of Sciences, China)	723
PA30	Research on Reconfigurable Multiplier Unit Based on GF[(28)]4 Field of Symmetric Cryptography Xu JianBo, Dai Zibin(Zhengzhou Information Science and Technology Institute, China), Xuan Yang (Jiangnan Institute of Computing Technology ,China) Su Yang(Zhengzhou Information Science and Technology Institute, China)	727
PA31	A Low-Voltage Differential Injection Locked Divider with Forward Body Bias Haipeng Fu, Hanchao Zhou, Yangyang Niu, Junyan Ren*, Wei Li*, Ning Li(Fudan	731

University, Shanghai, China)

PA32	Effects of unintended dopants on I-V characteristics of the double-gate MOSFETs, a simulation study Peicheng Li, Guanghui Mei, Guangxi Hu*, Ran Liu, and Tingao Tang(Fudan University, China)	735
PA33	A Control Scheme for a 65nm 32×32b 4-read 2-write Register File Jun Han, Xingxing Zhang, Baoyu Xiong, Zhiyi Yu*, Xiaoyang Zeng (Fudan University, China)	739
PA34	Reflection Analysis of Signal Transmission in 32-bit CPU Based SiP Zerong Tao, Liji Wu*, Xiangmin Zhang (Tsinghua University, China)	743
PA35	Research on Testing of 32-bit CPU Based SiP Chunlin Xie, Liji Wu*, Xiangmin Zhang (Tsinghua University, China)	747
PA37	A Security Processor Based on MIPS 4KE Architecture Shuai Wang1, Yang Li, Junbao Liu, Jun Han*, and Xiaoyang Zeng(Fudan University, China)	751
PA38	Design of A Reconfigurable Network Interface Processor Lei Zhang (Xi'An University of Posts and Telecom, China), Tao Li(Shaanxi Provincial Research Center of Telecom ASIC Design, China), Zhentao Li , Lin Jiang(Xi'An University of Posts and Telecom, China)	755
PA39	A Hardware Accelerator for Speech Recognition Applications Tao Chen, Jiawei Zheng, Xingsi Zhang, Shengchang Cai, YunChen(Fudan University, China)	760
PA40	A Programmable IP Core for LDPC Decoder Based on ASIP Jun Deng(Sichuan Institute of Solid-state Circuits, China), Bing Li(Southeast University, China), Lintao Liu(Science and Technology on Analog Integrated Circuit Laboratory, China),Rui Chen(Southeast University, Nanjing, 210096, China)	764
PA41	Parallel Structure of GF (2 ¹⁴) and GF (2 ¹⁶) Multipliers Based on Composite Finite Fields Jianing Su, Zhenghao Lu*(Soochow University, Suzhou, China)	768

PA43	A New Method to Improve the Unconditional Stability of InGaP/GaAs Heterojunction Bipolar Transistor Shanggong Feng1, Yanhu Chen, Huijun Li(Shan Dong University, China), Minghua Zhang(Artillery Command Academy, China)	772
PA44	An Accurate Physics-Based Method for Calculating DC Inductance of On-chip Square Multi-layer Inductors Jinran Du, Wanghui Zou, Xuecheng Zou(Huazhong University of Science and Technology, China)	775
PA45	Dual Frequency Based Real Time Location System Using Passive UHF RFID Junjuan Liu, Xi Tan, Hao Min (Fudan University, China)	779
PA47	A Reconfigurable Linear Array Processor Architecture for Data Parallel and Computation Intensive Applications Yucheng Liu, Jing Xie, Zhigang Mao (Shanghai Jiao Tong University, China)	783
PA48	A permutation network for configurable and scalable FFT processors Shuai Chen, Jialin Chen, Kanwen Wang, Wei Cao*, Lingli Wang, Member, IEEE(Fudan University, China)	787
PA49	Comparison of 2D MESH Routing Algorithm in NOC Pan Hao,Hong Qi, Du Jiaqin,Pan Pan(Anhui University, China)	791
PA50	Simulation of Carrier Transport in Quantum Cascade Lasers Yingying Li, Guo-Ping Ru(Fudan University, China), ZM. Simon Li(Crosslight Software Inc., Canada)	796
PA51	Design of a UHF RFID Tag Baseband with the Hummingbird Cryptographic Engine Mengqin Xiao, Xiang Shen and Junyu Wang(Fudan University, China), Joseph Crop	800
PA52	(Oregon State University, USA) A study on channel polarization and polar coding Yichao Lu, Satoshi Goto (WASEDA UNIVERSITY, Japan)	804
PA53	A Novel Linear Power Amplifier for 2.6GHz LTE applications Jianbao Deng*, Shilin Zhang, Luhong Mao, Sheng Xie, Huichao Li(Tianjin University, China)	808
PA54	Design of a Monolithic Low-power Micro-sensor Signal Processing System	812

Zhuping Wang, Keshu Zhang(Chinese Academy of Sciences, China)

SESSION PB

Poster Session (II)

PB01	TSV Based 3D IC Wire Length Calculation Algorithm Ligang Hou*, Shu Bai, Jinhui Wang(Beijing University of Technology, China)	816
PB02	A New Low Power Symmetric Folded Cascode Amplifier by Recycling Current in 65nm CMOS Technology Xiao Zhao, Huajun Fang and Jun Xu(Tsinghua University, China)	820
PB03	Ultra low voltage, wide tuning range voltage controlled ring oscillator Li Tianwang1, Jiang Jinguang (Wuhan University Wuhan, China), Ye Bo, Han Xingcheng(Shanghai University of Electric Power, China)	824
PB05	A 2.5V Supply Low Noise CMOS Amplifier Using Noise Reduction Technique of Chopper Stabilization Hossein yahyatabar1*, Prof.Farhad Razaghian1, Mehran Yahyavi(Islamic Azad University), Mohsen Habib Nezhad(Multi Media University)	828
PB07	Efficient Floating Random Walk Algorithm for Interconnect Capacitance Extraction Considering Multiple Dielectrics Gang Hu, Wenjian Yu(Tsinghua University, China), Hao Zhuang(Peking University, China), Shan Zeng(China University of Geosciences, China)	834
PB08	A Dual Mode High efficiency Buck DC-DC Converter Xu Gong, Jinguang Jiang*, Xifeng Zhou (Wuhan University, China)	838

PB10	A Novel Transimpedance Amplifier for 10 Gbit/s Optical Communication System Taiyi Huang, Qihui Zhang, Weifeng Zhang(Henan University, China)	843
PB11	Single Event Upset Mitigation for FDP2008 Meng Yang, Gengsheng Chen(Fudan University, China)	847
PB12	Electro-thermal Model Extraction of Power GaN HEMT Using I-V Pulsed and DC Measurements Zhifu Hu ,Xuebang Gao, Shujun Cai (Hebei Semiconductor Research Institute ,China)	850
PB13	Characterization and Analysis of Pattern dependent Variation-aware Interconnects for a 65nm Technology Lele Jiang, Xiaojing Qin(Shanghai Research Institute of Microelectronics, Peking University, China), Lifu Chang(Semiconductor Manufactuing International Corporation , China), Yuhua Cheng(Shanghai Research Institute of Microelectronics, Peking University, China)	854
PB14	Integrated Gm-C Based PI Controller for MEMS Gyroscope Drive Huan-ming Wu, Hai-gang Yang, Xiao-yan Cheng, Tao Yin(Chinese Academy of Sciences, China), Jiwei Jiao(Shanghai Institute of Microsystem and Information Technology, CAS, China)	858
PB15	Subthreshold MOSFET Bandgap for Ultra-Low Supply Voltage Yilei Li*, Yu Wang, Na Yan, Xi Tan and Hao Min(Fudan University, China)	862
PB16	A Highly Linear Wideband Variable Gain CMOS Balun-LNA Hui Wang, Taotao Yan, Dongpo Chen, and Jianjun Zhou(Shanghai Jiao Tong University, China)	866
PB17	A 65nm 10MHz Single-Inductor Dual-Output Switching Buck Converter with Time-Multiplexing Control Miao Yang, Weifeng Sun, Shen Xu, Shengli Lu, Longxing Shi(Southeast University, China)	870
PB18	Design and Implementation of pipelined TMVP multiplier using block recombination Xiao Ma1 and Guoqiang Bai (Tsinghua University, China)	874
PB19	A Novel Low THD 4-Quadrant Analog Multiplier Using Feedforward Compensation for PFC Yani LI, Yintang YANG, Zhangming ZHU (Xidian University, China), Wei Qiang (Xi'an Longtium Microelectronics Technology Developing Co., Ltd, China)	878

PB20	An Inductorless CMOS LNA with Single input and Differential output Jinguang Jiang, Qingyun Li, Xifeng Zhou (Wuhan University, China)	882
PB21	A New Nonlinear Parameterized Model Order Reduction Technique Combining the Interpolation Method and Proper Orthogonal Decomposition Zhiyu Xu, Xinnan Lin, Hao Zhuang, Bo Jiang, Haijun Lou (Peking University Shenzhen Graduate School, China), Jin He(PKU HKUST Shenzhen Institute, China)	886
PB22	A 0.6 ppm/°C Current-Mode Bandgap with Second-Order Temperature Compensation Yilei Li, Yu Wang, Na Yan*, Xi Tan and Hao Min(Fudan University, China)	890
PB23	A 12-bit 50-MSPS SHA-less Opamp-Sharing Analog-to-Digital Converter in 65nm CMOS ChenShu,Guanghua Shu, Jun Xu, Fan Ye, Junyan Ren(Fudan University, China)	894
PB25	A sixth-order Chebyshev low-pass filter for single-chip UHF RFID Reader Jiang Chen*, Shilin Zhang, Luhong Mao(Tianjin University, China)	898
PB26	A Realizable Reconstruction Filter for Sampled data Systems Muwahida Liaquat, Mohammad Bilal Malik(National University of Sciences and Technology, Pakistan)	902
PB27	Optimization of ADM with both restrictions of resolution and power dissipation in low supply voltage Shujuan Yin (Beijing Information Science and Technology University, China), Xiangyu Li(Tsinghua University, China)	906
PB28	A Timing-Perspective Study on the Wire Model in Placement Liu Liu (Tsinghua University, China), Yongqiang Lu (Research Institute of Information Technology Tsinghua University, China), Qiang Zhou(Tsinghua University, China)	910
PB29	Design for testability of FFT/IFFT IP core for UWB systems Weilu Su1, Longzhao Shi (Fuzhou University, China)	914
PB30	A CMOS Hysteresis Undervoltage Lockout with Current Source Inverter Structure Chao Zhang, Zhijia Yang, Zhipeng Zhang (Shenyang Institute of Automation Chinese Academy of Sciences, China)	918

PB31	A high linearity MOS capacitor for low voltage applications Shujuan Yin (Beijing Information Science and Technology University, China)	922
PB32	A Low-Kickback Preamplifier with Offset Cancellation For Pipelined Folding A/D Converter Xiaojuan Li*, Yintang Yang, Zhangming Zhu (Xidian University, China)	925
PB33	Auto-Assign Method for large scale flip-chip package design Haitao Han, Wen Yin, Wenqian Wang, Zegui Pang(IBM GCG Systems & Technology Lab)	929
PB34	A 60GHz Power Amplifier using 90-nm RF-CMOS Technology Nan Zhang, Lingling Sun, Jincai Wen, Jun Liu, Jia Lou, Guodong Su, He Li(Hangzhou Dianzi University, China)	933
PB35	The Design and Verification of SEU-hardened Configurable DFF Xinrui Zhang, Liguang Chen, Liyun Wang, Jian Wang, Jinmei Lai(Fudan University, China)	937
PB36	Efficient Temporal Task Partition for Coarse-Grain Reconfigurable Systems Based on Simulated Annealing Genetic Algorithm Yifan Zhou, Weiguang Sheng, Xie Liu, Weifeng He, Zhigang Mao (Shanghai Jiaotong University, China)	941
PB37	Improved Algorithm for Pareto Front Computation for CMOS Opamp Based on Multi-objective Genetic Optimization Peng Chen, Yushun Guo (Hangzhou Dianzi University, China)	945
PB38	Calibration Method Considering Second-Order Error Term of Timing Skew for A Novel Multi-Channel ADC Yong-sheng Yin , Rui Zhang, Jun Yang, Ming-lun Gao(Hefei University of Technology, China)	949
PB40	Large-Signal MOSFET Modeling by Means of Knowledge Based Fuzzy Logic System Liyuan Wang, Yushun Guo (Hangzhou Dianzi University, China)	953
PB41	Design and Application of Reusable SoC verification platform Lulu Feng, Zibin Dai, Wei Li, Jianlei Cheng(Zhengzhou Information Science and Technology Institute, China)	957

PB42	New power rail ESD clamp design with current starving technology Bo Li, Liji Wu, Xiangmin Zhang (Tsinghua University, China)	961
PB43	Design and Implementation of A Low Power Java Coprocessor for dual-interface IC BankCard Junwei He, Liji Wu, Xiangmin Zhang(Tsinghua University, China)	965
PB44	A Method to Build Reconfigurable Architectures by Extracting Common Subgraphs Tianyun Zhang, Rui Zhang, Lingli Wang(Fudan University, China), Yu Hu(University of Alberta, Canada)	970
PB45	A novel high-accuracy clock stabilizer with 50% duty cycle Biye Xu, Lenian He(Zhejiang University, China)	974
PB46	A 1.2 V 70 mA Low Drop-out Voltage Regulator in 0.13 μm CMOS Process Qin Wu, Wei Li, Ning Li, Junyan Ren(Fudan University, China)	978
PB47	Compensator Design for Digital Controlled Switched-Mode Power Supplies Ling Lin, Jianping Qiu, Lenian He(Zhejiang University, China)	982
PB49	A 1.2-V 250-MS/s 8-bit Pipelined ADC in 0.13-μm CMOS Peiyuan Wan, Wei Lang, Di Fang, Wei Cui, and Pingfen Lin(Beijing University of Technology, China)	986
PB50	A Novel RSD Correction for Pipeline ADC Dawei Fu, Lenian He, Biye Xu(Zhejiang University, China)	990
PB51	A Digital Sliding Mode controller for Swiching Power Supply Converters Guannan Xu, Chen Jia, Chun Zhang, Zhihua Wang (Tsinghua University, China)	994
PB52	A Low-Power Gm-R-C Image Rejection Filter for Complex Low-IF Receiver Hao Li, Hong Zhang, Xunwei Weng, Ruizhi Zhang (Xi'an Jiaotong University, China)	998
PB53	A 4GS/s 3b Two-way Time-Interleaved ADC in 0.13um CMOS Cunchen Gu, Yi Zhao, Zhiliang Hong(Fudan University, China)	1002
PB54	A Low Power 1.0 GHz VCO in 65nm-CMOS LP-Process Zhang Zhang (Hefei University of Technology, China), Zhiyi Yu, Xu Cheng,	1006

A Charge-Pump Circuit to Restrain Reference Spurs in the PLL	1010
Changhong Huan, Xiushan Wu(China Jiliang University, China), Dan Wang (Anhui	
University of Technology, China)	
A Wide Lock-Range, Low Jitter Phase-Locked Loop for Multi-Standard SerDes Application	1014
Shaolong Liu , Hui Wang, Yuhua Cheng(Shanghai Research Institute of	
Microelectronics, Peking University, China)	
Ultralow-power Analog Front-End IC Design for an Implantable Cardioverter	1018
Defibrillator (ICD) (invited paper)	
Weibo Hui, Yen-Ting Liui, Tam Nguyeni,2, Bosco Dsouzai and Donald	
Y.C. Lie1,2 (1Texas Tech University (TTU), USA. 2Texas Tech Health Sciences	
Center (TTUHSC), USA)	
	 University of Technology, China) A Wide Lock-Range, Low Jitter Phase-Locked Loop for Multi-Standard SerDes Application Shaolong Liu , Hui Wang, Yuhua Cheng(Shanghai Research Institute of Microelectronics, Peking University, China) Ultralow-power Analog Front-End IC Design for an Implantable Cardioverter Defibrillator (ICD) (invited paper) Weibo Hui, Yen-Ting Liui, Tam Nguyeni,2, Bosco Dsouzai and Donald Y.C. Liei,2 (<i>ITexas Tech University (TTU), USA. 2Texas Tech Health Sciences</i>

SESSION 1R

RF transceiver and building blocks (I)

1R-1	A 60GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver(invited paper) Kenichi Okada(Tokyo Institute of Technology, Japan)	1022
1R-2	An Area-Efficient Dual-Channel RF Receiver for GPS-L1/Galileo-E1/Compass-B1 Hongliang Tian, Dongpo Chen, Tingting Mo and Jianjun Zhou(Shanghai Jiao Tong University, China)	1026
1R-3	A 0.8-3GHz 40dB Dynamic Range CMOS Variable-Gain Amplifier Xingli Huang, Xi Qin, Yajie Qin, Zhiliang Hong(Fudan University, China),Hao Fang(LSI Corporation, China)	1030
1R-4	A Low-Noise WCDMA Transmitter with 25%-duty-cycle LO Generator in 65nm CMOS Haiyi Wang, Peichen Jiang, Tingting Mo,Jianjun Zhou(Shanghai Jiao Tong University, China)	1034

1R-5	Power Amplifier Driver for SDR Transmitter with High Gain Tuning Range and	1038
	Dynamic Power Control	
	Yilei Li, Kefeng Han, Na Yan, Xi Tan and Hao Min(Fudan University, China)	
1 R-6	A 0.18um CMOS 2.5Gbps Pre-Amplifier with AGC	1042

1R-7Aluminum Nitride Reconfigurable RF-MEMS Front-Ends (invited paper)1046Augusto Tazzoli, Matteo Rinaldi, Chengjie Zuo, Nipun Sinha, Jan Van Der
Spiegel, Gianluca Piazza* (University of Pennsylvania, USA)1046

Lin Shaoheng(XIAMEN UX HIGH-SPEED IC CO., LTD, China)

SESSION 2R

Wireless transceiver and building blocks (II)

2R-1	A Low Noise and Highly Linear 2.4-GHz RF Front-End Circuit for Wireless Sensor Networks(invited paper) Chihoon Choi, Joonwoo Choi, and Ilku Nam(Pusan National University, Korea)	1050
2R-2	An Auto-calibrating I/Q Mismatch Scheme for High Image Rejection GPS RF Receiver Lijiong Wang, Tingting Mo, Dongpo Chen(Shanghai Jiao Tong University, China)	1054
2R-3	A Dual-mode Analog Baseband Utilizing Digital-assisted Calibration for WCDMA/GSM Receivers Renzhong Xie, Chen Jiang, Weinan Li, Yumei Huang ,Zhiliang Hong(Fudan University, China)	1058
2R-4	A 0.25dB Gain Step High Linear Programmable Gain Amplifier Xiaobin Shen, Taotao Yan, Yuxiao Lu, Jianjun Zhou(Shanghai Jiao Tong University, China)	1062
2R-5	Reconfigurable Low Pass Filter with Automatic Frequency Tuning for WCDMA and GSM Application Chen Jiang, Renzhong Xie,Weinan Li, Yumei Huang and Zhiliang Hong(FudanUniversity, China)	1066

2R-6	A Wide Tuning Range Low-pass Gm-C Filter for Multi-Mode Wireless Receivers	1070
	with Automatic Frequency Calibration	
	Yu Wang, Na Yan, Hao Min(Fudan University, China)	
	RFIDsense: a Reconfigurable RFID Sensor Tag Platform Conforming to IEEE	1074

2R-7RFIDsense: a Reconfigurable RFID Sensor Tag Platform Conforming to IEEE1071451.7 StandardFeibai Zhu, Min Li, Haichao Han, Junyu Wang(Fudan University, China)107

SESSION 3R

Wireless transceiver and building blocks (III)

3R-1	Directional Coupler Design in 3G/LTE Power Amplifier Module(invited paper) Xiao Wang, Wenjun SHeng, Yang Li(Telink Semiconductor Inc, USA)	1078
3R-2	SiGe HBT Power Amplifier Design using 0.35 um BiCMOS Technology with Through-Silicon-Via(invited paper) Jingyang Zhang, Dasheng Fang(IBM Microelectronics China Design Center, China), Dawn Wang, Hanyi Ding, John Gillis, Wan Ni, Susan Sweeney(IBM Microelectronics, USA)	1082
3R-4	A 0.8-2.5GHz Wideband SiGe BiCMOS Low Noise Amplifier with Noise Fiugre of 1.98-3.3dB Lin Hua, Qiong Yan, Lei Chen,Runxi Zhang, Chunqi Shi, Zongsheng Lai(East China Normal University, China)	1086

3R-6Design of a High-Linearity RF Front-End With IP2 Calibration for SAW-Less1090W-CDMA ReceiverSong Hu, Weinan Li, Yumei Huang*, and Zhiliang Hong(Fudan University, China)1090

Special Session 1S

ESL Design

18-1	Architecture and Design Automation for Application-Specific Processors(invited paper) Philip Brisk(University of California, Riverside, USA)	1094
1S-2	High-Level Synthesis: On the Path to ESL Design(invited paper) Philippe COUSSY, Dominique HELLER, Cyrille CHAVET(Université de Bretagne-Sud, France)	1098
18-3	Study of High-Level Synthesis: Promises and Challenges(invited paper) Kyle Rupnow, Yun Liang, Yinan Li(Advanced Digital Sciences Center), Deming Chen(University of Illinois at Urbana-Champaign)	1102
1S-4	On Virtual Prototying of Embedded System-on-Chip(invited paper) Yi Ni, Wai Sum Mong, Jianwen Zhu(University of Toronto, Canada)	1106