

# **2012 13th International Symposium on Quality Electronic Design**

## **(ISQED 2012)**

**Santa Clara, California, USA  
19-21 March 2012**



**IEEE Catalog Number:** CFP12250-PRT  
**ISBN:** 978-1-4673-1034-5

## TABLE OF CONTENTS

### INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN

<b>Welcome to ISQED 2012 .....</b>	<b>iii</b>
<b>Best Paper Awards .....</b>	<b>iv</b>
<b>Committees .....</b>	<b>v</b>
<b>ISQED Fellow Award .....</b>	<b>x</b>
<b>Sessions at a Glance .....</b>	<b>xi</b>
<b>Calls for Papers – ASQED 2012 and ISQED 2013.....</b>	<b>End pages</b>

#### **SESSION 1A: Test and Measurement**

Chair: Sreejit Chakravarty, LSI Corporation  
 Co-Chair: Srivatsa Vasudevan, Synopsys Inc.

<b>Physical-Design-Friendly Hierarchical Logic Built-In Self-Test – A Case Study .....</b>	<b>1</b>
Kelvin Nelson, Jaga Shanmugavadivelu, Jayanth Mekkoth, Venkat Ghanta, Jun Wu, Fe Zhuang .....	Cisco Systems
Hao-Jan Chao, Shianling Wu, Jie Rao, Lizhen Yu, Laung-Terng Wang .....	SynTest Technologies, Inc.
<b>A Self-Testable SiGe LNA and Built-in-Self-Test Methodology          for Multiple Performance Specifications of RF Amplifiers.....</b>	<b>7</b>
Abhilash Goyal, Madhavan Swaminathan, Abhijit Chatterjee, Duane Howard, John Cressler .....	Georgia Institute of Technology
<b>Improved Path Clustering for Adaptive Path-Delay Testing .....</b>	<b>13</b>
Tuck-Boon Chan and Andrew Kahng .....	UC-San Diego
<b>TSV and DFT Cost Aware Circuit Partitioning for 3D-SOCs.....</b>	<b>21</b>
Amit Kumar, Sudhakar M. Reddy .....	University of Iowa
Irith Pomeranz .....	Purdue University
Bernd Becker .....	Albert Ludwigs University
<b>A Design-For-Test Apparatus for Measuring On-Chip Temperature with Fine Granularity.....</b>	<b>27</b>
James Tandon, Masahiro Sasaki, Makoto Ikeda, Kunihiro Asada .....	University of Tokyo

#### **SESSION 1B: Reliable System Design**

Chair: Payman Zarkesh-Ha, University of New Mexico  
 Co-Chair: Srinivas Bodapati, Intel

<b>Wearout-Aware Compiler-Directed Register Assignment for Embedded Systems.....</b>	<b>33</b>
Fahad Ahmed, Linda Milor .....	Georgia Institute of Technology
Mohamed Sabry, David Atienza .....	Ecole Polytechnique Federale de Lausanne
<b>Process-Variation Aware Mapping of Real-Time Streaming Applications          to MPSoCs for Improved Yield .....</b>	<b>41</b>
Davit Mirzoyan .....	Delft University of Technology
Benny Akesson, Kees Goossens .....	Eindhoven University of Technology
<b>Single Fault Reliability Analysis in FPGA Implemented Circuits .....</b>	<b>49</b>
Hadi Jahanirad, Karim Mohammadi .....	Iran University of Science and Technology
Pejman Attarsharghi .....	Sharif University of Technology
<b>Low Complexity Cross Parity Codes for Multiple and Random Bit Error Correction .....</b>	<b>57</b>
Mahesh Poolakkaparambil, Abusaleh Jabir .....	Oxford Brookes University
Jamison Matthew .....	University of Bristol
, Saraju Mohanty .....	University of North Texas

<b>Delay Insensitive Code-Based Timing and Soft Error-Resilient and Adaptive-Performance Logic.....</b>	<b>63</b>
Bao Liu, Xuemei Chen, Fiona Teshome .....	University of Texas at San Antonio

### **SESSION 1C: System Frameworks and Tools**

Chair: Makram Mansour, Texas Instruments

Co-Chair: Jose Silva Matos, University of Porto

<b>A Particle Swarm Optimization Approach for Synthesizing Application-specific Hybrid Photonic Networks-on-Chip .....</b>	<b>78</b>
Shirish Bahirat and Sudeep Pasricha .....	Colorado State University
<b>A Preliminary Study on System-level Impact of Persistent Main Memory .....</b>	<b>84</b>
Taciano Perez .....	Hewlett Packard Co.
Ney Laert Vilar Calazans, Cesar A. F. De Rose ....	Pontifícia Universidade Católica do Rio Grande do Sul
<b>Optimal Microarchitectural Design Configuration Selection for Processor Hard-Error Reliability .....</b>	<b>91</b>
Ying Zhang, Lide Duan, Bin Li, Lu Peng .....	Louisiana State University
<b>NoC-based Platform for Embedded Software Design: An Extension of the Hellfire Framework .....</b>	<b>97</b>
Felipe Magalhães, Oliver Longhi, Sérgio Filho, Alexandra Aguiar, Fabiano Hessel .....	Pontifícia Universidade Católica do Rio Grande do Sul (PUCRS)

### **SESSION 2A: Thermal and Power in 3D ICs**

Chair: Tan Yan, Synopsys, Inc.

Co-Chair: Martin Wang, UIUC

<b>Thermal Via Structural Design in Three-Dimensional Integrated Circuits .....</b>	<b>103</b>
Leslie Hwang, Kevin Lin, Martin Wong .....	University of Illinois Urbana-Champaign
<b>Functional Test Pattern Generation for Maximizing Temperature in 3D IC Chip Stack .....</b>	<b>109</b>
Sudarshan Srinivasan and Sandip Kundu .....	University of Massachusetts Amherst
<b>Thermal Analysis of 3D Integrated Circuits Based on Discontinuous Galerkin Finite Element Method .....</b>	<b>117</b>
Amir Zjajo, Nick van der Meij, Rene van Leuken .....	Delft University of Technology
<b>Full-chip Thermal Analysis of 3D ICs with Liquid Cooling by GPU-Accelerated GMRES Method .....</b>	<b>123</b>
Xue-Xin Liu, Zao Liu, Sheldon X.-D. Tan, Joseph Gordon .....	University of California, Riverside
<b>Leakage-Aware Performance-Driven TSV-Planning Based on Network flow Algorithm in 3D ICs .....</b>	<b>129</b>
Kan Wang, Sheqin Dong, Yuchun Ma .....	Tsinghua University
Goto Satoshi .....	Waseda University
Jason Cong .....	UCLA
<b>A 3D IC Designs Partitioning Algorithm with Power Consideration .....</b>	<b>137</b>
Ho-Lin Chang, Hsiang-Cheng Lai, Tsu-Yun Hsueh, Wei-Kai Cheng, Mely Chen Chi .....	Chung Yuan Christian University

### **SESSION 2B: Low Power Communication Circuits**

Chair: Syed Alam, Everspin Technologies Inc.

Co-Chair: Dinesh Somasekhar, Global Foundries

<b>Embracing Local Variability to Enable a Robust High-Gain Positive-Feedback Amplifier: Design Methodology and Implementation .....</b>	<b>143</b>
Kareem Ragab, Ranjit Gharpurey, Michael Orshansky .....	University of Texas at Austin

<b>An Ultra-Low Voltage Digitally Controlled Low-Dropout Regulator with Digital Background Calibration .....</b>	<b>151</b>
Yongtae Kim and Peng Li .....	Texas A&M University
<b>Dynamically Biased Low Power High Performance 3.3V Output Buffer in a Single Well Bulk CMOS 1.8V Oxide 45nm Process .....</b>	<b>159</b>
Karthik Rajagopal .....	Texas Instruments
<b>Design of an Efficient NoC Architecture using Millimeter-Wave Wireless Links .....</b>	<b>165</b>
Sujay Deb, Kevin Chang, Xinmin Yu, Partha Pande, Deuk Heo, Benjamin Belzer .....	Washington State University
Amlan Ganguly .....	Rochester Institute of Technology
Christof Teuscher .....	Portland State University
<b>A Novel Robust Signaling Scheme for High-Speed Low-Power Communication over Long Wires ...</b>	<b>173</b>
Marshnil Dave, Maryam Shojaei Baghini, Dinesh Sharma .....	IIT-Bombay
<b>An Extended-Range Incremental CT <math>\Sigma\Delta</math> ADC with Optimized Digital Filter .....</b>	<b>179</b>
Julian Garcia and Ana Rusu .....	KTH Royal Institute of Technology

### **SESSION 2C: Process-Induced Variability & Hot Spot Detection**

Chair: Rajan Beera, Texas Instruments

Co-Chair: Valeriy Sukharev, Mentor Graphics

<b>Test Structure, Circuits and Extraction Methods to Determine the Radius of Influence of STI and Polysilicon Pattern Density .....</b>	<b>185</b>
Albert H. Chang, Duane Boning .....	Massachusetts Institute of Technology
Kewei Zuo, Jean Wang, Douglas Yu .....	Taiwan Semiconductor Manufacturing Company, Ltd.
<b>Post-Placement Lithographic Hotspot Detection and Removal in One-Dimensional Gridded Designs .....</b>	<b>193</b>
Jen-Yi Wuu, Małgorzata Marek-Sadowska .....	University of California, Santa Barbara
Mark Simmons .....	Mentor Graphics Corporation
<b>On Lithography Aware Metal-Fill Insertion .....</b>	<b>200</b>
Vikram Suresh, Priyamvada Vijayakumar, Sandip Kundu .....	University of Massachusetts, Amherst
<b>Understanding, Modeling, and Detecting Pooling Hotspots in Copper CMP .....</b>	<b>208</b>
Aaron Gower-Hall, Tamba Gbondo-Tugbawa, JenPin Weng .....	Cadence Design Systems
Wei-tsung Tseng, Laertis Economikos, Toshiaki Yanagisawa, Pavan Bashaboina, Stephen Greco .....	IBM
<b>Methodology for Analysis of TSV Stress Induced Transistor Variation and Circuit Performance .....</b>	<b>216</b>
Li Yu, Duane Boning .....	Massachusetts Institute of Technology
Wen-Yao Chang, Kewei Zuo, Jean Wang, Douglas Yu .....	Taiwan Semiconductor Manufacturing Company, Ltd.
<b>High Performance Electrical Driven Hotspot Detection Solution for Full Chip Design using a Novel Device Parameter Matching Technique .....</b>	<b>223</b>
Rami Fathy, Mohamed Al-Imam, Abdelrahman ElMously, Haitham Eissa, Ahmed.....ArafaMentor Graphics Mohab Anis .....	American University in Cairo

### **SESSION 3A: Emerging Topics in EDA**

Chair: James Lei, Applied Harmonics Corporation

Co-Chair: Anand Iyer, AMD

<b>Fast Delay Estimation with Buffer Insertion for Through-Silicon-Via-Based 3D Interconnects .....</b>	<b>228</b>
Young-Joon Lee and Sung Kyu Lim .....	Georgia Institute of Technology
<b>Functional Composition: A New Paradigm for Performing Logic Synthesis .....</b>	<b>236</b>
Mayler Martins, Renato Ribas, Andre Reis .....	UFRGS

<b>A New Voltage Binning Technique for Yield Improvement Based on Graph Theory .....</b>	<b>243</b>
Ruijing Shen, Sheldon X.-D. Tan, Xue-Xin Liu .....	University of California, Riverside
<b>A Complete Power Estimation Methodology for DSP Blocks in FPGAs .....</b>	<b>249</b>
Hassan Hassan and Nizar Abdallah .....	Microsemi Corp.
<b>Process Variation Aware DRAM Design Using Block Based Adaptive Body Biasing Algorithm .....</b>	<b>255</b>
Satyajit Desai, Sanghamitra Roy, Koushik Chakraborty .....	Utah State University

### **SESSION 3B: Design & Analysis of Emerging Devices**

Chair: Paul Tong, Pericom Semiconductor  
 Co-Chair: Bao Liu, University of Texas

<b>Device- and System-Level Performance Modeling for Graphene P-N Junction Logic .....</b>	<b>262</b>
Chenyun Pan and Azad Naeemi .....	Georgia Institute of Technology
<b>Quasi-Planar Tri-gate (QPT) Bulk CMOS Technology for Single-Port SRAM Application .....</b>	<b>270</b>
Yasumasa Tsukamoto, Makoto Yabuuchi, Hidehiro Fujiwara, Koji Nii ....	Renesas Electronics Corporation
Changhwan Shin .....	University of Soeul
Tsu-Jae King Liu .....	University of California at Berkeley
<b>A Body-Voltage-Sensing-Based Short Pulse Reading Circuit for Spin-Torque Transfer RAMs (STT-RAMs) .....</b>	<b>275</b>
Fengbo Ren, Henry Park, Richard Dorrance, Yuta Toriyama, C.-K. Ken Yang, Dejan Marković .....	UCLA
<b>Interconnect Analysis in Spin-torque Devices: Performance Modeling, Optimal Repeater Insertion, and Circuit-size Limits .....</b>	<b>283</b>
Shaloo Rakheja and Azad Naeemi .....	Georgia Institute of Technology
<b>Analysis of Crosstalk Delay and Area for MWNT and Bundled SWNT in Global VLSI Interconnects .....</b>	<b>291</b>
Manoj Kumar Majumder, Nisarg D. Pandya, Brajesh Kumar Kaushik, Sanjeev Kumar Manhas .....	Indian Institute of Technology Roorkee

### **SESSION 3C: Variation-Aware Design Methodologies**

Chair: Rajesh Garg, Intel  
 Co-Chair: Riaz Naseer, Intel

<b>Robust Metastability-based TRNG Design in Nanometer CMOS with Sub-Vdd Pre-charge and Hybrid Self-calibration .....</b>	<b>298</b>
Vikram Suresh and Wayne Burleson .....	University of Massachusetts, Amherst
<b>Statistical Observations of NBTI-Induced Threshold Voltage Shifts on Small Channel-area Devices .....</b>	<b>306</b>
Takashi Sato, Hiromitsu Awano, Hirofumi Shimizu, Hiroshi Tsutsui, Hiroyuki Ochi .....	Kyoto University
<b>Error Mitigation in Digital Logic using a Feedback Equalization with Schmitt Trigger (FEST) Circuit .....</b>	<b>312</b>
Zafar Takhirov, Bobak Nazer, Ajay Joshi .....	Boston University
<b>The Combined Effect of Process Variations and Power Supply Noise on Clock Skew and Jitter .....</b>	<b>320</b>
Hu Xu, Vasilis F. Pavlidis, Giovanni De Micheli .....	EPFL
Wayne Burleson .....	University of Massachusetts Amherst
<b>TDDB-Based Performance Variation of Combinational Logic in Deeply Scaled CMOS Technology .....</b>	<b>328</b>
Haiqing Nan, Li Li, Ken Choi .....	Illinois Institute of Technology

## Poster Session

Chair: Mark Budnik, Valpraiso University

Co-Chair: Keith Bowman, Intel

<b>Critical Area Driven Dummy Fill Insertion to Improve Manufacturing Yield .....</b>	<b>334</b>
Nishant Dhumane and Sandip Kundu .....	University of Massachusetts, Amherst
<b>Impact of Transistor Aging Effects on Sense Amplifier Reliability in Nano-Scale CMOS .....</b>	<b>342</b>
Roberto Menchaca and Hamid Mahmoodi .....	San Francisco State University
<b>A Highly Reliable SEU Hardened Latch and High Performance SEU Hardened Flip-Flop .....</b>	<b>347</b>
Riadul Islam .....	Concordia University
<b>A Scalable Curve-fit Model of the Substrate Coupling Resistances for IC Design .....</b>	<b>353</b>
Vijaya Kumar Gurugubelli and Shreepad Karmalkar .....	Indian Institute of Technology Madras
<b>Efficient Reduction Techniques for Statistical Model Generation of Standard Cells .....</b>	<b>358</b>
Sachin Shrivastava and Harindranath Parameswaran .....	Cadence Design Systems
<b>Efficient Electro-Thermal Co-analysis on CPU+GPU Heterogeneous Architecture .....</b>	<b>364</b>
Kun Huang, Xu Yang, Guoxing Zhao, Zuying Luo .....	Beijing Normal University
<b>Dynamic Range Estimation for Systems with Control-flow Structures .....</b>	<b>370</b>
Bin Wu .....	Advanced Micro Devices, Inc.
<b>Comparison of Variations in MOSFET versus CNFET in Gigascale Integrated Systems .....</b>	<b>378</b>
Ali Arabi M. Shahi, Payman Zarkesh-Ha, Mirza Elahi .....	University of New Mexico
<b>Vertical Slit Field Effect Transistor in Ultra-Low Power Applications .....</b>	<b>384</b>
Xiang Qiu, Malgorzata Marek-Sadowska .....	University of California, Santa Barbara
Wojciech Maly .....	Carnegie Mellon University
<b>Design and Optimization of Power Gating for DVFS Applications .....</b>	<b>391</b>
Tong Xu and Peng Li .....	Texas A&M University
<b>An Area Efficient On-Chip Hybrid Voltage Regulator .....</b>	<b>398</b>
Selcuk Kose, Eby Friedman .....	University of Rochester
Simon Tam .....	Intel Corporation
Sally Pinzon, Bruce McDermott .....	Eastman Kodak
<b>Device and Electromagnetic Co-simulation of TSV: Substrate Noise Study and Compact Modeling of a TSV in a Matrix .....</b>	<b>404</b>
Patrick Le Maitre, Melanie Brocard, Alexis Farcy, Jean-Claude Marin .....	STMicroelectronics
<b>A Case for 3D Stacked Analog Circuits in High-Speed Sensing Systems .....</b>	<b>412</b>
Mohammad Abdel-Majeed, Mike S.W. Chen, Murali Annavaram .....	University of Southern California
<b>A DyadicCluster Method Used for Nonlinear Placement .....</b>	<b>418</b>
Wenchao Gao, Xu Qian .....	China University of Mining and Technology
Wenchao Gao, Qiang Zhou, Yici Cai .....	Tsinghua University
<b>Clock Mesh Framework .....</b>	<b>424</b>
Pinaki Chakrabarti, Dwight Hill, Aiqun Cao .....	Synopsys Inc.
Vikram Bhatt .....	University of California, San Diego
<b>Placement Aware Clock Gate Cloning and Redistribution Methodology .....</b>	<b>432</b>
Vishweshwara Ramamurthy, Mahita Nagabhiru, Venkatraman Ramakrishnan .....	Texas Instruments India
<b>Impact of C-Elements in Asynchronous Circuits .....</b>	<b>437</b>
Matheus Moreira, Bruno Oliveira, Fernando Moraes, Ney Calazans .....	PUCRS
<b>A Top-Down Design Methodology using Virtual Platforms for Concept Development .....</b>	<b>444</b>
Mohit Shah, Chaitali Chakrabarti, Andreas Spanias .....	Arizona State University
Brian Mears .....	Intel Corporation
<b>Partitioning and Dynamic Mapping Evaluation for Energy Consumption Minimization on NoC-Based MPSoC .....</b>	<b>451</b>
Eduardo Antunes, Matheus Soares, Alexandra Aguiar, Sergio Johann F., Marcos Sartori, Fabiano Hessel, Cesar Marcon .....	Pontifical University Catholic of Rio Grande do Sul

## **SESSION 4A: Physical Design**

Chair: Makoto Ikeda, University of Tokyo  
Co-Chair: Martin Wang, UIUC

<b>Ordinary Kriging Metamodel-Assisted Ant Colony Algorithm for Fast Analog Design Optimization .....</b>	<b>458</b>
Oghenekarho Okobiah, Saraju Mohanty, Elias Kougianos .....	University of North Texas
<b>CMOS Op-amp Circuit Synthesis with Geometric Programming Models for Layout-Dependent Effects .....</b>	<b>464</b>
Yu Zhang, Bo Liu, Bo Yang, Jing Li, Shigetoshi Nakatake .....	The University of Kitakyushu
<b>DRC-Free High Density Layout Exploration with Layout Morphing and Patterning Quality Assessment, with Application to SRAM .....</b>	<b>470</b>
Amith Singhee, Emrah Acar, Mohammad Younus, Rama Singh, Aditya Bansal .....	IBM Corp.
<b>Hierarchical Power Network Synthesis for Multiple Power Domain Designs .....</b>	<b>477</b>
Chieh-Jui Lee, Sean Shih-Ying Liu, Chuan-Chia Huang, Hung-Ming Chen .....	National Chiao Tung University
Chang-Tzu Lin, Chia-Hsin Lee .....	Industrial Technology Research Institute
<b>Algorithmic Study on the Routing Reliability Problem .....</b>	<b>483</b>
Qiang Ma, Zigang Xiao, Martin D. F. Wong .....	University of Illinois at Urbana-Champaign

## **SESSION 4B: Robust SRAM Design**

Chair: Srinivas Bodapati, Intel  
Co-Chair: Hamid Mahmoodi, SFSU

<b>A 40-nm 256-Kb 0.6-V Operation Half-Select Resilient 8T SRAM with Sequential Writing Technique Enabling 367-mV VDDmin Reduction .....</b>	<b>489</b>
Masaharu Terada, Shusuke Yoshimoto, Shunsuke Okumura, Hiroshi Kawaguchi, Masahiko Yosimoto .....	Kobe University
Toshikazu Suzuki, Shinji Miyano .....	Semiconductor Technology Academic Research Center (STARC)
<b>Process Variation Tolerant 9T SRAM Bitcell Design .....</b>	<b>493</b>
G. K. Reddy, Kapil Jainwal .....	Jaypee University of Engineering & Technology
Jawar Singh .....	Indian Institute of Information Technology, Design and Manufacturing
Saraju P. Mohanty .....	University of North Texas
<b>History &amp; Variation Trained Cache (HVT-Cache): A Process Variation Aware and Fine Grain Voltage Scalable Cache with Active Access History Monitoring .....</b>	<b>498</b>
Avesta Sasan, Kiarash Amiri, Ahmed Eltawil, Fadi Kurdahi .....	University of California Irvine
Houman Homayoun .....	University of California San Diego
<b>VAR-TX: A Variability-Aware SRAM Model for Predicting the Optimum Architecture to Achieve Minimum Access-Time for Yield Enhancement in Nano-scaled CMOS .....</b>	<b>506</b>
Jeren Samandari-Rad, Matthew Guthaus, Richard Hughey .....	University of California, Santa Cruz
<b>Bit Error Rate Estimation in SRAM Considering Temperature Fluctuation .....</b>	<b>516</b>
Yuki Kagiyama, Shunsuke Okumura, Koji Yanagida, Shusuke Yoshimoto, Yohei Nakata, Shintaro Izumi, Hiroshi Kawaguchi, Masahiko Yoshimoto .....	Kobe University

## **SESSION 4C: 3D Effects on Package Co-Design**

Chair: Kamesh Gadeppally, Texas Instruments  
Co-Chair: Lalitha Immaneni, Intel

<b>Chip-Package Power Delivery Network Resonance Analysis and Co-design Using Time and Frequency Domain Analysis Techniques .....</b>	<b>520</b>
Jonathan Watkins .....	Maxim
Jai Pollayil, Calvin Chow, Aveek Sarkar .....	Apache Design Inc.

<b>Maintaining Power Integrity by Damping the Cavity-Mode Anti-Resonances' Peaks on a Power Plane by Particle Swarm Optimization .....</b>	<b>525</b>
Jai Narayan Tripathi, Jayanta Mukherjee .....	Indian Institute of Technology Bombay
Raj Kumar Nagpal, Nitin Kumar Chhabra, Rakesh Malik .....	STMicroelectronics Pvt. Ltd.
<b>A Design Tradeoff Study with Monolithic 3D Integration .....</b>	<b>529</b>
Chang Liu and Sung Kyu Lim .....	Georgia Institute of Technology
<b>Cost-minimized Double Die DRAM Packaging for Ultra-High Performance DDR3 and DDR4 Multi-Rank Server DIMMs .....</b>	<b>537</b>
Richard Crisp, Wael Zohni, Bel Haba .....	Invensas Corp
Bill Gervasi .....	Discobolus Designs
 <b>SESSION 5A: Advanced Analysis &amp; Characterization for Sub-Micron Design</b>	
Chair: Masahiro Fujita, University of Tokyo	
Co-Chair: Anand Iyer, AMD	
<b>Speed-path Analysis for Multi-path Failed Latches with Random Variation .....</b>	<b>545</b>
Tsutomu Ishida, Izumi Nitta, Katsumi Homma, Yuji Kanazawa, Hiroaki Komatsu .....	Fujitsu, Ltd.
<b>HiSIM-RP: A Reverse-Profiling Based 1st Principles Compact MOSFET Model and its Application to Variability Analysis of 90nm and 40nm CMOS .....</b>	<b>553</b>
Hironori Sakamoto, Shigetaka Kumashiro .....	Renesas Electronics Corp.
Shigeo Sato .....	Fujitsu Semiconductor Ltd.
Naoki Wakita .....	Toshiba Corp.
Tohru Mogami .....	NEC Corp.
<b>An Accurate Current Source Model for CMOS Based Combinational Logic Cell .....</b>	<b>561</b>
Baljit Kaur, Sandeep Vundavalli, Sanjeev Kumar Manhas, Sudeb Dasgupta, Anand Bulusu .....	Indian Institute of Technology, Roorkee
<b>Efficient Approaches to Overcome Non-Convexity Issues in Analog Design Automation .....</b>	<b>566</b>
Supriyo Maji and Pradip Mandal .....	Indian Institute of Technology, Kharagpur
<b>Optimization of Importance Sampling Monte Carlo using Consecutive Mean-shift Method and its Application to SRAM Dynamic Stability Analysis .....</b>	<b>572</b>
Takeshi Kida, Yasumasa Tsukamoto, Yuji Kihara .....	Renesas Electronics Corporation
<b>Metamodel-Assisted Ultra-Fast Memetic Optimization of a PLL for WiMax and MMDS Applications .....</b>	<b>580</b>
Oleg Garitselov, Saraju Mohanty, Elias Kougianos, Oghenekarho Okobiah .....	University of North Texas
 <b>SESSION 5B: Power-Aware Design</b>	
Chair: Cheng Zhuo, Intel	
Co-Chair: Mark Budnik, Valparaiso University	
<b>24% Power Reduction by Post-Fabrication Dual Supply Voltage Control of 64 Voltage Domains in <math>V_{DD\min}</math> Limited Ultra Low Voltage Logic Circuits .....</b>	<b>586</b>
Tadashi Yasufuku, Yu Pu, Yun Fei Zheng, Ryo Takahashi, Masato Sasaki, Hiroshi Fuketa, Makoto Takamiya, Takayasu Sakurai .....	University of Tokyo
Koji Hirairi, Atsushi Muramatsu, Masahiro Nomura, Hirofumi Shinohara .....	Semiconductor Technology Academic Research Center
<b>Enhancing Efficiency and Robustness of a Photovoltaic Power System under Partial Shading .....</b>	<b>592</b>
Yanzhi Wang, Xue Lin, Massoud Pedram .....	University of Southern California
Younghyun Kim, Naehyuck Chang .....	Seoul National University
<b>Comparison between Power Gating and DVFS from the Viewpoint of Energy Efficiency .....</b>	<b>601</b>
Atsuki Inoue .....	Fujitsu Laboratories. Ltd.

<b>Design of Low-Power, Scalable-Throughput Systems at Near/Sub Threshold Voltage .....</b>	<b>609</b>
Meeta Srivastav, Michael Henry, Leyla Nazhandali .....	Virginia Tech University
<b>Analysis and Evaluation of Greedy Thread Swapping Based Dynamic Power Management for MPSoC Platforms .....</b>	<b>617</b>
Chirag Ravishankar, Sundaram Ananthanaryanan, Siddharth Garg, Andrew Kennings .....	University of Waterloo
Sundaram Ananthanaryanan .....	Anna University
<b>Efficient Leakage Power Saving by Sleep Depth Controlling for Multi-mode Power Gating .....</b>	<b>625</b>
Seidai Takeda, Shinobu Miwa, Hiroshi Nakamura .....	The University of Tokyo
Kimiyoshi Usami .....	Shibaura Institute of Technology

### **SESSION 5C: Circuit-Level Variability & Manufacturability**

Chair: Shubhankar Basu, Global Foundries

Co-Chair: Saraju Mohanty, University of North Texas

<b>DDRO: A Novel Performance Monitoring Methodology Based on Design-Dependent Ring Oscillators .....</b>	<b>633</b>
Tuck-Boon Chan, Andrew Kahng .....	UC San Diego
Puneet Gupta, LiangZhen Lai .....	UCLA
<b>An Analytical Approach to Efficient Circuit Variability Analysis in Scaled CMOS Design .....</b>	<b>641</b>
Samatha Gummalla, Anupama R Subramaniam, Yu Cao, Chaitali Chakrabarti ....Arizona State University	
<b>Process Mismatch Analysis based on Reduced-Order Models .....</b>	<b>648</b>
Mustafa B Yelten, Paul D Franzon, Michael B Steer .....	North Carolina State University
<b>Transistor Channel Decomposition for Structured Analog Layout, Manufacturability and Low-power Applications .....</b>	<b>656</b>
Qing Dong, Bo Yang, Gong Chen, Jing Li, Shigetoshi Nakatake .....	The University of Kitakyushu
<b>Theory of Redundancy for Logic Circuits to Maximize Yield/Area .....</b>	<b>663</b>
Mohammad Mirza-Aghatabar, Melvin A. Breuer, Sandeep K. Gupta, Shahin Nazarian .....	University of Southern California
<b>A Novel Sample Reuse Methodology for Fast Statistical Simulations with Applications to Manufacturing Variability .....</b>	<b>672</b>
Rouwaida Kanj and Rajiv Joshi .....	IBM Corp.
Rouwaida Kanj .....	American University of Beirut

### **SESSION 6A: Verification & Silicon Debug**

Chair: Srivatsa Vasudevan, Synopsys Inc.

Co-Chair: Sreejit Chakravarty, LSI Corporation

<b>Monitoring and Timing Prediction in Early Analyzing and Checking Performance of Interconnection Networks at ESL .....</b>	<b>679</b>
Mao-Yin Wang and Jen-Chieh Yeh .....	Industrial Technology Research Institute
<b>Automated Correction of Design Errors by Edge Redirection on High-Level Decision Diagrams ....</b>	<b>686</b>
Anton Karputkin, Raimund Ubar, Mati Tombak, Jaan Raik .....	Tallinn University of Technology
<b>Assertion Clustering for Compacted Test Sequence Generation .....</b>	<b>694</b>
Jason Tong, Dr. Zeljko Zilic .....	McGill University
Marc Boulé .....	École de Technologie Supérieure
<b>Transaction-Based Post-Silicon Debug of Many-Core System-on-Chips .....</b>	<b>702</b>
Amir Masoud Gharehbaghi and Masahiro Fujita .... University of Tokyo & Japan Science and Technology	
<b>An Enhanced Debug-Aware Network Interface for Network-on-Chip .....</b>	<b>709</b>
M. H. Neishaburi and Zeljko Zilic .....	McGill University

## **SESSION 6B: Challenges & Opportunities in New Technologies**

Chair: Paul Tong, Pericom Semiconductor

Co-Chair: Bao Liu, University of Texas

<b>Process Induced Mechanical Stress Aware Poly-Pitch Optimization for Enhanced Circuit Performance .....</b>	<b>717</b>
Naushad Alam, Bulusu Anand, Sudeb Dasgupta .....	Indian Institute of Technology Roorkee
<b>Design Issues and Insights of Multi-Fin Bulk Silicon FinFETs .....</b>	<b>723</b>
Hsun Li and Meng-Hsueh Chiang .....	National Ilan University
<b>Self-Heating Effects in Gate-all-around Silicon Nanowire MOSFETs: Modeling and Analysis .....</b>	<b>727</b>
Xin Huang, Tianwei Zhang, Runsheng Wang, Changze Liu, Yuchao Liu, Ru Huang .....	Peking University
<b>Comparison of Electrical, Optical and Plasmonic On-Chip Interconnects Based on Delay and Energy Considerations .....</b>	<b>732</b>
Shaloo Rakheja and Vachan Kumar .....	Georgia Institute of Technology
<b>Design Quality Tradeoff Studies for 3D ICs Built with Nano-scale TSVs and Devices .....</b>	<b>740</b>
Kaiyuan Yang .....	Tsinghua University
Dae Hyun Kim, Sung Kyu Lim .....	Georgia Institute of Technology

## **SESSION 6C: Energy-Aware System Design**

Chair: Lech Jozwiak, Eindhoven University of Technology

Co-Chair: Rajesh Berigei, Texas Instruments

<b>Learning Based DVFS for Simultaneous Temperature, Performance and Energy Management .....</b>	<b>747</b>
Hao Shen, Qinru Qiu .....	Syracuse University
Jun Lu .....	Binghamton University
<b>Hot Peripheral Thermal Management to Mitigate Cache Temperature Variation .....</b>	<b>755</b>
Houman Homayoun, Vasileios Kontoniris, Dean Tullsen .....	University of California, San Diego
Mehryar Rahmatian, Shahin Golshan .....	University of California, Irvine
<b>Power-Performance Yield Optimization for MPSoCs Using MILP .....</b>	<b>764</b>
Kshitij Bhardwaj, Sanghamitra Roy, Koushik Chakraborty .....	Utah State University
<b>A Variation and Energy Aware ILP Formulation for Task Scheduling in MPSoC .....</b>	<b>772</b>
Mahboobeh Ghorbani .....	University of Southern California
<b>Register Binding and Domain Assignment for Multi-Domain Clock Skew Scheduling-Aware High-Level Synthesis .....</b>	<b>778</b>
Keisuke Inoue and Mineo Kaneko .....	Japan Advanced Institute of Science and Technology