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JOINT PLENARY SESSION

- JK1 Advances in Computing ~~FFFF~~
- JK2 Gaining 10x in Power Efficiency in the Next Decade in Consumer Products ~~FFFF~~

JOINT SESSION I: Smart Handheld Platform (All Invited Talks)

- JSI1 Powerful Smartphone Solutions Unleashing New Technology Innovations ~~FFFF~~
- JSI2 Disruptive Technologies for Future Generation Smart Systems ~~FFFF~~
- JSI3 The 2012 ARM Powered Compute Subsystem – Delivering the Smart Handheld Platform ~~FFFF~~
- JSI4 Google's C/C++ Toolchain for Smart Handheld Devices ~~FFFF~~
- JSI5 Touch Techniques in Smart Handheld Device ~~FFFF~~

SESSION 2: CMOS

- T21 Advanced Channel and Contact Technologies for Future CMOS Devices (Invited) ~~FFFF~~H
- T22 On The Amplitude of Random Telegraph Noise ~~FFFF~~I
- T23 New Observations on the AC Random Telegraph Noise (AC RTN) in nano-MOSFETs ~~FFFF~~I
- T24 32nm Strained Nitride MTP Cell by Fully CMOS Logic Compatible Process ~~FFFF~~J
- T25 New Criteria for the RDF Induced Drain Current Variation Considering Strain and Transport Effects ~~FFFF~~F
- in Strain-Silicon CMOS Devices
- T26 Ultra-Thin-Body $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ -on-Nothing N-MOSFET with Pd-InGaAs Source/Drain Contacts ~~FFFF~~G
- Enabled by a New Self-Aligned Cavity Formation Technology
- T27 Embedded Metal Source/Drain ($e\text{MSD}$) for Series Resistance Reduction in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ N-Channel ~~FFFF~~G
- Ultra-Thin Body Field-Effect Transistor (UTB-FET)
- T28 Metal Stanogermanide Contacts with Enhanced Thermal Stability for High Mobility Germanium-Tin ~~FFFF~~G
- Field-Effect Transistor
- T29 PMOSFET Layout Dependency with Embedded SiGe Source/Drain at POLY and STI Edge in ~~FFFF~~G
- 32/28nm CMOS Technology

SESSION 3: Gate Stack

- T31 A Study of Novel ALD Beryllium Oxide as an Interface Passivation Layer for Si MOS Devices ~~FFFF~~F
- T32 Gate-First TiAlN P-Gate Electrode for Cost Effective High-k Metal Gate Implementation ~~FFFF~~H
- T33 Simple FinFET Gate Doping Technique for Dipole-Engineered V_t Tuning and CET Scaling ~~FFFF~~I
- T34 III-V Gate Stack Interface Improvement to Enable High Mobility 11nm node CMOS ~~FFFF~~I
- T35 Impact of 45° Rotated Substrate on UTBOX FDSOI High-k Metal Gate Technology ~~FFFF~~J
- T36 Systematical Investigation and Physical Mechanism of HfO_2 Gate Stacks Band Alignment, V_{FB} Shift ~~FFFF~~F
- and Fermi Level Pinning
- T37 Challenges of III-V Materials in Advanced CMOS Logic (Invited) ~~FFFF~~H
- T38 PBTI Improvement in Gate Last HfO_2 Gate Dielectric nMOSFET due to Zr Incorporation ~~FFFF~~I
- T39 Characteristics of HfZrO_x Gate Stack Engineering for Reliability Improvement on 28nm HK/MG ~~FFFF~~I
- CMOS Technology
- T310 Understanding and Improving SILC Behavior under TDDB Stress in Full Gate-Last High-k/Metal ~~FFFF~~J
- Gate nMOSFETs

VLSI-TSA PLENARY SESSION I

- K1 Thin Body FinFET as Low-Voltage Transistors (Keynote) ~~FFFF~~F

SESSION 4: SRAM/DRAM

- T41 A High Density Cylinder-Type MIM Capacitor Integrated with Advanced 28nm Logic High-K/Metal-Gate Process for Embedded DRAM
- T42 Intrinsic MOSFET Leakage of High-k Peripheral DRAM Devices: Measurement and Simulation
- T43 A 20nm Low-Power Triple-Gate Multibody 1T-DRAM Cell
- T44 Optimizing State-of-the-Art 28nm core/SRAM Device Performance by Cryo-Implantation Technology
- T45 Impact of Fin Height Variations on SRAM Yield
- T46 Comparison of Differential and Large-Signal Sensing Scheme for Subthreshold/Superthreshold FinFET SRAM Considering Variability

SESSION 5: Fabrication

- T51 Enabling the Use of I_{on} Implantation for Ultra-thin FDSOI n-MOSFETs
- T52 Improvements in Low Temperature (<625°C) FDSOI Devices Down to 30nm Gate Length
- T53 Novel Selenium Implant and Segregation for Reduction of Effective Schottky Barrier Height in NiGe/n-Ge Contacts
- T54 Key Enabling Technologies of 300mm 3DIC Process Integration
- T55 Simultaneous Formation of Electrical Connection, Mechanical Support and Hermetic Seal with Bump-less Cu-Cu Bonding for 3D Wafer Stacking
- T56 Electrical Characterization and Reliability Investigations of Cu TSVs with Wafer-Level Cu/Sn-BCB Hybrid Bonding

SESSION 6: RRAM/SONOS

- T61 Stabilization of Resistive Switching with Controllable Self-Compliant Ta₂O₅-based RRAM
- T62 Suppressed Soft-errors and Highly Reduced Current for HfO_x Based Unipolar RRAM by Inserting AlO_x Layer
- T63 Modeling and Tuning the Filament Properties in RRAM Metal Oxide Stacks for Optimized Stable Cycling
- T64 Superior Filament Formation Control in HfO₂ Based RRAM for High-performance Low-power Operation of 1 μ A to 20 μ A at +/- 1V
- T65 Logic/Resistive-switching Hybrid Transistor for Two-bit-per-cell Storage
- T66 P-Channel Schottky Barrier Nanowire SONOS Memory with Low-Voltage Operations and Excellent Reliability

JOINT SESSION II: New Memory System (All Invited Talks)

- JSII1 Transforming Memory Systems: Optimizing for Client Value on Emerging Workloads
- JSII2 Emerging Memory Technology Perspective
- JSII3 Review of 3D High Density Storage Class Memory (SCM) Architecture
- JSII4 Computer Architecture for Die Stacking

SESSION 7: Technology Transition (All Invited Talks)

- T71 MOSFETs Transitions towards Fully Depleted Architectures
- T72 Transition to EUV Lithography
- T73 Planar Interconnects to 3D Interconnects

T74 Transition of Memory Technologies

SESSION 8: Novel Device

- T81 Z²-FET: A Zero-slope Switching Device with Gate-controlled Hysteresis
- T82 PBTI Characteristics of N-Channel Tunneling Field Effect Transistor with HfO₂ Gate Dielectric: New Insights and Physical Model
- T83 Multi-Input/Multi-Output Relay Design for More Compact and Versatile Implementation of Digital Logic with Zero Leakage
- T84 Impacts of Wire-LER on Nanowire MOSFET Devices, Subthreshold SRAM and Logic Circuits
- T85 Nano Carbon Devices and Applications (Invited)
- T86 A High Efficient and Compact Charge Pump with Multi-pillar Vertical MOSFET
- T87 AlGaN/GaN-on-Silicon MOS-HEMTs with Breakdown Voltage of 800 V and On-State Resistance of 3 mΩ.cm² using a CMOS-Compatible Gold-Free Process
- T88 Optimization of Control Gate Material and Structure for Enhancing 20nm 64Gb NAND Flash Reliability

TSA PLENARY SESSION II

- K2 Reliability Challenges of Advanced CMOS Process and Product Development: Design and Application Aware Qualification (Keynote)

SESSION 9: Memory

- T91 Optimization of Programming Current on Endurance of Phase Change Memory
- T92 Scaling Behavior of PCM Cells in Off-State Conduction
- T93 Excellent Resistive Switching Memory: Influence of GeO_x in WO_x Mixture
- T94 Emerging Memory Technologies: Challenges and Opportunities (Invited)
- T95 Improvement of Resistive Switching Memory Parameters Using IrO_x Nanodots in High-k AlO_x Cross-Point

SESSION 10: FinFET/Multi Gate Device

- T101 Performance and Variability in Multi-V_T FinFETs Using Fin Doping
- T102 On the R_{series} Extraction Techniques for sub-22nm CMOS FinFET and SiGe Technologies
- T103 Comparative Study of Geometry-dependent Capacitances of Planar FETs and Double-Gate FinFETs: Optimization and Process Variation
- T104 Body Effect Induced Variability in Bulk Tri-gate MOSFETs
- T105 Impact of Thermal Budget on Dopant-Segregated (DS) Metal S/D Gate-All-Around (GAA) PFETs
- T106 Investigation of Scalability for Ge and InGaAs Channel Multi-Gate NMOSFETs