2012 IEEE COOL Chips XV

Yokohama, Japan
18-20 April 2012

IEEE Catalog Number: CFP12COL-PRT
ISBN: 978-1-4673-1201-1

Final Program

April 18, 2012 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

13:00-15:30 **Special Session 1**
Co-chairs: Hiroyuki Tomiyama (Ritsumeikan University)

13:00-15:30 **Advanced Virtual Prototyping of Multiprocessor Systems on Chip**
Speaker: Frédéric Pétrot (TIMA Laboratory, France)

Abstract: Virtual prototyping is a technology whose goal is to simulate the behavior of an entire digital system, including the software running on the processors, and the digital hardware. It relies on specific modeling approaches, at different levels of abstraction, so that speed/accuracy trade-offs can be made. This talk will review the challenges of virtual prototyping techniques, and introduce the level of abstractions that have been agreed upon. We will then more specifically focus on the interpretation of software codes and detail two techniques, an interpretive one based on dynamic binary translation and a native one making use of hardware assisted virtualization.

15:30-16:00 **Break**

16:00-18:30 **Special Session 2**
Co-chairs: Hiroyuki Tomiyama (Ritsumeikan University)

16:00-18:30 **Analyzing Embedded Processor Behavior in the Age of Complex SoCs**
Speaker: Markus Levy (EEMBC, U.S.A.)

Abstract: Drawing on the experience of the Embedded Microprocessor Benchmark Consortium (EEMBC), this presentation will detail the methodology used to develop benchmarks that target horizontal technologies such as floating-point and multicore and vertical technologies such as smartphones, automotive, and Android. In addition to performance-related aspects, I will also discuss battery-life measurement techniques for smartphones, a subject that is often fraught with misinterpretation and abuse. The advanced development effort of these benchmarks is faced with many challenges such as ensuring repeatability, portability, and the ability to defeat unwarranted optimizations. Furthermore, these diverse and popular topics present the design engineer with unique challenges in trying to understand how to analyze the embedded processor and system behavior. Therefore, this presentation will also explain how to apply these benchmark techniques to designing next-generation processors and systems, as well as for system designers making tradeoffs between performance and power.

April 19, 2012 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
(Yokohama Media & Communications Center)

9:30-10:40 **Session I**

9:30-9:50 **Welcome and Opening Remarks**
Chair: Kazumasa Suzuki (Renesas Electronics)

Hiroaki Kobayashi,	*Chair of the Organizing Committee*
Donald. A. Draper,	*Chair of TCMCOMP*
Fumio Koyama,	*President of Electronics Society, IEICE*
Fumiko Hayashi,	*Mayor of Yokohama City*

9:50-10:40 **Keynote Presentation 1**
Co-chairs: Ryusuke Egawa (Tohoku University), Makoto Ikeda (University of Tokyo)

The Expanding Universe of Embedded Imaging
Masaki Hiraga (Morpho)

Abstract: Embedded devices have been evolving at a tremendous speed for the past 10 years, especially mobile phones. Multi-core CPUs and GPGPUs are becoming ever so popular and the resolution of display devices as well as digital cameras keep increasing. Image processing is mainly performed in parallel, so it has high compatibility with the advancement of hardware. As a result, highly complex imaging technology which was once used only on super computers and workstations now runs on embedded devices. By combining imaging technology with portability of mobile devices and network communications, image processing applications with new concepts are now emerging into the market. In this session, the evolution of mobile phone hardware and software in the past 10 years will be looked upon from image processing perspective, and the present and future imaging technology will be elaborated.

10:40-11:00 **Break**

11:00-11:50 **Session II: Object Recognition**
Co-Chairs: Abderazek Ben-Abdallah (University of Aizu), Yuichiro Shibata (Nagasaki University)

11:00-11:25 **A Simultaneous Multithreading Heterogeneous Object Recognition Processor with Machine Learning Based Dynamic Resource Management** **1**
Jinwook Oh, Gyeonghoon Kim, Junyoung Park, Injoon Hong, Seungjin Lee, Joo-Young Kim, Hoi-Jon Yoo (KAIST, Korea)

11:25-11:50 **Dual-Stage Hardware Architecture of On-Line Clustering with High-Throughput Parallel Divider for Low-Power Signal Processing** **4**
Tse-Wei Chen, Makoto Ikeda (University of Tokyo)

11:50-12:30 **Session III : Poster Short Speeches** **7**
Chair: Koji Hashimoto (Fukuoka University)

Poster 1 **Energy Saving of BTB by Focusing on Useless References**
Yoshio Shimomura, Hayato Usui, Genta Abe, Ryotaro Kobayashi (Toyohashi University of Technology)

Poster 2 **A Reduction Technique of Static Power Consumption of Scratch-Pad Memory by Dynamic Switching of SPM Block**
Shoma Kawai, Takashi Morimoto, Ryotaro Kobayashi (Toyohashi University of Technology)

Poster 3 **A Preliminary Study on Reducing Cache Size by Focusing on Data Redundancy**
Daisuke Matsukawa, Yoshio Shimomura, Ryotaro Kobayashi (Toyohashi University of Technology)

Poster 4 **A Preliminary Study on Value Consistency for Preload**
Kazuki Sekikawa, Hayato Usui, Yoshio Shimomura, Ryotaro Kobayashi (Toyohashi University of Technology)

Poster 5 **A Low Power SRAM Design with Segmented Stacking Technique**
Shuang-An Tseng, Tung-Chi Wu, Yen-Jen Chang (National Chung Hsing University, Taiwan)

Poster 6 **Synthesis and Implementation of Low Power Logic Cells**
Tsung-Yi Wu, Tai-Lun Li, Hao-Lung Hsueh (National Changhua University of Education, Taiwan)

Poster 7 **High-Performance Low-Power Motion Estimation Algorithm and C Code for ATmega328 and ARM Cortex-M3**
Tsung-Yi Wu, Tsung-Che Lee, Yu-Sheng Wu (National Changhua University of Education, Taiwan)

Poster 8 **Low-Area, High-Speed Logarithmic and Anti-logarithmic Converters for Digital Signal Processors Based on Hybrid Number System**
Van-Phuc Hoang, Cong-Kha Pham (University of Electro-Communications)

Poster 9 **A Branch Target Address Predictor for Reducing the BTB Miss by Using CAM**
Lin Meng, Takeshi Kumaki, Katsuhiro Yamazaki, Takeshi Ogura, Shigeru Oyanagi (Ritsumeikan University)

Poster 10 **Co-design of the Extremely Scalable Algorithms/Architecture for 3D Discrete Transforms**
Stanislav G. Sedukhin, Toshiaki Miyazaki, Kenichi Kuroda (University of Aizu)

Poster 11 **A Bypass Mechanism for Way-Adaptable Caches**
Takumi Takai, Yusuke Tobo, Masayuki Sato, Ryusuke Egawa, Hiroyuki Takizawa, Hiroaki Kobayashi (Tohoku University)

Poster 12 **Application Development for a Heterogeneous Multi-Core Processor**
Yusuke Koizumi[1], Eiichi Sasaki[1], Mitaro Namiki[2], Hideharu Amano[1] ([1]Keio University, [2]Tokyo University of Agriculture & Technology)

Poster 13 **Design Exploration of PE Array Networks for Cool Mega Array**
Rie Uno, Nobuaki Ozaki, Hideharu Amano (Keio University)

Poster 14 **Extension of memory controller equipped with MuCCRA-3**
Toru Katagiri, Kazuei Hironaka, Hideharu Amano (Keio University)

Poster 15 **A Fine-Grained Power Gating Control for a Real Time Operating System**
Yumi Shimada[1], Hiroaki Kobayashi[1], Akihiro Takahashi[1], Ryuiti Sakamoto[1], Mikiko Sato[1], Masaaki Kondo[2], Hideharu Amano[3], Hiroshi Nakamura[4], Mitaro Namiki[1]

([1]Tokyo University of Agriculture & Technology, [2]University of Electro-Communication, [3]Keio University, [4]University of Tokyo)

Poster 16 **A Hardware Edge Detector of an Image Based on a Bump Circuit and the Neighbor Pixels**
Kwang-Seok Oh , Sang-Jin Lee, Kyoungrok Cho (Chungbuk National University, Korea)

Poster 17 **Application of SerDes for FPGA-based digital DC-DC Converters**
Yoshihiko Yamabe, Kanako Nakashima, Keisuke Dohi, Kazuhiro Kajiwara, Fujio Kurokawa, Yuichiro Shibata (Nagasaki University)

Poster 18 **A Design Methodology for High-Performance D/A Converter utilizing Optimized Weights**
Daisuke Kanemoto, Haruichi Kanaya, Keiji Yoshida, Ramesh Pokharel (Kyushu University)

Poster 19 **Enhancing Simulation Performance of Network-on-Chip by Using Multi-core Systems**
Kuei-Chung Chang (Feng Chia University, Taiwan)

Poster 20 **Simple On-chip Optical Interconnection for Improving Performance of Coherency Traffic in CMPs**
Sandro Bartolini, Paolo Grani (University of Siena, Italy)

Poster 21 **Distributed Computing Circuits in Scalable 2D/3D FPGA Array for 2D/3D Poisson Equation Problem**
Jiang Li, Kenichi Takahashi, Hakaru Tamukoh, Masatoshi Sekine (Tokyo University of Agriculture & Technology)

Poster 22 **Scheduling Sensor IO for Minimizing Battery Consumption and Voltage Drop in Sensor Node**
Qian Zhao[1], Shimpei Yamada[1], Yukikazu Nakamoto[1], Koutaro Yamamura[2], Makoto Iwata[2], Masayoshi Kai[2] ([1]University of Hyogo, [2]NEC System Technologies)

12:30-14:00 **Lunch Time Break**

14:00-14:50 **Session IV**
Co-chairs: Kohji Takano (IBM), Yusuke Nitta (Renesas Electronics)

14:00-14:50 **<u>Keynote Presentation 2</u>**
The IBM Blue Gene/Q Supercomputer
George Liang-Tai Chiu (IBM, U.S.A.)

Abstract: Blue Gene/Q™ is the third generation in the IBM Blue Gene® line of massively parallel supercomputer systems, and is scalable to deliver a peak performance of twenty PetaFLOP/s and beyond. The aim of the Blue Gene platform remains the same, namely to build a massively parallel high performance computing (HPC) system out of highly power-efficient processor chips. Such power-efficient chips, in turn, allow very dense packaging, which consequently results in superior power efficiency, space utilization, and total cost of ownership. A focus on reliability during all phases of the design also contributes to the feasibility of scaling to large but reliable systems. The heart of a Blue Gene/Q system is its Compute chip, implemented as a System-on-a-Chip (SOC) design. It combines processors, memory hierarchy and network communications on a single ASIC. Integrating these functions on a single chip reduces the number of chip-to-chip interfaces, thereby reducing power, while increasing performance, reliability and bandwidth. It also

reduces network cost substantially. This presentation will discuss the Blue Gene/Q Compute chip architecture and design, emphasizing the aspects that result in a peak performance increase of 15x versus the previous generation, Blue Gene/P, while achieving a power efficiency increase of 5.6x. The Blue Gene/Q Compute (BQC) chip is a 19 x 19 mm chip in IBM's Cu-45 (45nm SOI) technology. The chip functionally contains 18 processor cores, intended to be used as 16 user cores, 1 core for operating system services, and 1 core as a spare. The processor core is an augmented version of the 4-way multithreaded Power A2 core used on the IBM PowerEN™ chip. Blue Gene/Q-specific modifications include a Quad Floating Point Unit (QPU) with a 4-way SIMD architecture supporting integrated scalar and vector floating-point arithmetic. The QPU can concurrently execute up to 8 floating-point operations (based on a 4-wide FMA instruction), a store instruction and a load instruction. The QPU also provides a set of permute instructions to support efficient vector data reorganization, and instructions for complex number arithmetic that act on adjacent vector element pairs. In addition, each processor core interfaces, via a sophisticated L1-prefetching unit and a crossbar switch, to a 32 MB central L2 cache, which uses embedded DRAM for data storage. The L2 cache allows for the storage of multiple data versions per address. The versioning can be used for advanced cache management techniques such as Speculative Execution (SE) and Transactional Memory (TM). These techniques support aggressive multithreading of applications, as hardware will detect and deal with access conflicts. L2 cache access misses are handled by two integrated memory controllers that interface to DDR3 memory (16GB, directly attached to the BQC chip). The BQC on-chip networking logic supports 10 bidirectional 2GB/s links to neighboring chips, allowing the chips to be interconnected into a high-bandwidth, low-latency 5-D torus network, as well as providing for an additional IO link. The on-chip network logic incorporates routing between these ports, DMA facilities to support remote memory access, and hardware-assist facilities for broadcast and reduction operations. As a result of these architectural features, BQC is a power-efficient compute chip, optimized for a wide range of parallel applications. The Blue Gene/Q systems took over the Green500 top spot since November 2010 three times consecutively, achieving a power efficiency of ~2 GigaFLOPS/Watt. It also received the top honor of Graph500 in November 2011 in a data analytics application.

14:50-16:20 **Break (Poster Open: 7th floor poster show room)**

16:20-18:20 **Session V: Panel Discussions** **9**

Technology exchange: Supercomputing and Embedded computing

Organizer & Moderator: Hideharu Amano (Keio University)

Panelists: Geroge Liang-Tai Chiu (IBM, U.S.A.)

Yuichiro Ajima (Fujitsu)

Wen-mei Hwu (University of Illinois, U.S.A.)

Felipe A. Cruz (Nagasaki University)

Toru Shimizu (Renesas Electronics)

April 20, 2012 *Main Hall(7th Floor), Yokohama Joho Bunka Center*
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9:30-11:10 **Session VI**

9:30-10:20 **Keynote Presentation 3**
Co-chairs: Yoshio Hirose (Fujitsu Labs.), Yasuo Unekawa (Toshiba)

Tofu Interconnect Controller for Fujitsu's Highly Scalable Supercomputer
Yuichiro Ajima (Fujitsu)

Abstract: The K computer, which is the current world's fastest supercomputer, combines 88,128 processor chips using an interconnection network called Tofu Interconnect. Fujitsu's new supercomputer system FX10 is also powered by the Tofu interconnect. We developed an interconnect controller (ICC) chip which integrates all active components of the Tofu interconnect. In this talk, we will present a technical overview of the ICC chip. The ICC chip provides a Tofu network router, four Tofu network interfaces, and a Tofu barrier interface. The Tofu network router provides four internal and ten external ports. Internal ports connect the Tofu network interface for each, and external ports are used to construct a six-dimensional mesh/torus network. The Tofu network interface supports Remote Direct Memory Access (RDMA) communication, and a Tofu barrier interface provides offload capability for synchronization and reduction communication.

10:20-11:10 **Keynote Presentation 4**
Co-chairs: Hiroyuki Takizawa (Tohoku University), Akihiko Hashiguchi (Sony)

Application Scalability and Portability - Key to Low Power, Performance Growth, and Exascale
Wen-mei Hwu (Illinois University, U.S.A.)

Abstract: Parallelism has become the main venue of performance growth and power reduction. Once an application achieves good performance for a given hardware and data set, it must be able to scale effectively in terms of hardware parallelism and data size. Parallelism scalability allows the application to take advantage of a wide range of current and future generation hardware. Data scalability allows the application to handle the ever increasing data size in the real world while managing the ever limiting memory bandwidth. The rise of CPU-GPU heterogeneous computing has significantly boosted the pace of progress in this field. There has been rapid progress in numeric methods, algorithm design, programming techniques, compiler transformations and optimization tools for developing scalable applications. In preparation of petascale applications for deployment on Blue Waters, we have been further accelerating this revolution. In this talk, I will discuss these recent advances, their implications on the future course of computing and computer design.

11:10-11:30 **Break (Poster Open: 7th floor poster show room)**

11:30-12:20 **Session VII: 3D Integration**
Co-chairs: Tetsuya Yamada (Hitachi), Tomochika Harada (Yamagata University)

11:30-11:55 **A 5.184Gbps/ch Through-Chip Interface and Automated Place-and-Route Design Methodology for 3-D Integration of 45nm CMOS Processors** **11**
Yasuhisa Shimazaki[1], Noriyuki Miura[2], Tadahiro Kuroda[2] ([1]Renesas Electronics, [2]Keio University)

11:55-12:20 **Cool System Scalable 3-D stacked Heterogeneous Multi-Core / Multi-Chip Architecture for Ultra Low-Power Digital TV Applications** 14
Yukoh Matsumoto[1], Tomoyuki Morimoto[1], Michiya Hagimoto[1], Hiroyuki Uchida[1], Nobuyuki Hikichi[1], Fumito Imura[2], Hiroshi Nakagawa[2], Masahiro Aoyagi[2] ([1]TOPS Systems, [2]AIST)

12:20-13:50 Lunch Time Break

13:50-14:40 Session VIII
Co-chairs: Kazumasa Suzuki (Renesas Electronics), Hiroyuki Igura (NEC)

13:50-14:40 **Keynote Presentation 5**
Nonvolatile Logic-in-Memory Architecture Using an MTJ/MOS-Hybrid Structure and Its Applications
Takahiro Hanyu (Tohoku University)

Abstract: Communication bottleneck between memory and logic modules has increasingly become a serious problem, which causes large power dissipation in the recent nanometer-scaled VLSI chips. One method to solve such emerging VLSI-chip problems is to use "nonvolatile" logic-in-memory architecture. In this architecture, nonvolatile storage elements are distributed over a logic-circuit plane, so that it is expected to realize both ultra-low-power and reduced interconnection delay because of great reduction of global interconnection counts and volatile storage-element counts. In this presentation, I demonstrate concrete standby power-free logic circuits based on a nonvolatile logic-in-memory structure using magnetic tunnel junction (MTJ) devices in combination with MOS transistors. Since the MTJ device with a spin-injection write capability is only one device that has all the following superior features as large resistance ratio, virtually unlimited endurance, fast read/write accessibility, scalability, CMOS-process compatibility, and no volatility, it is very suited to implement the MOS/MTJ-hybrid logic circuit with logic-in-memory architecture. As typical examples of the proposed nonvolatile logic-in-memory circuitry, an MTJ-based nonvolatile Look-Up Table (LUT) circuit for an instant power-ON/OFF Field Programmable Gate Array and an MTJ-based nonvolatile Ternary Content-Addressable Memory are also demonstrated together with the fabricated test-chip results.

14:40-14:50 Break (Poster Open: 7th floor poster show room)

14:50-16:05 Session IX: Power Gating and Circuit
Co-chairs: Kyoung-Rok Cho (Chungbuk National University), Sugako Otani (Renesas Electronics)

14:50-15:15 **Gate-level Process Variation Offset Technique by using Dual Voltage Supplies to Achieve Near-threshold Energy Efficient Operation** 17
Benjamin Devlin, Makoto Ikeda, Kunihiro Asada (University of Tokyo)

15:15-15:40 **An Area-Efficient, Standard-Cell Based On-Chip NMOS and PMOS Performance Monitor for Process Variability Compensation** 20
Toshiyuki Yamagishi, Tatsuo Shiozawa, Koji Horisaki, Hiroyuki Hara, Yasuo Unekawa (Toshiba)

15:40-16:05 **Trade-off Analysis of Fine-grained Power Gating Methods for Functional Units in a CPU** 23
Weihan Wang[1], Yuya Ohta[2], Yoshifumi Ishii[1], Kimiyoshi Usami[2], Hideharu Amano[1] ([1]Keio University, [2] Shibaura Institute of Technology)

16:05-16:20 **Break**

16:20-17:40 **Session X: Processor**
Co-chairs: Jun Yao (Nara Institute of Science and Technology), Yuetsu Kodama (University of Tsukuba)

16:20-16:45 **A Media-oriented Vector Architectural Extension with a High Bandwidth Cache System** **26**
Ye Gao, Naoki Shoji, Ryusuke Egawa, Hiroyuki Takizawa, Hiroaki Kobayashi (Tohoku University)

16:45-17:10 **Dependable Responsive Multithreaded Processor for Distributed Real-Time Systems** **29**
Kazutoshi Suito, Kei Fujii, Hiroki Matsutani, Nobuyuki Yamasaki (Keio University)

17:10-17:40 **Special Invited Talk**
Seahawk - Optimizing power efficiency in a high performance Cortex-A15 processor implementations
Dermot O'Driscoll, Sumit Sahai (ARM, U.K.)

Abstract: The ARM Cortex™-A15 MPCore™ high performance processor enables compelling SoC designs for a wide range of applications ranging from mobile computing, high-end digital home, servers and wireless infrastructure. SoC designers wishing to exploit the full potential of such high performance processors need considerable implementation expertise and intimate knowledge of new geometries to achieve the optimal balance between performance and power.
Seahawk is a highly optimized implementation of a quad core Cortex-A15 processor on TSMC 28HPM process. The paper describes the various challenges and design choices involved in such designs, and the techniques used by the ARM design team during the implementation of the hard macrocell.

17:40-18:00 **Poster Award and Closing Remark**
Makoto Ikeda, Program Committee Co-chair (University of Tokyo)