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SESSION 1 – TAPA 1 / 2

Plenary Session

Tuesday, June 12, 8:05 a.m.

Chairs: K. Schruefer, Intel Mobile Communications
T. Hiramoto, The University of Tokyo

8:05 a.m. **Welcome, Opening Remarks and Awards**
M-R Lin, GLOBALFOUNDRIES
H. Wakabayashi, Sony Corp.

Session 2 – TAPA 2

Advanced Fin FET Devices and Technology

Tuesday, June 12, 10:25 a.m.

Chairs: G. Yeap, Qualcomm
M. Masahara, Nat'l Institute of AIST

Session 3 – TAPA 2

NAND Flash

Tuesday, June 12, 10:25 a.m.

Chairs: J. Alsmeier, SanDisk
H.-T. Lue, Macronix International Co, Ltd.

3.1 - 10:25 a.m.

A New Metal Control Gate Last Process (MCGL Process) for High Performance DC-SF (Dual Control Gate with Surrounding Floating Gate) 3D NAND Flash Memory, Y. Noh, Y. Ahn, H. Yoo, B. Han, S. Chung, K. Shim, K. Lee, S. Kwak, S.Shin, I. Choi, S. Nam, G. Cho, D. Sheen, S. Pyi, J. Choi, S. Park, J. Kim, S. Lee, S. Aritome, S. Hong, S. Park, Hynix Semiconductor Inc. **19**

3.2 - 10:50 a.m.

Intrinsic Fluctuations in Vertical NAND Flash Memories, E. Nowak, J.-H. Kim, H.Y. Kwon, Y.-G. Kim, J.S. Sim, S.-H. Lim, D.S. Kim, K.-H. Lee, Y.-K. Park, J.-H. Choi, C. Chung, Samsung Electronics Co. Ltd. 21

3.3 - 11:15 a.m.

A New GIDL Phenomenon by Field Effect of Neighboring Cell Transistors and its Control Solutions in Sub-30 nm NAND Flash Devices, I.H. Park, W.-G. Hahn, K.-W. Song, K.H. Choi, H.-K. Choi, S.B. Lee, C.-S. Lee, J.H. Song, J.M. Han, K.H. Kyoung, Y.-H. Jun, Samsung Electronics **23**

3.4 - 11:40 a.m.

Ferroelectricity in HfO_2 Enables Nonvolatile Data Storage in 28 nm HKMG, J. Müller, E. Yurchuk*, T. Schlösser**, J. Paul, R. Hoffmann, S. Müller*, D. Martin*, S. Slesazeck*, P. Polakowski, J. Sundqvist, M. Czernohorsky, K. Seidel, P. Kücher, R. Boschke**, M. Trentzsch**, K. Gebauer**, U. Schröder*, T. Mikolajick*, Fraunhofer Center Nanoelectronic Technologies, *NaMLab GmbH, **GLOBALFOUNDRIES 25

Session 4 – TAPA 1

High-K / Metal Gate Scaling

Tuesday, June 12, 1:30 p.m.

Chairs: T.-J. King Liu, Univ. of California, Berkeley
Y. Akasaka, Tokyo Electron Taiwan, Ltd.

Session 5 – TAPA 2

Alternative Memory

Tuesday, June 12, 1:30 p.m.

Chairs: K. Attenborough, NXP Central R&D
S. Choi, Samsung Electronics Co., Ltd.

Session 6 – TAPA 1

Low Power and Steep Subthreshold Technology

Tuesday, June 12, 3:25 p.m.

Chairs: A. Seabaugh, Notre Dame Univ.
T. Iwamatsu, Renesas Electronics Corp.

Session 7 – TAPA 2
STT MRAM

Tuesday, June 12, 3:25 p.m.
Chairs: E. Kan, Cornell Univ.
S. Hong, Hynix Semiconductor, Inc.

Technology Rump Sessions
Tuesday, June 12, 8:00 p.m. – 10:00 p.m.

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 12
8:00 p.m. – 10:00 p.m.

Organizers:

Circuits	**Technology**
M. Bauer, Micron	T. Skotnicki, STMicroelectronics
N. Lu, Etron	K. Miyashita, Toshiba

RJ1: Scaling Challenges Beyond 1x nm DRAM and NAND Flash

Moderator: R. Shrivastava, SanDisk
N. Lu, Etron

The combined revenues of DRAM and NAND Flash approached $54 Billion in 2010. This is expected to continue to grow in the coming years. Emerging silicon and package technologies will further drive lower cost and new applications. The difficulty of scaling and developing new technologies and investments to build new factories is increasing at about the same rate as the memory bit growth in the world. At the same time, the industry is becoming aware that we are closing in on physical and electrical scaling limitations. As we close in on scaling limits, the use of new materials, manufacturing processes, and circuit design will become unavoidable. To compound the problem, fierce competition is forcing shorter development times. Our industry needs to openly address these issues and challenges in order to continue developing better and lower cost memories for the decade to come. The whole industry faces these challenges and issues. They are huge. We have assembled a representative group of industry experts for this Joint Rump Session. We will ask them to discuss the top issues from the perspective of each one's area of expertise. The floor will be open to question the panelist's view or challenge them to consider issues that audience would like to raise.

Panelists:

S. Aritome, Hynix
G. Atwood, Micron
G. Bronner, Rambus
H. Hazama, Toshiba
H-K Kang, Samsung
M. Koyanagi, Tohoku Univ.
C.Y. Lu, Macronix
K. Takeuchi, University of Tokyo

R2: Evolution of FinFET and beyond?
Moderators: G. Yeap, Qualcomm
Y. Miyamoto, Tokyo Institute of Technology

As conventional scaling approaches its limits, the semiconductor industry has been evaluating for more than a decade on 3D multi-gate FINFET/Tri-gate transistors as well as planar transistors with alternative channel designs (such as FD-SOI, Ge, III-V) for achieving the power efficiency, performance, density, reliability, and form factor required in advanced mobile devices.

It is extremely exciting that in 2012 the industry finally enters into the 3-D era with the high volume production of 3-D Tri-gate/FinFET transistors in 22nm standalone CPU technology. Did 1st generation 3-D tri-gate transistor fully deliver the power/performance value proposition, and achieve the required density/cost and reliability? How well can multi-gate 3D or alternative channel designs overcome scaling bottlenecks, such as parasitic R&C and variability? How fast the 3-D transistor production will spread to other applications especially the driver application of mobile computing SoC? Will 3-D transistor technology completely and utterly dominate the industry or there are rooms for planar architecture be extended or enhanced for a cost/PPA sweat spot for certain applications/markets? How will the 2nd/3rd generation 3-D technology look like? How best the 3-D transistor technology coupled with 2.5/3-D interconnect technology to deliver holistic system scaling for complex, power constrained mobile computing and wireless applications? What is life after FinFET – any Joker left in the pocket?

This panel moderated by Geoffrey Yeap/Y. Miyamoto will start out with a "fire side chat" on the issues from each panelist's perspective, and evolve into a what we hope is a passionate discussion with some serious audience participation. The panelists whose views range across the spectrum include:

F. Boeuf, STMicroelectronics
J.P. Colinge, TSMC
W. Haensch, IBM
D.W. Kim, Samsung
A. Thean, IMEC
S. Thompson, SuVolta

R3: Advanced Patterning for Next Generation Technology Nodes: EUV or Tricky-193nm, EBDW? DSA, Resists, Masks, Regular Layouts, Metrology?

Moderators: G. Vandenberghe, IMEC
M. Tomoyasu, Tokyo Electron

To EUV or not to EUV? That is at least one of the questions that will be tackled by all panelists. In this rump session, the lithography/patterning challenges to enable further scaling will be discussed by multiple experts, involved in the many different fields of lithography as chipmaker, fabless company or equipment manufacturer. What are the ultimate limits of 193nm immersion lithography with multiple patterning schemes? What is the manufacturability readiness of EUV lithography? And how about ebeam direct write? Can directed self assembly be seen as an extension technique? Are only unidirectional layouts allowed and how will the EDA tackle the patterning complexity? What will be the patterning demand from under layer materials and structure direction? How will the metrology enable the lithography challenges?

Y. Borodovsky, Intel
A. Chen, ASML
H. Levinson, GLOBALFOUNDRIES
B. Lin, TSMC
S. Nagahara, TEL
A. Yamaguchi, Hitachi

Session 8 – TAPA 1

RRAM I

Wednesday, June 13**,** 8:05 a.m.

Chairs: J. Zahurak, Micron Technology, Inc.
N. Kasai, Tohoku Univ.

Session 9 – TAPA 2

Process Technology

Wednesday, June 13, 10:25 a.m.

Chairs: C.-P. Chang, Applied Materials
K. Miyashita,Toshiba Corp.

Session 10 – TAPA 3

Technology / Circuits Joint Focus Session – Memory

Wednesday, June 13, 10:25 a.m.
Chairs: J. Zahurak, Micron Technology
M. Hane, Renesas Electronics Corp.

Session 11 – TAPA 2
Mobility Enhancement

Wednesday, June 13, 1:30 p.m.
Chairs: M. Mehrotra, Texas Instruments
S. Takagi, The University of Tokyo

Session 12 – TAPA 3

Technology / Circuits Joint Focus Session – 3D-System Integration

Wednesday, June 13, 1:30 p.m.

Chairs: A. Antonelli,Novellus Systems, Inc.
T. Tanaka, Tohoku Univ.

CIRCUITS SESSION 6 – TAPA I

Technology/Circuits Joint Focus Session - Emerging Nonvolatile Memory

Wednesday, June 13, 3:25 p.m.
Chairpersons: J. DeBrosse, IBM
S. Yamakawa,Sony Corp.

C-6.1 - 3:25 p.m.

A 0.13µm 8Mb Logic Based Cu_xSi_yO Resistive Memory with Self-Adaptive Yield Enhancement and Operation Power Reduction, X.Y. Xue, W.X. Jian, J.G. Yang, F.J. Xiao, G. Chen, X.L. Xu, Y.F. Xie, Y.Y. Lin, R. Huang*, Q.T. Zhou*, J.G. Wu*, Fudan University, *Semiconductor Manufactoring International Corp. N/A

C-6.2 - 3:50 p.m.

A 3.14 um^2 4T-2MTJ-Cell Fully Parallel TCAM Based on Nonvolatile Logic-in-Memory Architecture, S. Matsunaga, S. Miura*, H. Honjou*, K. Kinoshita, S. Ikeda, T. Endoh, H. Ohno, T. Hanyu, Tohoku University, *NEC Corporation N/A

C-6.3 - 4:15 p.m.

1Mb 4T-2MTJ Nonvolatile STT-RAM for Embedded Memories Using 32b Fine-Grained Power Gating Technique with 1.0ns/200ps Wake-up/Power-off Times, T. Ohsawa, H. Koike, S. Miura*, H. Honjo*, K. Tokutome*, S. Ikeda, T. Hanyu, H. Ohno, T. Endoh, Tohoku University, *NEC Coropration N/A

T-6.4 - 4:40 p.m.

A Simple New Write Scheme for Low Latency Operation of Phase Change Memory, Y.-Y. Lin, Y.-C. Chen, F.-M. Lee, M. BrightSky*, H.-L. Lung, C. Lam*, Macronix International Co., Ltd., *IBM T.J. Watson Research Center 51

T-6.5 - 5:05 p.m.

Analysis of Random Telegraph Noise and Low Frequency Noise Properties in 3-D Stacked NAND Flash Memory with Tube-Type Poly-Si Channel Structure, M.-K. Jeong, S.-M. Joe, C.-S. Seo, K.-R. Han*, E. Choi*, S.-K. Park*, J.-H. Lee, Seoul National University, *Hynix Semiconductor Inc. 55

Session 13 – TAPA 2
Ultra-Thin Body Devices

Wednesday, June 13, 3:25 p.m.
Chairs: M. Khare, IBM
C.H. Wann, TSMC

Session 14 – TAPA 3

Novel Passive and Active BEOL Technologies

Wednesday, June 13, 3:25 p.m.
Chairs: R. Klein, AMD
H. Morimura, NTT Microsystem Integration Lab

CIRCUITS SESSION 8 – TAPA I
Technology/Circuit Joint Focus Session - Advanced SRAM

Thursday, June 14, 8:05 a.m.
Chairpersons: G. Lehmann, Infineon Technologies AG
H. Yamauchi, Fukuoka Institute of Technology

C- 8.1 - 8:05 a.m.
A 0.41µA Standby Leakage 32Kb Embedded SRAM with Low-Voltage Resume-Standby Utilizing All Digital Current Comparator in 28nm HKMG CMOS, N. Maeda, S. Komatsu, M. Morimoto, Y. Shimazaki, Renesas Electronics Corp. N/A

C- 8.2 - 8:30 a.m.
A 13.8pJ/Access/Mbit SRAM with Charge Collector Circuits for Effective Use of Non-Selected Bit Line Charges, S. Moriwaki, Y. Yamamoto, A. Kawasumi, T. Suzuki*, S. Miyano, T. Sakurai**, H. Shinohara, Semiconductor Technology Academic Research Center, *Panasonic Corp., **University of Tokyo N/A

C-8.3 - 8:55 a.m.
A SRAM Cell Array with Adaptive Leakage Reduction Scheme for Data Retention in 28nm High-K Metal-Gate CMOS, P. Hsu, Y. Tang, D. Tao, M.-C. Huang, M.-J. Wang, C. Wu, Q. Li, TSMC N/A

C- 8.4 - 9:20 a.m.
A 28nm High-k Metal-Gate SRAM with Asynchronous Cross-Couple Read Assist (AC2RA) Circuitry Achieving 3X Reduction on Speed Variation for Single Ended Arrays, R. Lee, J.-P. Yang, C.-E. Huang, C.-C. Chiu, W.-S. Kao, H.-C. Cheng, H.-J. Liao, J. Chang, TSMC N/A

Session 15 – TAPA 2
CMOS Platform

Thursday, June 14, 8:05 a.m.
Chairs: W. Maszara, Globalfoundries
S. Inaba, Toshiba Corp.

15.1 - 8:05 a.m.

High Performance Bulk Planar 20nm CMOS Technology for Low Power Mobile Applications, H. Shang, S. Jain, E. Josse*, E. Alptekin, M.H. Nam**, S.W. Kim^, K.H. Cho^, I. Kim^, Y. Liu**, X. Yang**, X. Wu**, J. Ciavatti**, N.S. Kim**, R. Vega, L. Kang**, H.V. Meer**, S. Samavedam**, M. Celik*, S. Soss**, H. Utomo, R. Ramachandran, W. Lai, V. Sardesai, C. Tran, J.Y. Kim^, Y.H. Park^, W.L. Tan**, T. Shimizu^^, R. Joy**, J. Strane, K. Tabakman, F. Lalanne*, P. Montanini*, K. Babich**, J.B. Kim^, L. Economikos, W. Cote, C. Reddy**, M. Belyansky, R. Arndt, U. Kwon, K. Wong, D. Koli**, D. Leveakis, J.W. Lee^, J. Muncy, S. Krishnan, D. Schepis, X. Chen, B.D. Kim^, C. Tian, B.P. Linder, E. Cartier, V. Narayanan, G. Northrop, O. Menut*, J. Meiring, A. Tomas, M. Aminpur, S.H. Park^, K.Y. Weybright, R. Mann**, A. Mittal**, M. Eller#, S. Lian^, R. Divakaruni, S. Bukofsky, J.D. Kim^, J. Sudijono**, W. Neumueller#, F. Matsuoka^^, R. Sampson*, IBM Microelectronics, *STMicroelectronics, **GLOBALFOUNDRIES, ^Samsung Electronics, ^^Toshiba Corporation, #IMC GmbH 129

15.2 - 8:30 a.m.

A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors, C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyun, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roester, J. Sanford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, G. Weber, P. Yashar, K. Zawadzki, K. Mistry, Intel Corp. 131

15.3 - 8:55 a.m.

28nm FDSOI Technology Platform for High-Speed Low-Voltage Digital Applications, N. Planes, O.Weber*, V. Barral*, S. Haendler, D. Noblet, D. Croain, M. Bocat, P.-O. Sassoulas, X. Federspiel, A. Cros, A. Bajolet, E. Richard, B. Dumont, P. Perreau*, D. Petit, D. Golanski, C. Fenouillet-Beranger*, N. Guillot, M. Rafik, V. Huard, S. Puget, X. Montagner, M.-A. Jaud*, O. Rozeau*, O. Saxod, F. Wacquant, F. Monsier, D. Barge, L. Pinzelli, M. Mellier, F. Boeuf, F. Arnaud, M. Haond, STMicroelectronics, *CEA-LETI, MINATEC 133

15.4 - 9:20 a.m.

Advanced Modeling and Optimization of High Performance 32nm HKMG SOI CMOS for RF/Analog SoC Applications, S. Lee, J. Johnson, B. Greene, A. Chou, K. Zhao, M. Chowdhury, J. Sim, A. Kumar, D. Kim, A. Sutton, S.H. Ku, Y. Liang, Y. Wang, D. Slisher, K. Duncan, P. Hyde, R. Thoma, J. Deng, Y. Deng, R. Rupani, R. Williams, L. Wagner, C. Wermer, H. Li, B. Johnson, D. Daley, J.O. Plouchart, S. Narasimha, C. Putnam, E. Maciejewski, W. Henson, S. Springer, IBM Semiconductor Research and Development Center 135

Session 16 – TAPA 3
Noise Phenomena

Thursday, June 14, 8:05 a.m.
Chairs: C. Mazure, SOITEC Group
S.S. Chung, Nat'l Chiao Tung Univ.

Session 17 – TAPA 2

Technology / Circuits Joint Focus Session – Design in Scaled Technologies

Thursday, June 14, 10:00 a.m.
Chairs: J. Cheek, Freescale
R. Takemura, Hitachi, Ltd.

Session 18 – TAPA 3

RRAM II

Thursday, June 14, 10:00 a.m.
Chairs: G. Jurczak, IMEC
Y. Nakao, Rohm Co., Ltd.

CIRCUITS SESSION 12 – Tapa 1
Technology/Circuits Joint Focus Session - Design Enablement in Scaled CMOS

Thursday, June 14, 1:30 p.m.
Chairpersons: K. Wilcox, AMD
K. Nose, Renesas Electronics Corp.

C-12.1 - 1:30 p.m.
A 22nm Dynamically Adaptive Clock Distribution for Voltage Droop Tolerance, K. Bowman, C. Tokunaga, T. Karnik, V. De, J. Tschanz, Intel N/A

C-12.2 - 1:55 p.m.
Voltage Droop Reduction Using Throttling Controlled by Timing Margin Feedback, M. Floyd, A. Drake*, R. Berry, H. Chase, R. Willaman, J. Pena, IBM System and Technology Group, *IBM Austin Research Lab N/A

C-12.3 - 2:20 p.m.
An On-Die All-Digital Delay Measurement Circuit with 250fs Accuracy, M. Mansuri, B. Casper, F. O'Mahony, Intel Corporation N/A

C-12.4 - 2:45 p.m.
A 47% Access Time Reduction with a Worst-Case Timing-Generation Scheme Utilizing a Statistical Method for Ultra Low Voltage SRAMs, A. Kawasumi, Y. Takeyama, O. Hirabayashi, K. Kushida, F. Tachibana, Y. Niki, S. Sasaki, T. Yabe, Toshiba **N/A**

Session 19 – TAPA 2

High Mobility – Ge Devices

Thursday, June 14, 1:30 p.m.

Chairs: T. Ernst, CEA-LETI, MINATEC
T. Tanaka, Fujitsu Semiconductor

Session 20 - TAPA 3

3D Integration Technology

Thursday, June 14, 1:30 p.m.

Chairs: A. Antonelli, Novellus Systems, Inc.
T. Tanaka, Tohoku Univ.

CIRCUITS SESSION 14 – TAPA II
Technology/Circuits Focus Session - Embedded Memory

Thursday, June 14, 3:25 p.m.
Chairpersons: L. Cheng, Oracle
M. Yamaoka, Hitachi America, Ltd.

C- 14.1 - 3:25 p.m.
Isolated Preset Architecture for a 32nm SOI embedded DRAM Macro, J. Barth, D. Plass, A. Vehabovic, R. Joshi*, R. Kanj*, S. Burns, T. Weaver, IBM Systems and Technology Group, *IBM Research N/A

C-14.2 - 3:50 p.m.
A 260mV L-shaped 7T SRAM with Bit-Line (BL) Swing Expansion Schemes Based on Boosted BL, Asymmetric-V_{TH} Read-Port, and Offset Cell VDD Biasing Techniques, M.-P. Chen, L.-F. Chen, M.-F. Chang, S.-M. Yang, Y.-J. Kuo, J.-J. Wu, M.-S. Ho**, H.-Y. Su*, Y.-H. Chu*, W.-C. Wu*, T.-Y. Yang*, H. Yamauchi^, National Tsing Hua University, *ICL, ITRI, **National Chung Hsing University, ^Fukuoka Institute of Technology N/A

C- 14.3 - 4:15 p.m.
A 1.6-mm2 38-mW 1.5-Gb/s LDPC Decoder Enabled by Refresh-Free Embedded DRAM, Y.S. Park, D. Blaauw, D. Sylvester, Z. Zhang, University of Michigan N/A

C-14.4 - 4:40 p.m.
1Gsearch/sec Ternary Content Addressable Memory Compiler with Silicon-Aware Early-Predict Late-Correct Single-Ended Sensing, I. Arsovski, T. Hebig, D. Dobson, R. Wistort, IBM Systems Technology Group N/A

C- 14.5 - 5:05 p.m.
A 2.8GHz 128-entry x 152b 3-Read/2-Write Multi-Precision Floating-Point Register File and Shuffler in 32nm CMOS, S. Hsu, A. Agarwal, M. Anders, H. Kaul, S. Mathew, F. Sheikh, R. Krishnamurthy, S. Borkar, Intel Corporation N/A

Session 21 – TAPA 2

Scaled III-V Transistors and Modeling

Thursday, June 14, 3:25 p.m.

Chairs: J. Kavalieros, Intel Corp.
B.H. Lee, Gwangju Institute of Sci. and Tech.

Session 22 – TAPA 3

Variability Characterization and Modeling

Thursday, June 14, 3:25 p.m.

Chairs: T. Skotnicki, STMicroelectronics
N. Sugii, Hitachi, Ltd.