

2012 Symposium on VLSI Technology

(VLSIT 2012)

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12 – 14 June 2012**



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SESSION 1 – TAPA 1 / 2
Plenary Session

Tuesday, June 12, 8:05 a.m.

Chairs: K. Schruefer, Intel Mobile Communications
T. Hiramoto, The University of Tokyo

8:05 a.m. Welcome, Opening Remarks and Awards
M-R Lin, GLOBALFOUNDRIES
H. Wakabayashi, Sony Corp.

1.1 – 8:40 a.m.

Peering through the Technology Scaling Fog (Invited), M. Mayberry, Intel 1

1.2 – 9:25 a.m.

Wearable Sensing Systems for Healthcare Monitoring (Invited), I. Yamada, G. Lopez, University of Tokyo 5

Session 2 – TAPA 2
Advanced Fin FET Devices and Technology

Tuesday, June 12, 10:25 a.m.

Chairs: G. Yeap, Qualcomm
M. Masahara, Nat'l Institute of AIST

2.1 - 10:25 a.m.

10nm-Diameter Tri-Gate Silicon Nanowire MOSFETs with Enhanced High-Field Transport and V_{th} Tunability through Thin BOX, M. Saitoh, K. Ota, C. Tanaka, K. Uchida*, T. Numata, Toshiba Corp., *Tokyo Institute of Technology 11

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2.3 - 11:15a.m.

Channel Doping Impact on FinFETs for 22nm and Beyond, C.-H. Lin, R. Kambhampati*, R. Miller*, T. Hook, A. Bryant, W. Haensch, P. Oldiges, I. Lauer, T. Yamashita, V. Basker, T. Standaert, K. Rim, E. Leobandung, H. Bu, M. Khare, IBM Research Division, *GLOBALFOUNDRIES 15

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FinFET Parasitic Resistance Reduction by Segregating Shallow Sb, Ge and As Implants at the Silicide Interface, C. Kenney, K.-W. Ang, K. Matthews, M. Liehr, M. Minakais, M. Rodgers*, V. Kaushik*, S. Novak*, S. Gausepohl*, C. Hobbs, P. Kirsch, R. Jammy, J. Pater, SEMATECH, *CNSE State University of New York 17

Session 3 – TAPA 2
NAND Flash

Tuesday, June 12, 10:25 a.m.

Chairs: J. Alsmeier, SanDisk
H.-T. Lue, Macronix International Co, Ltd.

3.1 - 10:25 a.m.

A New Metal Control Gate Last Process (MCGL Process) for High Performance DC-SF (Dual Control Gate with Surrounding Floating Gate) 3D NAND Flash Memory, Y. Noh, Y. Ahn, H. Yoo, B. Han, S. Chung, K. Shim, K. Lee, S. Kwak, S. Shin, I. Choi, S. Nam, G. Cho, D. Sheen, S. Pyi, J. Choi, S. Park, J. Kim, S. Lee, S. Aritome, S. Hong, S. Park, Hynix Semiconductor Inc.

3.2 - 10:50 a.m.

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3.3 - 11:15 a.m.

A New GIDL Phenomenon by Field Effect of Neighboring Cell Transistors and its Control Solutions in Sub-30 nm NAND Flash Devices, I.H. Park, W.-G. Hahn, K.-W. Song, K.H. Choi, H.-K. Choi, S.B. Lee, C.-S. Lee, J.H. Song, J.M. Han, K.H. Kyoung, Y.-H. Jun, Samsung Electronics 23

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Session 4 – TAPA 1
High-K / Metal Gate Scaling

Tuesday, June 12, 1:30 p.m.

Chairs: T.-J. King Liu, Univ. of California, Berkeley
Y. Akasaka, Tokyo Electron Taiwan, Ltd.

4.1 - 1:30 p.m.

Implementing Cubic-Phase HfO₂ with K-Value ~ 30 in Low-V_T Replacement Gate pMOS Devices for Improved EOT- Scaling and Reliability, L.-Å. Ragnarsson, C. Adelman, Y. Higuchi, K. Opsomer, A. Veloso, S.A. Chew, E. Röhr, E. Vecchio, X. Shi, K. Devriendt, F. Sebaai, T. Kauerauf, M. Pawlak, T. Schram, S. Van Elshocht, N. Horiguchi, A. Thean, Imec 27

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Chairs: K. Attenborough, NXP Central R&D
S. Choi, Samsung Electronics Co., Ltd.

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Scalable 3-D Vertical Chain-Cell-Type Phase-Change Memory with 4F² Poly-Si Diodes, M. Kinoshita, Y. Sasago, H. Minemura, Y. Anzai, M. Tai, Y. Fujisaki, S. Kusaba, T. Morimoto, T. Takahama, T. Mine, A. Shima, Y. Yonamoto, T. Kobayashi, Hitachi, Ltd. 35

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Tuesday, June 12, 3:25 p.m.

Chairs: A. Seabaugh, Notre Dame Univ.
T. Iwamatsu, Renesas Electronics Corp.

6.1 – 3:25 p.m.

Recent Progress and Challenges for Relay Logic Switch Technology (Invited), T.-J. King Liu, L. Hutin, I-R. Chen, R. Nathanael, Y. Chen, E. Alon, University of California, Berkeley 43

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6.5 - 5:05 p.m.

Demonstration of Improved Heteroepitaxy, Scaled Gate Stack and Reduced Interface States Enabling Heterojunction Tunnel FETs with High Drive Current and High On-Off Ratio, D. Mohata, B. Rajamohanan, Y. Zhu*, M. Hudait*, R. Southwick*, Z. Chbili**, D. Gundlach**, J. Suehle**, J. Fastenau^, D. Loubychev^, A. Liu^, T. Mayer, V. Narayanan, S. Datta, The Pennsylvania State University, *Virginia Tech, **NIST, ^IQE Inc. 53

Session 7 – TAPA 2
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Tuesday, June 12, 3:25 p.m.

Chairs: E. Kan, Cornell Univ.
S. Hong, Hynix Semiconductor, Inc.

7.1 - 3:25 p.m.

Enhancement of Data Retention and Write Current Scaling for Sub-20nm STT-MRAM by Utilizing Dual Interfaces for Perpendicular Magnetic Anisotropy, J.-H. Park, Y. Kim, W. Lim, J. Kim, S. Park, J. Kim, W. Kim, K. Kim, J. Jeong, K.S. Kim, H. Kim, Y.J. Lee, S. Oh, J.E. Lee, S.O. Park, S. Watts*, D. Apalkov*, V. Nikitin*, M. Krounbi*, S. Jeong, S. Choi, H. Kang, C. Chung, Samsung Electronics Co., Ltd., *Grandis Inc. 57

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Demonstration of Non-Volatile Working Memory Through Interface Engineering in STT-MRAM, C. Yoshida, T. Ochiai, Y. Iba, Y. Yamazaki, K. Tsunoda, A. Takahashi, T. Sugii, LEAP 59

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7.4 - 4:40 p.m.

Spintronics Primitive Gate with High Error Correction Efficiency $6 (P_{\text{error}})^2$ for Logic-in Memory Architecture, Y. Tsuji, R. Nebashi, N. Sakimura, A. Morioka, H. Honjo, K. Tokutome, S. Miura, T. Suzuki*, S. Fukami*, K. Kinoshita[^], T. Hanyu[^], T. Endo[^], N. Kasai[^], H. Ohno[^], T. Sugibayashi, NEC Corp., *Renesas Electronics Corp., [^]Tohoku University 63

7.5 - 5:05 p.m.

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Technology Rump Sessions
Tuesday, June 12, 8:00 p.m. – 10:00 p.m.

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 12
8:00 p.m. – 10:00 p.m.

Organizers:

Circuits

M. Bauer, Micron
N. Lu, Etron

Technology

T. Skotnicki, STMicroelectronics
K. Miyashita, Toshiba

RJ1: Scaling Challenges Beyond 1x nm DRAM and NAND Flash

Moderator: R. Shrivastava, SanDisk
N. Lu, Etron

The combined revenues of DRAM and NAND Flash approached \$54 Billion in 2010. This is expected to continue to grow in the coming years. Emerging silicon and package technologies will further drive lower cost and new applications. The difficulty of scaling and developing new technologies and investments to build new factories is increasing at about the same rate as the memory bit growth in the world. At the same time, the industry is becoming aware that we are closing in on physical and electrical scaling limitations. As we close in on scaling limits, the use of new materials, manufacturing processes, and circuit design will become unavoidable. To compound the problem, fierce competition is forcing shorter development times. Our industry needs to openly address these issues and challenges in order to continue developing better and lower cost memories for the decade to come. The whole industry faces these challenges and issues. They are huge. We have assembled a representative group of industry experts for this Joint Rump Session. We will ask them to discuss the top issues from the perspective of each one's area of expertise. The floor will be open to question the panelist's view or challenge them to consider issues that audience would like to raise.

Panelists:

S. Aritome, Hynix
G. Atwood, Micron
G. Bronner, Rambus
H. Hazama, Toshiba

H-K Kang, Samsung
M. Koyanagi, Tohoku Univ.
C.Y. Lu, Macronix
K. Takeuchi, University of Tokyo

R2: Evolution of FinFET and beyond?

Moderators: G. Yeap, Qualcomm
Y. Miyamoto, Tokyo Institute of Technology

As conventional scaling approaches its limits, the semiconductor industry has been evaluating for more than a decade on 3D multi-gate FINFET/Tri-gate transistors as well as planar transistors with alternative channel designs (such as FD-SOI, Ge, III-V) for achieving the power efficiency, performance, density, reliability, and form factor required in advanced mobile devices.

It is extremely exciting that in 2012 the industry finally enters into the 3-D era with the high volume production of 3-D Tri-gate/FinFET transistors in 22nm standalone CPU technology. Did 1st generation 3-D tri-gate transistor fully deliver the power/performance value proposition, and achieve the required density/cost and reliability? How well can multi-gate 3D or alternative channel designs overcome scaling bottlenecks, such as parasitic R&C and variability? How fast the 3-D transistor production will spread to other applications especially the driver application of mobile computing SoC? Will 3-D transistor technology completely and utterly dominate the industry or there are rooms for planar architecture be extended or enhanced for a cost/PPA sweet spot for certain applications/markets? How will the 2nd/3rd generation 3-D technology look like? How best the 3-D transistor technology coupled with 2.5/3-D interconnect technology to deliver holistic system scaling for complex, power constrained mobile computing and wireless applications? What is life after FinFET – any Joker left in the pocket?

This panel moderated by Geoffrey Yeap/Y. Miyamoto will start out with a "fire side chat" on the issues from each panelist's perspective, and evolve into a what we hope is a passionate discussion with some serious audience participation. The panelists whose views range across the spectrum include:

F. Boeuf, STMicroelectronics
J.P. Colinge, TSMC
W. Haensch, IBM

D.W. Kim, Samsung
A. Thean, IMEC
S. Thompson, SuVolta

R3: Advanced Patterning for Next Generation Technology Nodes: EUV or Tricky-193nm, EBDW? DSA, Resists, Masks, Regular Layouts, Metrology?

Moderators: G. Vandenberghe, IMEC
M. Tomoyasu, Tokyo Electron

To EUV or not to EUV? That is at least one of the questions that will be tackled by all panelists. In this rump session, the lithography/patterning challenges to enable further scaling will be discussed by multiple experts, involved in the many different fields of lithography as chipmaker, fabless company or equipment manufacturer. What are the ultimate limits of 193nm immersion lithography with multiple patterning schemes? What is the manufacturability readiness of EUV lithography? And how about ebeam direct write? Can directed self assembly be seen as an extension technique? Are only unidirectional layouts allowed and how will the EDA tackle the patterning complexity? What will be the patterning demand from under layer materials and structure direction? How will the metrology enable the lithography challenges?

Y. Borodovsky, Intel
A. Chen, ASML
H. Levinson, GLOBALFOUNDRIES
B. Lin, TSMC
S. Nagahara, TEL
A. Yamaguchi, Hitachi

Session 8 – TAPA 1
RRAM I

Wednesday, June 13, 8:05 a.m.

Chairs: J. Zahurak, Micron Technology, Inc.
N. Kasai, Tohoku Univ.

8.1 - 8:05 a.m.

A Novel Cross Point One-Resistor (0T1R) Conductive Bridge Random Access Memory (CBRAM) with Ultra Low Set/Reset Operation Current, F.M. Lee, Y.Y. Lin, M.H. Lee, W.C. Chien, H.L. Lung, K.Y. Hsieh, C.Y. Lu, Macronix International Co., Ltd. 67

8.2 - 8:30 a.m.

Field-Driven Ultrafast sub-ns Programming in W\Al₂O₃\Ti\CuTe-Based 1T1R CBRAM System, L. Goux, K. Sankaran, G. Kar, N. Jossart, K. Opsomer, R. Degraeve, G. Pourtois, G.-M. Rignanese*, C. Detavernier**, S. Clima, Y.-Y. Chen, A. Fantini, B. Govoreanu, D.J. Wouters, M. Jurczak, L. Altimime, J. Kittl, imec, *UCL and ETSF, **University of Gent 69

8.3 - 8:55 a.m.

Multi-level Switching of Triple-layered TaOx RRAM with Excellent Reliability for Storage Class Memory, S.R. Lee, Y.-B. Kim, M. Chang, K.M. Kim, C.B. Lee, J.H. Hur, G.-S. Park, D. Lee, M.-J. Lee, C.J. Kim, U.-I. Chung, I.-K. Yoo, K. Kim, Samsung Advanced Institute of Technology 71

8.4 - 9:20 a.m.

Conductive Filament Scaling of TaOx Bipolar ReRAM for Long Retention with Low Current Operation, T. Ninomiya, T. Takagi, Z. Wei, S. Muraoka, R. Yasuhara, K. Katayama, Y. Ikeda, K. Kawai, Y. Kato, Y. Kawashima, S. Ito, T. Mikawa, K. Shimakawa, K. Aono, Panasonic Corporation 73

8.5 - 9:45 a.m.

Dynamic 'Hour Glass' Model for SET and RESET in HfO₂ RRAM, R. Degraeve, A. Fantini, S. Clima, B. Govoreanu, L. Goux, Y.Y. Chen, D. Wouters, P. Roussel, G.S. Kar, G. Pourtois, S. Cosemans, J. Kittle, G. Groeseneken, M. Jurczak, L. Altimime, IMEC 75

Session 9 – TAPA 2
Process Technology

Wednesday, June 13, 10:25 a.m.

Chairs: C.-P. Chang, Applied Materials
K. Miyashita, Toshiba Corp.

9.1 - 10:25 a.m.

Atom Probe Tomography for 3D-Dopant Analysis in FinFET Devices, A.K. Kambham, G. Zschaetzsch, Y. Sasaki, M. Togo, 77
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Belfast

9.2 - 10:50 a.m.

A 32nm High-K and Metal-Gate Anti-Fuse Array Featuring a 1.01 μm^2 1T1C Bit Cell, S. Kulkarni, S. Pae, Z. Chen, W. 79
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9.3 - 11:15 a.m.

Replacement Metal Gate Extendible to 11 nm Technology, N. Yoshida, X. Fu, K. Xu, Y. Lei, H. Yang, S. Sun, H. Chen, A. 81
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9.4 - 11:40 a.m.

ZnO: An Attractive Option for n-Type Metal-Interfacial Layer-Semiconductor (Si, Ge, SiC) Contacts, P. Paramahans 83
Manik, S. Gupta*, R. Mishra, N. Agarwal, A. Nainani*, Y.-C. Huang*, M. Abraham*, S. Kapadia, U. Ganguly, S. Lodha,
Indian Institute of Technology Bombay, *Applied Materials Inc.

Session 10 – TAPA 3
Technology / Circuits Joint Focus Session – Memory

Wednesday, June 13, 10:25 a.m.

Chairs: J. Zahurak, Micron Technology
M. Hane, Renesas Electronics Corp.

10.1 – 10:25 a.m.

SRAMs Design in Nano-Scale CMOS Technologies (Invited), K. Zhang, Intel Corp. 85

10.2 – 10:50 a.m.

Hybrid Memory Cube New DRAM Architecture Increases Density and Performance (Invited), J. Jeddeloh, B. Keeth, 87
Micron

10.3 – 11:15 a.m.

Restructuring of Memory Hierarchy in Computing System with Spintronics-Based Technologies (Invited), T. Endoh, T. 89
Ohsawa, H. Koike, T. Hanyu, H. Ohno, Tohoku University

10.4 - 11:40 a.m.

**A Highly Pitch Scalable 3D Vertical Gate (VG) NAND Flash Decoded by a Novel Self-Aligned Independently Controlled 91
Double Gate (IDG) String Select Transistor (SSL)**, C.-P. Chen, H.-T. Lue, K.-P. Chang, Y.-H. Hsiao, C.-C. Hsieh, S.-H. Chen,
Y.-H. Shih, K.-Y. Hsieh, T. Yang, K.-C. Chen, C.-Y. Lu, Macronix International., Ltd.

Session 11 – TAPA 2
Mobility Enhancement

Wednesday, June 13, 1:30 p.m.

Chairs: M. Mehrotra, Texas Instruments
S. Takagi, The University of Tokyo

11.1 - 1:30pm

A New Liner Stressor (GeTe) Featuring Stress Enhancement due to Very Large Phase-Change Induced Volume Contraction for p-Channel FinFETs, R. Cheng, Y. Ding, S.M. Koh, A. Gyanathan, F. Bai, B. Liu, Y.-C. Yeo, National University of Singapore 93

11.2 - 1:55pm

GeSn Channel nMOSFETs: Material Potential and Technological Outlook, S. Gupta, B. Vincent*, D. Lin*, M. Gunji, A. Firrincieli*, F. Gencarelli*, B. Magyari-Köpe, B. Yang**, B. Douhard*, J. Delmotte*, A. Franquet*, M. Caymax*, J. Dekoster*, Y. Nishi, K. Saraswat, Stanford University, *IMEC, **GLOBALFOUNDRIES 95

11.3 - 2:20pm

Strained Germanium-Tin (GeSn) N-Channel MOSFETs Featuring Low Temperature N⁺/P Junction Formation and GeSnO₂ Interfacial Layer, G. Han, S. Su*, L. Wang, W. Wang, X. Gong, Y. Yang, Ivana, P. Guo, C. Guo, G. Zhang*, J. Pan**, Z. Zhang**, C. Xue*, B. Cheng*, Y.-C. Yeo, National University of Singapore, *Chinese Academy of Sciences, **A*STAR 97

11.4 - 2:45pm

Towards High Performance Ge_{1-x}Sn_x and In_{0.7}Ga_{0.3}As CMOS: A Novel Common Gate Stack Featuring Sub-400 °C Si₂H₆ Passivation, Single TaN Metal Gate, and Sub-1.3 nm EOT, X. Gong, S. Su*, B. Liu, L. Wang, W. Wang, Y. Yang, E. Kong, B. Cheng*, G. Han, Y.C. Yeo, National University of Singapore, *Chinese Academy of Sciences 99

Session 12 – TAPA 3
Technology / Circuits Joint Focus Session – 3D-System Integration

Wednesday, June 13, 1:30 p.m.

Chairs: A. Antonelli, Novellus Systems, Inc.
T. Tanaka, Tohoku Univ.

12.1 – 1:30 p.m.

Practical Implications of Via-Middle Cu TSV-induced Stress in a 28nm CMOS Technology for Wide-IO Logic-Memory Interconnect (Invited), J. West, Y.S. Choio, C. Vartuli, Texas Instruments 101

12.2 – 1:55 p.m.

Thermal Stress Characteristics and Impact on Device Keep-Out Zone for 3-D ICs Containing Through-Silicon-Vias (Invited), T. Jiang, S-K Ryu, Q. Zhao, J. Im, H-Y Son, K-Y Byun, R. Huang, P.S. Ho, University of Texas, Austin and Hynix 103

12.3 – 2:20 p.m.

Near-Field Wireless Connection for 3D-System Integration (Invited), T. Kuroda, Keio University 105

12-4 - 2:45 p.m.

An Ultra-Thin Interposer Utilizing 3D TSV Technology, W.-C. Chiou, K.-F. Yang, C. Yeh, S.-H. Wang, Y.-H. Liou, T.-J. Wu, J.-C. Lin, C.-C. Hsieh, H.A. Teng, C.C. Chiu, D.C. Yeh, W.C. Wu, A.J. Su, S.L. Chiu, H.-P. Chang, J. Wei, Y.-C. Lin, Y.-H. Chen, H.-J. Tu, H.D. Ko, T.-H. Yu, J.P. Hung, P.-H. Tsai, C.L. Huang, S.W. Lu, S.Y. Hou, D.-Y. Shih, K.H. Chen, S.-P. Jeng, C.-H. Yu, TSMC 107

CIRCUITS SESSION 6 – TAPA I
Technology/Circuits Joint Focus Session - Emerging Nonvolatile Memory

Wednesday, June 13, 3:25 p.m.

Chairpersons: J. DeBrosse, IBM
S. Yamakawa, Sony Corp.

C-6.1 - 3:25 p.m.

A 0.13 μ m 8Mb Logic Based Cu_xSi_yO Resistive Memory with Self-Adaptive Yield Enhancement and Operation Power Reduction, X.Y. Xue, W.X. Jian, J.G. Yang, F.J. Xiao, G. Chen, X.L. Xu, Y.F. Xie, Y.Y. Lin, R. Huang*, Q.T. Zhou*, J.G. Wu*, Fudan University, *Semiconductor Manufacturing International Corp. **N/A**

C-6.2 - 3:50 p.m.

A 3.14 μ m² 4T-2MTJ-Cell Fully Parallel TCAM Based on Nonvolatile Logic-in-Memory Architecture, S. Matsunaga, S. Miura*, H. Honjou*, K. Kinoshita, S. Ikeda, T. Endoh, H. Ohno, T. Hanyu, Tohoku University, *NEC Corporation **N/A**

C-6.3 - 4:15 p.m.

1Mb 4T-2MTJ Nonvolatile STT-RAM for Embedded Memories Using 32b Fine-Grained Power Gating Technique with 1.0ns/200ps Wake-up/Power-off Times, T. Ohsawa, H. Koike, S. Miura*, H. Honjo*, K. Tokutome*, S. Ikeda, T. Hanyu, H. Ohno, T. Endoh, Tohoku University, *NEC Corporation **N/A**

T-6.4 - 4:40 p.m.

A Simple New Write Scheme for Low Latency Operation of Phase Change Memory, Y.-Y. Lin, Y.-C. Chen, F.-M. Lee, M. BrightSky*, H.-L. Lung, C. Lam*, Macronix International Co., Ltd., *IBM T.J. Watson Research Center **51**

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Analysis of Random Telegraph Noise and Low Frequency Noise Properties in 3-D Stacked NAND Flash Memory with Tube-Type Poly-Si Channel Structure, M.-K. Jeong, S.-M. Joe, C.-S. Seo, K.-R. Han*, E. Choi*, S.-K. Park*, J.-H. Lee, Seoul National University, *Hynix Semiconductor Inc. **55**

Session 13 – TAPA 2
Ultra-Thin Body Devices

Wednesday, June 13, 3:25 p.m.

Chairs: M. Khare, IBM
C.H. Wann, TSMC

13.1 - 3:25 p.m.

Poly/High-k/SiON Gate Stack and Novel Profile Engineering Dedicated for Ultralow-Voltage Silicon-on-Thin-BOX (SOTB) CMOS Operation, Y. Yamamoto, H. Makiyama, T. Tsunomura, T. Iwamatsu, H. Oda, N. Sugii, Y. Yamaguchi, T. Mizutani*, T. Hiramoto, LEAP, *University of Tokyo 109

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Efficiency of Mechanical Stressors in Planar FDSOI n and p MOSFETs Down to 14nm Gate Length, S. Morvan, F. Andrieu, M. Cassé, O. Weber, N. Xu, P. Perreau, J.-M. Hartmann, J.-C. Barbé, J. Mazurier, P. Nguyen*, C. Fenouillet-Bérangée, C. Tabone, L. Tosti, L. Brévard, A. Toffoli, F. Allain, D. Lafond, B.-Y. Nguyen*, G. Ghibaudo[^], F. Boeuf**, O. Faynot, T. Poiroux, CEA, LETI, MINATEC, *SOITEC, **STMicroelectronics, [^]IMEP-LAHC/MINATEC 111

13.3 - 4:15 p.m.

Impact of Back Biasing on Carrier Transport in Ultra-Thin-Body and BOX (UTBB) Fully Depleted SOI MOSFETs, N. Xu, F. Andrieu*, B. Ho, B.-Y. Nguyen*, O. Weber*, C. Mazure*, O. Faynot*, T. Poiroux*, T.-J. King Liu, University of California, Berkeley, *CEA-LETI, Minatec, **SOITEC 113

13.4 - 4:40 p.m.

Enhancement of Devices Performance of hybrid FDSOI/Bulk Technology by using UTBOX sSOI substrates, C. Fenouillet-Beranger, P. Perreau, O. Weber, I. Ben-Akkez*, A. Cros*, A. Bajolet*, S. Haendler*, P. Fonteneau*, P. Gouraud*, E. Richard*, F. Abbate*, D. Barge*, D. Pellissier-Tanon*, B. Dumont*, F. Andrieu, J. Passieux*, R. Bon*, V. Barral, D. Golanski*, D. Petit*, N. Planes*, O. Bonin**, W. Schwarzenbach**, T. Poiroux, O. Faynot, M. Haond*, F. Boeuf*, CEA-LETI, MINATEC, *STMicroelectronics, **SOITEC 115

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Strain Engineered Extremely Thin SOI (ETSOI) for High-Performance CMOS, A. Khakifirooz, K. Cheng, T. Nagumo*, N. Loubet**, T. Adam, A. Reznicek, J. Kuss, D. Shahrjerdi, R. Sreenivasan, S. Ponothe, H. He, P. Kulkarni, Q. Liu**, P. Hashemi[#], P. Khare**, S. Luning[^], S. Mehta, J. Gimbert**, Y. Zhu[#], Z. Zhu^{##}, J. Li, A. Madan^{##}, T. Levin, F. Monsieur**, T. Yamamoto*, S. Naczas, S. Schmitz, S. Holmes, C. Aulnette[^], N. Daval[^], W. Schwarzenbach[^], B.-Y. Nguyen[^], V. Parachuri, M. Khare, G. Shahidi[#], B. Doris, IBM Research, *Renesas, **STMicroelectronics, [^]GLOBALFOUNDRIES, ^{^^}SOITEC, [#]IBM TJ Watson Research Center, ^{##}IBM SRDC 117

Session 14 – TAPA 3
Novel Passive and Active BEOL Technologies

Wednesday, June 13, 3:25 p.m.

Chairs: R. Klein, AMD
H. Morimura, NTT Microsystem Integration Lab

14.1 - 3:25 p.m.

A Novel Chemically, Thermally and Electrically Robust Cu Interconnect Structure with an Organic Non-porous Ultralow-k Dielectric Fluorocarbon ($k=2.2$), X. Gu, A. Teramoto, R. Kuroda, Y. Tomita, T. Nemoto, S.-i. Kuroki, S. Sugawa, T. Ohmi, Tohoku University 119

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Graphene Interconnect Lifetime Under High Current Stress, X. Chen, D. Seo*, S. Seo**, H. Chung*, H.-S.P. Wong, 121
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Operation of Functional Circuit Elements using BEOL-Transistor with InGaZnO Channel for On-chip High/Low Voltage Bridging I/Os and High-Current Switches, K. Kaneko, H. Sunamura, M. Narihiro, S. Saito, N. Furutake, M. Hane, Y. Hayashi, Renesas Electronics Corporation 123

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14.5 - 5:05 p.m.

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*National Taiwan University, **Chang Gung University, University of California, Berkeley

CIRCUITS SESSION 8 – TAPA I
Technology/Circuit Joint Focus Session - Advanced SRAM

Thursday, June 14, 8:05 a.m.

Chairpersons: G. Lehmann, Infineon Technologies AG
H. Yamauchi, Fukuoka Institute of Technology

C- 8.1 - 8:05 a.m.

A 0.41 μ A Standby Leakage 32Kb Embedded SRAM with Low-Voltage Resume-Standby Utilizing All Digital Current Comparator in 28nm HKMG CMOS, N. Maeda, S. Komatsu, M. Morimoto, Y. Shimazaki, Renesas Electronics Corp. N/A

C- 8.2 - 8:30 a.m.

A 13.8pJ/Access/Mbit SRAM with Charge Collector Circuits for Effective Use of Non-Selected Bit Line Charges, S. Moriwaki, Y. Yamamoto, A. Kawasumi, T. Suzuki*, S. Miyano, T. Sakurai**, H. Shinohara, Semiconductor Technology Academic Research Center, *Panasonic Corp., **University of Tokyo N/A

C-8.3 - 8:55 a.m.

A SRAM Cell Array with Adaptive Leakage Reduction Scheme for Data Retention in 28nm High-K Metal-Gate CMOS, P. Hsu, Y. Tang, D. Tao, M.-C. Huang, M.-J. Wang, C. Wu, Q. Li, TSMC N/A

C- 8.4 - 9:20 a.m.

A 28nm High-k Metal-Gate SRAM with Asynchronous Cross-Couple Read Assist (AC2RA) Circuitry Achieving 3X Reduction on Speed Variation for Single Ended Arrays, R. Lee, J.-P. Yang, C.-E. Huang, C.-C. Chiu, W.-S. Kao, H.-C. Cheng, H.-J. Liao, J. Chang, TSMC N/A

Session 15 – TAPA 2
CMOS Platform

Thursday, June 14, 8:05 a.m.

Chairs: W. Maszara, Globalfoundries
S. Inaba, Toshiba Corp.

15.1 - 8:05 a.m.

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Divakaruni, S. Bukofsky, J.D. Kim^, J. Sudijono**, W. Neumueller#, F. Matsuoka^^, R. Sampson*, IBM Microelectronics,
*STMicroelectronics, **GLOBALFOUNDRIES, ^Samsung Electronics, ^^Toshiba Corporation, #IMC GmbH

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Research and Development Center

Session 16 – TAPA 3
Noise Phenomena

Thursday, June 14, 8:05 a.m.

Chairs: C. Mazure, SOITEC Group
S.S. Chung, Nat'l Chiao Tung Univ.

16.1 - 8:05 a.m.

Voltage and Temperature Dependence of Random Telegraph Noise in Highly Scaled HKMG ETSOI nFETs and its Impact on Logic Delay Uncertainty, H. Miki, M. Yamaoka, D.J. Frank*, K. Cheng*, D.-G. Park*, E. Leobandung*, K.Torii**, Hitachi America, Ltd., IBM Corp, **Hitachi Ltd. **137**

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16.3 - 8:55 a.m.

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16.4 - 9:20 a.m.

Continuous Characterization of MOSFET From Low-Frequency Noise to Thermal Noise Using a Novel Measurement System up to 100 MHz, K. Ohmori, R. Hasunuma, W. Feng, K. Yamada, University of Tsukuba **143**

Session 17 – TAPA 2

Technology / Circuits Joint Focus Session – Design in Scaled Technologies

Thursday, June 14, 10:00 a.m.

Chairs: J. Cheek, Freescale
R. Takemura, Hitachi, Ltd.

T-17.1 – 10:00 a.m.

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Designing in Scaled Technologies: 32nm and Beyond (Invited), S. Kosonocky, T. Burd, K. Kasprak, R. Schultz, R. Stephay, AMD 147

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Dynamic Intrinsic Chip ID Using 32nm High-K/Metal Gate SOI Embedded DRAM, D. Fainstein, S. Rosenblatt, A. Cestero, N/A
N. Robson, T. Kirihata, S.S. Iyer, IBM Systems and Technology Group

C-17.5 – 11:40 a.m.

A Fully-Digital Phase-Locked Low Dropout Regulator in 32nm CMOS, A. Raychowdhury, D. Somasekhar, J. Tschanze, V. De, Intel Corp. N/A

Session 18 – TAPA 3
RRAM II

Thursday, June 14, 10:00 a.m.

Chairs: G. Jurczak, IMEC
Y. Nakao, Rohm Co., Ltd.

18.1 - 10:00 a.m.

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18.2 - 10:25 a.m.

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CIRCUITS SESSION 12 – Tapa 1
Technology/Circuits Joint Focus Session - Design Enablement in Scaled CMOS

Thursday, June 14, 1:30 p.m.

Chairpersons: K. Wilcox, AMD
K. Nose, Renesas Electronics Corp.

C-12.1 - 1:30 p.m.

A 22nm Dynamically Adaptive Clock Distribution for Voltage Droop Tolerance, K. Bowman, C. Tokunaga, T. Karnik, V. De, J. Tschanz, Intel N/A

C-12.2 - 1:55 p.m.

Voltage Droop Reduction Using Throttling Controlled by Timing Margin Feedback, M. Floyd, A. Drake*, R. Berry, H. Chase, R. Willaman, J. Pena, IBM System and Technology Group, *IBM Austin Research Lab N/A

C-12.3 - 2:20 p.m.

An On-Die All-Digital Delay Measurement Circuit with 250fs Accuracy, M. Mansuri, B. Casper, F. O'Mahony, Intel Corporation N/A

C-12.4 - 2:45 p.m.

A 47% Access Time Reduction with a Worst-Case Timing-Generation Scheme Utilizing a Statistical Method for Ultra Low Voltage SRAMs, A. Kawasumi, Y. Takeyama, O. Hirabayashi, K. Kushida, F. Tachibana, Y. Niki, S. Sasaki, T. Yabe, Toshiba N/A

Session 19 – TAPA 2
High Mobility – Ge Devices

Thursday, June 14, 1:30 p.m.

Chairs: T. Ernst, CEA-LETI, MINATEC
T. Tanaka, Fujitsu Semiconductor

19.1 - 1:30pm

High Mobility Ge pMOSFETs with 0.7 nm Ultrathin EOT using HfO₂/Al₂O₃/GeO_x/Ge Gate Stacks Fabricated by Plasma Post Oxidation, R. Zhang, P.-C. Huang, N. Taoka, M. Takenaka, S. Takagi, University of Tokyo 161

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19.4 - 2:45 p.m.

Segmented-Channel Si_{1-x}Ge_x/Si pMOSFET for Improved I_{ON} and Reduced Variability, B. Ho, N. Xu, B. Wood*, V. Tran*, S. Chopra*, Y. Kim*, B.-Y. Nguyen**, O. Bonnin**, C. Mazure**, S. Kuppurao*, C.-P. Chang*, T.-J. King Liu, University of California, Berkeley, *Applied Materials, **SOITEC 167

Session 20 - TAPA 3
3D Integration Technology

Thursday, June 14, 1:30 p.m.

Chairs: A. Antonelli, Novellus Systems, Inc.
T. Tanaka, Tohoku Univ.

20.1 - 1:30 p.m.

Ultrafast Parallel Reconfiguration of 3D-Stacked Reconfigurable Spin Logic Chip with On-chip SPRAM (SPin-transfer torque RAM), T. Tanaka, H. Kino, R. Nakazawa, K. Kiyoyama*, H. Ohno, M. Koyanagi, Tohoku University, *Nagasaki Institute of Applied Science **169**

20.2 - 1:55 p.m.

Development of Ultra-Thin Chip-on-Wafer Process Using Bumpless Interconnects for Three-Dimensional Memory/Logic Applications, N. Maeda, H.Kitada, K. Fujimoto**, Y. Kim, S.Kodama*, S.Yoshimi**, M. Akazawa**, Y. Mizushima^, T. Ohba, University of Tokyo, *DISCO Corporation, **Dai Nippon Printing, ^Fujitsu Laboratory Ltd. **171**

20.3 - 2:20 p.m.

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20.4 - 2:45 p.m.

Demonstration of Inter-chip Data Transmission in a Three-dimensional Stacked Chip Fabricated by Chip-level TSV Integration, K. Hozawa, F. Furuta, Y. Hanaoka, M. Aoki, K. Osada, K. Takeda, K.W. Lee*, T. Fukushima*, M. Koyanagi*, ASET, *Tohoku University **175**

CIRCUITS SESSION 14 – TAPA II
Technology/Circuits Focus Session - Embedded Memory

Thursday, June 14, 3:25 p.m.

Chairpersons: L. Cheng, Oracle

M. Yamaoka, Hitachi America, Ltd.

C- 14.1 - 3:25 p.m.

Isolated Preset Architecture for a 32nm SOI embedded DRAM Macro, J. Barth, D. Plass, A. Vehabovic, R. Joshi*, R. Kanj*, S. Burns, T. Weaver, IBM Systems and Technology Group, *IBM Research N/A

C-14.2 - 3:50 p.m.

A 260mV L-shaped 7T SRAM with Bit-Line (BL) Swing Expansion Schemes Based on Boosted BL, Asymmetric- V_{TH} Read-Port, and Offset Cell VDD Biasing Techniques, M.-P. Chen, L.-F. Chen, M.-F. Chang, S.-M. Yang, Y.-J. Kuo, J.-J. Wu, M.-S. Ho**, H.-Y. Su*, Y.-H. Chu*, W.-C. Wu*, T.-Y. Yang*, H. Yamauchi[^], National Tsing Hua University, *ICL, ITRI, **National Chung Hsing University, [^]Fukuoka Institute of Technology N/A

C- 14.3 - 4:15 p.m.

A 1.6-mm² 38-mW 1.5-Gb/s LDPC Decoder Enabled by Refresh-Free Embedded DRAM, Y.S. Park, D. Blaauw, D. Sylvester, Z. Zhang, University of Michigan N/A

C-14.4 - 4:40 p.m.

1Gsearch/sec Ternary Content Addressable Memory Compiler with Silicon-Aware Early-Predict Late-Correct Single-Ended Sensing, I. Arsovski, T. Hebig, D. Dobson, R. Wistort, IBM Systems Technology Group N/A

C- 14.5 - 5:05 p.m.

A 2.8GHz 128-entry x 152b 3-Read/2-Write Multi-Precision Floating-Point Register File and Shuffler in 32nm CMOS, S. Hsu, A. Agarwal, M. Anders, H. Kaul, S. Mathew, F. Sheikh, R. Krishnamurthy, S. Borkar, Intel Corporation N/A

Session 21 – TAPA 2
Scaled III-V Transistors and Modeling

Thursday, June 14, 3:25 p.m.

Chairs: J. Kavalieros, Intel Corp.
B.H. Lee, Gwangju Institute of Sci. and Tech.

21.1 - 3:25 p.m.

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21.2 - 3:50 p.m.

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*University of Modena and Emilia, **CNSE, [^]Teledyne, ^{^^}Massachusetts Institute of Technology

21.3 - 4:15 p.m.

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