2012 Symposium on VLSI Circuits

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Session 1 – Coral Ballroom 4 and 5
Plenary Session

Wednesday, June 13, 8:05 a.m.
Chairpersons: V. De, Intel Corp.
H. Kabuo, Panasonc Corp.

8:05 a.m. **Welcome, Opening Remarks, and Awards**
A. Amerasekera, Texas Instruments
M. Nagata, Kobe University

1.1 – 8:35 a.m.
The Evolution of Next Generation Data Center Networks for High Capacity Computing, Nicholas Ilyadis, Broadcom Corporation M

1.2 – 9:20 a.m.
Technology Innovations for Smart Cities, Akira Maeda, Hitachi, Ltd. C

Session 2 – Coral Ballroom 4

Phase Locked Loops and Oscillators

Wednesday, June 13, 10:05 a.m

Chairpersons: B. Nauta, University of Twente
S. Cho, KAIST

2.1 - 10:25 a.m.

Components for Generating and Phase Locking 390-GHz Signal in 45-nm CMOS, D. Shim#, D. Koukis, D. Arenas, D. Tanner, E. Seok*, J. Brewer, K. O**, #University of Florida and Seoul National University of Scince and Technology, *Texas Instruments, **University of Texas at Dallas МЛ

2.2 - 10:50 a.m.

A 160-GHz Receiver-Based Phase-Locked Loop in 65 nm CMOS Technology, W.-Z. Chen, T.-Y. Lu, Y.-T. Wang, J.-T. Jian, Y.-H. Yang, G.-W. Huang*, W.-D. Liu*, C.-H. Hsiao*, S.-Y. Lin*, J.Y. Liao*, National Chiao Tung University, *National Nano Device Laboratory МН

2.3 - 11:15 a.m.

A 32.4 ppm/°C 3.2-1.6V Self-chopped Relaxation Oscillator with Adaptive Supply Generation, K.-J. Hsiao, MediaTec Inc. МП

2.4 - 11:40 a.m.

A 280nW, 100kHz, 1-Cycle Start-up Time, On-chip CMOS Relaxation Oscillator Employing a Feedforward Period Control Scheme, T. Tokairin, K. Nose, K. Takeda, K. Noguchi, T. Maeda, K. Kawai, M. Mizuno, Renesas Electronics Corporation **МС**

TECHNOLOGY SESSION 10 – Coral Ballroom 5

Technology / Circuits Joint Focus Session – Memory

Wednesday, June 13, 10:25 a.m.
Chairs: J. Zahurak, Micron Technology

T-10.1 – 10:25 a.m.
SRAMs Design in Nano-Scale CMOS Technologies (Invited), K. Zhang, Intel Corp. bk!

T-10.2 – 10:50 a.m.
Hybrid Memory Cube New DRAM Architecture Increases Density and Performance (Invited), J. Jeddeloh, B. Keeth, bk!
Micron

T-10.3 – 11:15 a.m.
Restructuring of Memory Hierarchy in Computing System with Spintronics-Based Technologies (Invited), T. Endoh, T. bk!
Ohsawa, H. Koike, T. Hanyu, H. Ohno, Tohoku University

T-10.4 - 11:40 a.m.
A Highly Pitch Scalable 3D Vertical Gate (VG) NAND Flash Decoded by a Novel Self-Aligned Independently Controlled Double Gate (IDG) String Select Transistor (SSL), C.-P. Chen, H.-T. Lue, K.-P. Chang, Y.-H. Hsiao, C.-C. Hsieh, S.-H. Chen, Y.-H. Shih, K.-Y. Hsieh, T. Yang, K.-C. Chen, C.-Y. Lu, Macronix International., Ltd. **bk!**

Session 3 – Coral Ballroom 2
Analog Devices

Wednesday, June 13, 10:25 a.m.
Chairpersons: J. Paramesh, Carnegie Mellom
M. Ikeda, University of Tokyo

3.1 - 10:25 a.m.
Circuit Techniques to Overcome Class–D Audio Amplifier Limitations in Mobile Devices, X. Jiang, J. Song, M. Wang, J. Chen, S.K. Arunachalam, T. Brooks, Broadcom Corporation

3.2 - 10:50 a.m.
A 5.2mW, 0.0016% THD up to 20kHz, Ground-Referenced Audio Decoder with PSRR-enhanced Class-AB 16Ω Headphone Amplifiers, S.-H. Wen, C.-C. Yang, MediaTek Inc.

3.3 - 11:15 a.m.
A Sub-1V 3.9µW Bandgap Reference with a 3σ Inaccuracy of ±0.34% from −50°C to +150°C using Piecewise-Linear-Current Curvature Compensation, S. Sano, Y. Takahashi, M. Horiguchi, M.Ota, Renesas Electronics Corporation

3.4 - 11:40 a.m.
A 1.2V 8.3nJ Energy-Efficient CMOS Humidity Sensor for RFID Applications, Z. Tan, Y. Chae, R. Daamen*, A. Humbert*, Y. Ponomarev*, M. Pertijs*, Delft University of Technology, *NXP Semiconductors

Session 4 – Coral Ballroom 4
A/D Converters

Wednesday, June 13, 1:30 p.m.
Chairpersons: T.C. Carusone, University of Toronto
M. Ito, Renesas Electronics Corp.

4.1 - 1:30 p.m.
A 6b 3GS/s 11mW Fully Dynamic Flash ADC in 40nm CMOS with Reduced Number of Comparators, Y.-S. Shu, MediaTek Inc. нс

4.2 - 1:55 p.m.
An Event-Driven, Alias-Free ADC with Signal-Dependent Resolution, C. Weltin-Wu, Y. Tsividis, Columbia University ну

4.3 - 2:20 p.m.
A 10-Bit 1-GHz 33-mW CMOS ADC, B.D. Sahoo, B. Razavi, University of California, Los Angeles ол

4.4 - 2:45 p.m.
A 61.5dB SNDR Pipelined ADC Using Simple Highly-Scalable Ring Amplifiers, B. Hershberg, S. Weaver, K. Sobue*, S. Takeuchi*, K. Hamashita*, U.-K. Moon, Oregon State University, Asahi Kasei Microdevices он

TECHNOLOGY SESSION 12 – Coral Ballroom 5

Technology / Circuits Joint Focus Session – 3D-System Integration

Wednesday, June 13, 1:30 p.m.

Chairs: A. Antonelli,Novellus Systems, Inc.
T. Tanaka, Tohoku Univ.

T- 12.1 – 1:30 p.m.

Practical Implications of Via-Middle Cu TSV-induced Stress in a 28nm CMOS Technology for Wide-IO Logic-Memory Interconnect (Invited), J. West, Y.S. Choio, C. Vartuli, Texas Instruments

T-12.2 – 1:55 p.m.

Thermal Stress Characteristics and Impact on Device Keep-Out Zone for 3-D ICs Containing Through-Silicon-Vias (Invited),T. Jiang, S-K Ryu, Q. Zhao, J. Im, H-Y Son, K-Y Byun, R. Huang, P.S. Ho, University of Texas, Austin and Hynix

T-12.3 – 2:20 p.m.

Near-Field Wireless Connection for 3D-System Integration (Invited), T. Kuroda, Keio University

T-12-4 - 2:45 p.m.

An Ultra-Thin Interposer Utilizing 3D TSV Technology, W.-C. Chiou, K.-F. Yang, C. Yeh, S.-H. Wang, Y.-H. Liou, T.-J. Wu, J.-C. Lin, C.-C. Hsieh, H.A. Teng, C.C. Chiu, D.C. Yeh, W.C. Wu, A.J. Su, S.L. Chiu, H.-P. Chang, J. Wei, Y.-C. Lin, Y.-H. Chen, H.-J. Tu, H.D. Ko, T.-H. Yu, J.P. Hung, P.-H. Tsai, C.L. Huang, S.W. Lu, S.Y. Hou, D.-Y. Shih, K.H. Chen, S.-P. Jeng, C.-H. Yu, TSMC

Session 5 – Coral Ballroom 2

Ultra Low Power Radios

Wednesday, June 13, 1:30 p.m.
Chairpersons: G. Van der Plas, IMEC
K. Agawa, Toshiba Corp.

5.1 - 1:30 p.m.

A 440pJ/bit 1Mb/s 2.4GHz Multi-Channel FBAR-based TX and an Integrated Pulse-shaping PA, A. Paidimarri, P. Nadeau, P. Mercier, A. Chandrakasan, Massachusetts Institute of Technology

5.2 - 1:55 p.m.

An 8-PPM, 45 pJ/bit UWB Transmitter with Reduced Number of PA Elements, V. Majidzadeh, A. Schmid, Y. Leblebici, J. Rabaey*, EPFL, *University of California, Berkeley

5.3 - 2:20 p.m.

An All 0.5V, 1Mbps, 315MHz OOK Transceiver with 38-µW Career-Frequency-Free Intermittent Sampling Receiver and 52-uW Class-F Transmitter in 40-nm CMOS, A. Saito, K. Honda*, Y. Zheng*, S. Iguchi*, K. Watanabe, T. Sakurai*, M. Takamiya*, STARC, *University of Tokyo

5.4 - 2:45 p.m.

A 2.4GHz Hybrid PPF Based BFSK Receiver with ±180ppm Frequency Offset Tolerance for Wireless Sensor Networks, R. Ni, K. Mayaram, T. Fiez, Oregon State University

Session 6 – Coral Ballroom 4

Technology/Circuits Joint Focus Session - Emerging Nonvolatile Memory

Wednesday, June 13, 3:25 p.m.
Chairpersons: J. DeBrosse, IBM
S. Yamakawa,Sony Corp.

C-6.1 - 3:25 p.m.
A 0.13µm 8Mb Logic Based Cu_xSi_yO Resistive Memory with Self-Adaptive Yield Enhancement and Operation Power Reduction, X.Y. Xue, W.X. Jian, J.G. Yang, F.J. Xiao, G. Chen, X.L. Xu, Y.F. Xie, Y.Y. Lin, R. Huang*, Q.T. Zhou*, J.G. Wu*, Fudan University, *Semiconductor Manufactoring International Corp.

C-6.2 - 3:50 p.m.
A 3.14 um^2 4T-2MTJ-Cell Fully Parallel TCAM Based on Nonvolatile Logic-in-Memory Architecture, S. Matsunaga, S. Miura*, H. Honjou*, K. Kinoshita, S. Ikeda, T. Endoh, H. Ohno, T. Hanyu, Tohoku University, *NEC Corporation

C-6.3 - 4:15 p.m.
1Mb 4T-2MTJ Nonvolatile STT-RAM for Embedded Memories Using 32b Fine-Grained Power Gating Technique with 1.0ns/200ps Wake-up/Power-off Times, T. Ohsawa, H. Koike, S. Miura*, H. Honjo*, K. Tokutome*, S. Ikeda, T. Hanyu, H. Ohno, T. Endoh, Tohoku University, *NEC Coropration

T-6.4 - 4:40 p.m.
A Simple New Write Scheme for Low Latency Operation of Phase Change Memory, Y.-Y. Lin, Y.-C. Chen, F.-M. Lee, M. BrightSky*, H.-L. Lung, C. Lam*, Macronix International Co., Ltd., *IBM T.J. Watson Research Center

T-6.5 - 5:05 p.m.
Analysis of Random Telegraph Noise and Low Frequency Noise Properties in 3-D Stacked NAND Flash Memory with Tube-Type Poly-Si Channel Structure, M.-K. Jeong, S.-M. Joe, C.-S. Seo, K.-R. Han*, E. Choi*, S.-K. Park*, J.-H. Lee, Seoul National University, *Hynix Semiconductor Inc.

Session 7 – Coral Ballroom 2

High Data Rate Wireless and Imaging

Wednesday, June 13, 3:25 p.m.

Chairpersons: A. Cathelin, STMicroelectronics
C.M. Hung, MStar Semiconductor, Inc.

7.1 - 3:25 p.m.

A 260 GHz Fully Integrated CMOS Transceiver for Wireless Chip-to-Chip Communication, J.-D. Park, S. Kang, S. Thyagarajan, E. Alon, A. Niknejad, University of California, Berkeley

7.2 - 3:50 p.m.

135 GHz 98 mW 10 Gbps ASK Transmitter and Receiver Chipset in 40 nm CMOS, N. Ono, M. Motoyoshi*, K. Takano*, K. Katayama*, R. Fujimoto**, M. Fujishima*, Semiconductor Technology Academic Research Center, *Hiroshima University, **Toshiba Corp.

7.3 - 4:15 p.m.

A 21.5mW 10+Gb/s mm-Wave Phased-Array Transmitter in 65nm CMOS, L. Kong, E. Alon, University of California, Berkeley

7.4 - 4:40 p.m.

A UWB IR Timed-Array Radar Using Time-Shifted Direct-Sampling Architecture, C.-M. Lai, K.-W. Tan, L.-Y. Yu, Y.-J. Chen, J.-W. Huang, S.-C. Lai, F.-H. Chung, C.-F. Yen, J.-M. Wu, P.-C. Huang, K.-J. Chang, S.-Y. Huang, T.-S. Chu, National Tsing Hua University

7.5 - 5:05 p.m.

A 94GHz mm-Wave to Baseband Pulsed-Radar for Imaging and Gesture Recognition, A. Arbabian, S. Kang*, S. Callender*, J.-C. Chien*, B. Afshar*, A. Niknejad*, Stanford University, *University of California, Berkeley

Session 8 – Coral Ballroom 4

Technology/Circuit Joint Focus Session - Advanced SRAM

Thursday, June 14, 8:05 a.m.

Chairpersons: G. Lehmann, Infineon Technologies AG
H. Yamauchi, Fukuoka Institute of Technology

8.1 - 8:05 a.m.

A 0.41µA Standby Leakage 32Kb Embedded SRAM with Low-Voltage Resume-Standby Utilizing All Digital Current Comparator in 28nm HKMG CMOS, N. Maeda, S. Komatsu, M. Morimoto, Y. Shimazaki, Renesas Electronics Corp.

8.2 - 8:30 a.m.

A 13.8pJ/Access/Mbit SRAM with Charge Collector Circuits for Effective Use of Non-Selected Bit Line Charges, S. Moriwaki, Y. Yamamoto, A. Kawasumi, T. Suzuki*, S. Miyano, T. Sakurai**, H. Shinohara, Semiconductor Technology Academic Research Center, *Panasonic Corp., **University of Tokyo

8.3 - 8:55 a.m.

A SRAM Cell Array with Adaptive Leakage Reduction Scheme for Data Retention in 28nm High-K Metal-Gate CMOS, P. Hsu, Y. Tang, D. Tao, M.-C. Huang, M.-J. Wang, C. Wu, Q. Li, TSMC

8.4 - 9:20 a.m.

A 28nm High-k Metal-Gate SRAM with Asynchronous Cross-Couple Read Assist (AC2RA) Circuitry Achieving 3X Reduction on Speed Variation for Single Ended Arrays, R. Lee, J.-P. Yang, C.-E. Huang, C.-C. Chiu, W.-S. Kao, H.-C. Cheng, H.-J. Liao, J. Chang, TSMC

Session 9 – Coral Ballroom 2

Medical Electronics

Thursday, June 14, 8:05 a.m.

Chairpersons: J. Gealow, MediaTek Wireless, Inc.
C.-Y. Lee,National Chiao Tung University

9.1 - 8:05 a.m.

A 0.6V 2.9µW Mixed-Signal Front-End for ECG Monitoring, M. Yip, J.L. Bohorquez*, A.P. Chandrakasan, Massachusetts Institute of Technology, *Convergence Medical Devices CC

9.2 - 8:30 a.m.

A 700µW 8-Channel EEG/Contact-impedance Acquisition System for Dry-electrodes, S. Mitra, J. Xu, A. Matsumoto*, K.A.A. Makinwa**, C. Van Hoof, R.F. Yazicioglu, imec, *Panasonic Corporation, **Delft University of Technology CY

9.3 - 8:55 a.m.

A Wirelessly Powered Log-based Closed-loop Deep Brain Stimulation SoC with Two-way Wireless Telemetry for Treatment of Neurological Disorders, H.-G. Rhew, J. Jeong, J. Fredenburg, S. Dodani, P. Patil, M.Flynn, University of Michigan **TЛ**

9.4 - 9:20 a.m.

A Fully-Integrated 10.5µW Miniaturized (0.125mm^2) Wireless Neural Sensor, D. Yeager, W. Biederman, N. Narevsky, E. Alon, J. Rabaey, University of California, Berkeley TH

Session 10 – Coral Ballroom 4

Wireless Connectivity and Software Defined Radios

Thursday, June 14, 10:00 a.m.

Chairpersons: B. Ginsberg, Texas Instruments
H. Ishikuro, Keio University

10.1 - 10:00 a.m.

A -70dBm-Sensitivity 522Mbps 0.19nJ/bit-TX 0.43nJ/bit-RX Transceiver for TransferJet™ SoC in 65nm CMOS, D. Miyashita, K.Agawa, H. Kajihara, K. Sami, M. Iwanaga, Y. Ogasawara, T. Ito, D. Kurose, N. Koide, T. Hashimoto, H. Sakurai, T. Yamaji, T. Kurihara, K.Sato, I. Seto, H. Yoshid, R. Fujimoto, Y. Unikawa, Toshiba Corp.

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10.2 - 10:25 a.m.

A 2.4GHz WLAN Transceiver with Fully-integrated Highly-linear 1.8V 28.4dBm PA, 34dBm T/R Switch, 240MS/s DAC, 320MS/s ADC, and DPLL in 32nm SoC CMOS, Y. Tan, J. Duster, C.-t. Fu, E. Alpman, A. Balankutty, C.C. Lee, A. Ravi, S. Pellerano, K. Chandrashekar, H. S. Kim, B. Carlton, S. Suzuki, M. Shafi, Y. Palaskas, H. Lakdawala, Intel Corporation

тс

10.3 - 10:50 a.m.

A +30.5 dBm CMOS Doherty Power Amplifier with Reliability Enhancement Technique, K.Onizuka, S. Saigusa, S.Otaka, Toshiba Corporation

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10.4 - 11:15 a.m.

A Harmonic-Rejecting CMOS LNA for Broadband Radios, J.W. Park, B. Razavi, University of California, Los Angeles

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10.5 - 11:40 a.m.

A 13.5mA Sub-2.5dB NF Multi-Band Receiver, M. Mikhemar, A. Mirzaei, A. Hadji-Abdolhamid, J. Chiu, H. Darabi, Broadcom Corporation

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Technology Session 17 – Coral Ballroom 1

Technology / Circuits Joint Focus Session – Design in Scaled Technologies

Thursday, June 14, 10:00 a.m.

Chairs: J. Cheek, Freescale
R. Takemura, Hitachi, Ltd.

T-17.1 – 10:00 a.m.

Design Enablement at 14nm: The Challenge of Being Early, Accurate, and Complete (Invited), M.E. Mason, Texas bк! Instruments

T-17.2 – 10:25 a.m.

Designing in Scaled Technologies: 32nm and Beyond (Invited), S. Kosonocky, T. Burd, K. Kasprak, R. Schultz, R. Stephay, bк! AMD

T-17.3 – 10:50 a.m.

The Optimum Device Parameters for High RF and Analog/MS Performance in Planar MOSFET and FinFET (Invited) T. bк! Ohguro, Y. Higashi, K. Okano, S. Inaba, Y. Toyoshima, Toshiba

C-17.4 – 11:15 a.m.

Dynamic Intrinsic Chip ID Using 32nm High-K/Metal Gate SOI Embedded DRAM, D. Fainstein, S. Rosenblatt, A. Cestero, мпс N. Robson, T. Kirihata, S.S. Iyer, IBM Systems and Technology Group

C-17.5 – 11:40 a.m.

A Fully-Digital Phase-Locked Low Dropout Regulator in 32nm CMOS, A. Raychowdhury, D. Somasekhar, J. Tschanze, V. мпу De, Intel Corp.

Session 11 – Coral Ballroom 2

Successive Approximation A/D Converters

Thursday, June 14, 10:00 a.m.

Chairpersons: M. Flynn, University of Michigan
S. Dosho, Panasonic Corp.

11.1 - 10:00 a.m.

A 2.8GS/s 44.6mW Time-Interleaved ADC Achieving 50.9dB SNDR and 3dB Effective Resolution Bandwidth of 1.5GHz in 65nm CMOS, D. Stepanovic, B. Nikolic, University of California, Berkeley

11.2 - 10:25 a.m.

A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure, C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, R. Martins*, University of Macau, *TU of Lisbon

11.3 - 10:50 a.m.

A 4.5-mW 8-b 750-MS/s 2-b/Step Asynchronous Subranged SAR ADC in 28-nm CMOS Technology, Y.-C. Lien, MediaTek

11.4 - 11:15 a.m.

A 34fJ 10b 500 MS/s Partial-Interleaving Pipelined SAR ADC, Y. Zhu, C.-H. Chan, S.-W. Sin, S.-P. U, R. Martins*, University of Macau, *TU of Lisbon

11.5 - 11:40 a.m.

A 3.2fJ/c.-s. 0.35V 10b 100KS/s SAR ADC in 90nm CMOS, H.-Y. Tai, H.-W. Chen, H.-S. Chen, National Taiwan University

Session 12 – Coral Ballroom 4

Technology/Circuits Joint Focus Session - Design Enablement in Scaled CMOS

Thursday, June 14, 1:30 p.m.
Chairpersons: K. Wilcox, AMD
K. Nose, Renesas Electronics Corp.

12.1 - 1:30 p.m.
A 22nm Dynamically Adaptive Clock Distribution for Voltage Droop Tolerance, K. Bowman, C. Tokunaga, T. Karnik, V. De, J. Tschanz, Intel

12.2 - 1:55 p.m.
Voltage Droop Reduction Using Throttling Controlled by Timing Margin Feedback, M. Floyd, A. Drake*, R. Berry, H. Chase, R. Willaman, J. Pena, IBM System and Technology Group, *IBM Austin Research Lab

12.3 - 2:20 p.m.
An On-Die All-Digital Delay Measurement Circuit with 250fs Accuracy, M. Mansuri, B. Casper, F. O'Mahony, Intel Corporation

12.4 - 2:45 p.m.
A 47% Access Time Reduction with a Worst-Case Timing-Generation Scheme Utilizing a Statistical Method for Ultra Low Voltage SRAMs, A. Kawasumi, Y. Takeyama, O. Hirabayashi, K. Kushida, F. Tachibana, Y. Niki, S. Sasaki, T. Yabe, Toshiba

Session 13 – Coral Ballroom 2

High Performance Transceivers

Thursday, June 14, 1:30 p.m.

Chairpersons: J. Zerbe, Rambus

J. Terada, NTT Microsystem Integration Labs

13.1 - 1:30 p.m.

A 3.1mW/Gbps 30Gbps Quarter-Rate Triple-Speculation 15-tap SC-DFE RX Data Path in 32nm CMOS, T. Toifl, M. Ruegg*, R. Inti**, C. Menolfi, M. Brändli, M. Kossel, P. Buchmann, P.A. Francese, T. Morf, IBM Research GmbH, *Miromico, **Oregon State University

МЛН

13.2 - 1:55 p.m.

A Wide Common-Mode Fully-Adaptive Multi-Standard 12.5Gb/s Backplane Transceiver in 28nm CMOS, J. Savoj, K. Hsieh, P. Upadhyaya, F.-T. An, A. Bekele, S. Chen, X. Jiang, K.W. Lai, C.F. Poon, A. Sewani, D. Turker, K. Venna, D. Wu, B. Xu, E. Alon*, K. Chang, Xilinx, Inc., *University of California, Berkeley

МЛП

13.3 - 2:20 p.m.

A 25-Gb/s 2.2-W Optical Transceiver Using an Analog FE Tolerant to Power Supply Noise and Redundant Data Format Conversion in 65-nm CMOS, T. Takemoto, H. Yamashita, T. Kamimura, F. Yuki, N. Masuda, H. Toyoda, N. Chujo, K. Kogo, Y. Lee, S. Tsuji, S. Nishimura, Hitachi, Ltd.

МЛС

13.4 - 2:45 p.m.

A 100+ meter 12Gb/s/Lane Copper Cable Link Based on Clock-Forwarding, T. Ali, W.H. Park, P. Mulage, E.-H. Chen, R. Ho*, C.-K.K. Yang, UCLA, *Oracle Labs

МЛУ

Session 14 – Coral Ballroom 4

Technology/Circuits Focus Session - Embedded Memory

Thursday, June 14, 3:25 p.m.

Chairpersons: L. Cheng, Oracle
M. Yamaoka, Hitachi America, Ltd.

14.1 - 3:25 p.m.

Isolated Preset Architecture for a 32nm SOI embedded DRAM Macro, J. Barth, D. Plass, A. Vehabovic, R. Joshi*, R. Kanj*, S. Burns, T. Weaver, IBM Systems and Technology Group, *IBM Research ММЛ

14.2 - 3:50 p.m.

A 260mV L-shaped 7T SRAM with Bit-Line (BL) Swing Expansion Schemes Based on Boosted BL, Asymmetric-V_{TH} Read-Port, and Offset Cell VDD Biasing Techniques, M.-P. Chen, L.-F. Chen, M.-F. Chang, S.-M. Yang, Y.-J. Kuo, J.-J. Wu, M.-S. Ho**, H.-Y. Su*, Y.-H. Chu*, W.-C. Wu*, T.-Y. Yang*, H. Yamauchi^, National Tsing Hua University, *ICL, ITRI, **National Chung Hsing University, ^Fukuoka Institute of Technology **ММН**

14.3 - 4:15 p.m.

A 1.6-mm2 38-mW 1.5-Gb/s LDPC Decoder Enabled by Refresh-Free Embedded DRAM, Y.S. Park, D. Blaauw, D. Sylvester, Z. Zhang, University of Michigan ММП

14.4 - 4:40 p.m.

1Gsearch/sec Ternary Content Addressable Memory Compiler with Silicon-Aware Early-Predict Late-Correct Single-Ended Sensing, I. Arsovski, T. Hebig, D. Dobson, R. Wistort, IBM Systems Technology Group **ММС**

14.5 - 5:05 p.m.

A 2.8GHz 128-entry x 152b 3-Read/2-Write Multi-Precision Floating-Point Register File and Shuffler in 32nm CMOS, S. Hsu, A. Agarwal, M. Anders, H. Kaul, S. Mathew, F. Sheikh, R. Krishnamurthy, S. Borkar, Intel Corporation ММУ

Session 15 – Coral Ballroom 2

Analog Sensor Interfaces

Thursday, June 14, 3:25p.m.

Chairpersons: J. Lloyd, Analog Devices
J. Lee, National Taiwan University

15.1 - 3:25 p.m.

High-resolution Sensing Sheet for Structural-health Monitoring via Scalable Interfacing of Flexible Electronics with High-performance ICs, Y. Hu, W. Rieutort-Louis, J. Sanz-Robinson, K. Song, J.C. Sturm, S. Wagner, N. Verma, Princeton University МНЛ

15.2 - 3:50 p.m.

Nanostructured CMOS Wireless Ultra-Wideband Label-free DNA Analysis SoC, H.M. Jafari, L. Soleymani*, K. Abdelhalim, E. Sargent, S. Kelley, Roman Genov, University of Toronto, *McMaster University МНН

15.3 - 4:15 p.m.

A Fully Integrated Hepatitis B Virus (HBV) DNA Detection SoC based on Monolithic Polysilicon Nanowire CMOS Process, C.-W. Huang, Y.-J. Huang, P.-W. Yen, H.-T. Hsueh, C.-Y. Lin*, M.-C. Chen*, C.-H. Ho*, F.-L. Yang*, H.-H. Tsai**, H.-H. Liao**, Y.-Z. Juang**, C.-K. Wang, C.-T. Lin, S.-S. Lu, National Taiwan University, *National Nano Device Laboratories, **National Applied Research Laboratories МНП

15.4 - 4:40 p.m.

A Fully-Electronic Charge-Based DNA Sequencing CMOS Biochip, A. Manickam, R. Singh, N. Wood, B. Li, A. Ellington, A. Hassibi, University of Texas at Austin МНС

15.5 - 5:05 p.m.

An 88dB SNR, 30µm Pixel Pitch Infra-Red Image Sensor with a 2-Step 16 bit A/D Conversion, A. Peizerat, J.-P. Rostaing, N. Zitouni, N. Baier, F. Guellec, R. Jalby, M. Tchagaspanian, CEA-LETI, Minatec МНУ

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 12
8:00 p.m. – 10:00 p.m.

Organizers:

Circuits	**Technology**
N. Lu, Etron	T. Skotnicki, STMicroelectronics
M. Bauer, Micron	K. Miyashita, Toshiba

RJ1: Scaling Challenges Beyond 1x nm DRAM and NAND Flash

Moderator: N. Lu, Etron
R. Shrivastava, SanDisk

The combined revenues of DRAM and NAND Flash approached $54 Billion in 2010. This is expected to continue to grow in the coming years. Emerging silicon and package technologies will further drive lower cost and new applications. The difficulty of scaling and developing new technologies and investments to build new factories is increasing at about the same rate as the memory bit growth in the world. At the same time, the industry is becoming aware that we are closing in on physical and electrical scaling limitations. As we close in on scaling limits, the use of new materials, manufacturing processes, and circuit design will become unavoidable. To compound the problem, fierce competition is forcing shorter development times. Our industry needs to openly address these issues and challenges in order to continue developing better and lower cost memories for the decade to come. The whole industry faces these challenges and issues. They are huge. We have assembled a representative group of industry experts for this Joint Rump Session. We will ask them to discuss the top issues from the perspective of each one's area of expertise. The floor will be open to question the panelist's view or challenge them to consider issues that audience would like to raise.

Panelists:

S. Aritome, Hynix
G. Atwood, Micron
G. Bronner, Rambus
H. Hazama, Toshiba
H-K Kang, Samsung
M. Koyanagi, Tohoku University
C.Y. Lu, Macronix
K. Takeuchi, University of Tokyo

CIRCUITS RUMP SESSION
Thursday, June 14
8:00 p.m. – 10:00 p.m.

Organizers: J. Zerbe, Rambus
K. Agawa, Toshiba

R1: Is VLSI Innovation Dead?

Moderator: J. Zerbe, Rambus

Since the 90's the drop-off in venture-capitalist funded semiconductor startups has been noticeably precipitous. Between the burst of the internet bubble and the economic slowdown, IC companies seem like they are taking a back seat. Headlines touting innovative companies are now dominated by web software or server/OEMs with chip companies noticeably absent. Memory has matured, processors have matured, even networking and performance graphics has matured. Attend any conference with a grizzled IC veteran and you may hear the standard refrain "it's all been done before". The question is: is VLSI semiconductor innovation fine, dead, dying, or does it just need some kind of kick-start?

Panelists:

M. Horowitz, Stanford
S. Kawahito, Shizuoka Univ.
S. Kosonocky, AMD
H. Lee, MIT
H. Morimura, NTT
G. Shahidi, IBM
I. Young, Intel

R2: Will the Future Have More Analog or Digital Processing?

Organizers: B. Ginsburg, Texas Instruments
M. Takamiya, University of Tokyo

Moderator: B. Ginsburg, Texas Instruments

Since the early days of DSP, traditional analog functionality has been increasingly replaced by digital circuits, due to added flexibility, robustness, and the promise of smaller area and lower power operation. The extent of digital has progressed commensurate with the ability to efficiently digitize signals. ADC energy efficiency has improved by more than 500x over the last decade, such that it can be more efficient to generate bits than actually process them in the digital domain. Given new technology nodes do not exhibit the same digital energy scaling as experienced in the past, will real energy-constrained systems become increasingly analog in their partitioning? Is the push towards digital replacing analog finished, or is the overall trend irreversible?

Panelists:
E. Alon, Univ. of California, Berkeley
M. Ikeda, University of Tokyo
T. Miki, Renesas Electronics
A. Momtaz, Broadcom
K. Nakamura, Analog Devices
J. Savoj, Xilinx

Session 16 – Tapa I

Circuits Special Focus Session - Flash Memory

Friday, June 15, 8:05 a.m.

Chairpersons: M. Bauer, Micron Tech.
H. Hwang, Samsung Electronics Co., Ltd.

16.1 - 8:05am

A Logic-Compatible Embedded Flash Memory Featuring a Multi-Story High Voltage Switch and a Selective Refresh Scheme, S.-H. Song, K.C. Chun, C.H. Kim, University of Minnesota **МОЛ**

16.2 - 8:30 a.m.

A New 3-bit Programming Algorithm using SLC-to-TLC Migration for 8MB/s High Performance TLC NAND Flash Memory, S.-h. Shin, D.-K. Shim, J.-Y. Jeong, O.-S. Kwon, S.-Y. Yoon, M.-H. Choi, T.-Y. Kim, H.-W. Park, H.-J. Yoon, Y.-S. Song, Y.-H. Choi, S.-W. Shim, Y.-L. Ahn, K.-T. Park, J.-M. Han, K.-H. Kyung, Y.-H. Jun, Samsung Electronics **МОН**

16.3 - 8:55 a.m.

x11 Performance Increase, x6.9 Endurance Enhancement, 93% Energy Reduction of 3D TSV-Integrated Hybrid ReRAM/MLC NAND SSDs by Data Fragmentation Suppression, H. Fujii, K. Miyaji, K. Johguchi, K. Higuchi, C. Sun, K. Takeuchi, University of Tokyo **МОП**

16.4 - 9:20 a.m.

Adaptive Multi-Pulse Program Scheme Based on Tunneling Speed Classification for Next Generation Multi-Bit/Cell NAND FLASH, Y.S. Cho, I.H. Park, S.Y. Yoon, N.H. Lee, S.H. Joo, K.-W. Song, K. Choi, J.M. Han, K.H. Kyung , Y.-H. Jun, Samsung Electronics Co., Ltd. **МОС**

Session 17 – Tapa II

Low Power Receivers and Jitter Reduction

Friday, June 15, 8:05 a.m.
Chairpersons: K. Chang, Xilinx
C. Yoo, Hanyang University

17.1 - 8:05 a.m.
A 25-Gb/s 5-mW CMOS CDR/Deserializer, J.W. Jung, B. Razavi, University of California, Los Angeles МОУ

17.2 - 8:30 a.m.
4×12 Gb/s 0.96 pJ/b/lane Analog-IIR Crosstalk Cancellation and Signal Reutilization Receiver for Single-Ended I/Os in 65 nm CMOS, T. Oh, R. Harjani, University of Minnesota **МПЛ**

17.3 - 8:55 a.m.
A Clock Jitter Reduction Circuit Using Gated Phase Blending Between Self-Delayed Clock Edges, K. Niitsu, N. Harigai, D. Hirabayashi, D. Oki, M. Sakurai, O. Kobayashi*, T.J. Yamaguchi, H. Kobayashi, Gunma University, *STARC МПН

17.4 - 9:20 a.m.
A 1.22mW/Gb/s 9.6Gb/s Data Jitter Mixing Forwarded-Clock Receiver Robust against Power Noise with 1.92ns Latency Mismatch between Data and Clock in 65nm CMOS, S.-H. Chung, L.-S. Kim, KAIST **МПП**

Session 18 – Tapa I

SoC and Signal Processors

Friday, June 15, 10:00 a.m.

Chairpersons: E. Yeo, Marvell Semiconductors
M. Motomura, Hokkaido University

18.1 - 10:00 a.m.

A Low Power Many-Core SoC with Two 32-Core Clusters Connected by Tree Based NoC for Multimedia Applications, H. Xu, J. Tanabe, H. Usui, S. Hosoda, T. Sano, K. Yamamoto, T. Kodaka, N. Nonogaki, N. Ozaki, T. Miyamori, Toshiba Corporation мрл

18.2 - 10:25 a.m.

A 69mW 140-meter/60fps and 60-meter/300fps Intelligent Vision SoC for Versatile Automotive Applications, Y.-M. Tsai, T.-J. Yang, C.-C. Tsai, K.-Y. Huang, L.-G. Chen, National Taiwan University мрн

18.3 - 10:50 a.m.

A 4320p 60fps H.264/AVC Intra-Frame Encoder Chip with 1.41Gbins/s CABAC, D. Zhou, G. He, W. Fei, Z. Chen, J. Zhou, S. Goto, Waseda University мрп

18.4 - 11:15 a.m.

A Sub-100µW Multi-Functional Cardiac Signal Processor for Mobile Healthcare Applications, S.-Y. Hsu, Y. Ho, Y. Tseng, T.-Y. Lin, P.-Y. Chang, J.-W. Lee, J.-H. Hsiao, S.-M. Chuang, T.-Z. Yang*, P.-C. Liu, T.-F. Yang, R.-J. Chen**, C. Su, C.-Y. Lee, National Chiao Tung University, *Taipei Medical University Hospital, **Wan Fang Hospital мрс

18.5 - 11:40 a.m.

A 0.25V 460nW Asynchronous Neural Signal Processor with Inherent Leakage Suppression, T.-T. Liu, J. Rabaey, University of California, Berkeley мру

Session 19 – Tapa II

ΔΣ Converters

Friday, June 15, 10:00 a.m.

Chairpersons: I. Fujimori, Broadcom Corp.
M. Yoshioka, Fujitsu Labs, Ltd.

19.1 - 10:00 a.m.

A 10 MHz BW 50 fJ/conv. Continuous Time ΔΣ Modulator with High-order Single Opamp Integrator using Optimization-based Design Method, K. Matsukawa, K. Obata, Y. Mitani, S. Dosho, Panasonic Corporation МСЛ

19.2 - 10:25 a.m.

A 5MHz BW 70.7dB SNDR Noise-Shaped Two-Step Quantizer Based ΔΣ ADC, T. Oh, N. Maghari*, U.-K.Moon, Oregon State University, *University of Florida МСН

19.3 - 10:50 a.m.

An 85dB SFDR 67dB SNDR 8OSR 240MS/s ΣΔ ADC with Nonlinear Memory Error Calibration, S.-C. Lee, B. Elies*, Y. Chiu*, University of Illinois at Urbana-Champagne, *University of Texas at Dallas МСП

19.4 - 11:15 a.m.

A Reconfigurable Mostly-Digital ΔΣ ADC with a Worst-Case FOM of 160dB, G. Taylor, I. Galton*, Analog Devices, *University of California at San Diego МСС

19.5 - 11:40 a.m.

A 71dB Dynamic Range Third-Order ΔΣ TDC Using Charge-Pump, M. Gande, N. Maghari*, T. Oh, U.-K. Moon, Oregon State University, *University of Florida МСУ

Session 20 – Tapa I

Clock and Interconnect

Friday, June 15, 1:30 p.m.
Chairpersons: N. Kurd, Intel Corp.
R. Kuppuswamy, Intel India

20.1 - 1:30 p.m.

A Shorted Global Clock Design for Multi-GHz 3D Stacked Chips, L.-T. Pang, P. Restle, M. Wordeman, J. Silberman, R. Franch, G. Maier*, IBM TJ Watson Research Center, *IBM Systems and Technology Group МТЛ

20.2 - 1:55 p.m.

A 3-stage Pseudo Single-phase Flip-flop Family, H. Partovi, A. Yeung, L. Ravezzi, M. Horowitz*, Veloce Technologies, Inc., *Stanford University МТН

20.3 - 2:20 p.m.

A Standard Cell Compatible Bidirectional Repeater with Thyristor Assist, S. Satpathy, D. Sylvester, D. Blaauw, University of Michigan МТП

20.4 - 2:45 p.m.

An Integral Path Self-Calibration Scheme for a 20.1-26.7GHz Dual-Loop PLL in 32nm SOI CMOS, M. Ferriss, J.-O. Plouchart, A. Natarajan, A. Rylyakov, B. Parker, A. Babakhani, S. Yaldiz, B. Sadhu, A. Valdes-Garcia, J. Tierno, D. Friedman, IBM TJ Watson Research Center МТС

Session 21 – Tapa II
DC-DC Converters

Friday, June 15, 1:30 p.m.
Chairpersons: T. Burd, AMD
M. Takamiya, University of Toyko

21.1 - 1:30 p.m.
A 50nA Quiescent Current Asynchronous Digital-LDO with PLL-Modulated Fast-DVS Power Management in 40nm CMOS for 5.6 times MIPS Performance, Y.-H. Lee, S.-Y. Peng, C.-H. Wu, C.-C. Chiu, Y.-Y. Yang, M.-H. Huang, K.-H. Chen, Y.-H. Lin*, S.-W. Wang, C.-Y. Yeh*, C.-C. Huang*, C.-C. Lee*, National Chiao Tung University, *Realtek Semiconductor Corp. **МТУ**

21.2 - 1:55 p.m.
High Area-Efficient DC-DC Converter using Time-Mode Miller Compensation (TMMC), S.-W. Hong, T.-H. Kong, S. Jung, Su.-W. Lee, S.-W. Wang, J.-P. Im, G.-H. Cho, KAIST МУЛ

21.3 - 2:20 p.m.
A 900mA 93% Efficient 50µA Quiescent Current Fixed Frequency Hysteretic Buck Converter Using a Highly Digital Hybrid Voltage- and Current-mode Control, Q. Khan, A. Elshazly, S. Rao, R. Inti, P. Hanumolu, Oregon State University **МУН**

21.4 - 2:45 p.m.
A 198-ns/V V_O-Hopping Reconfigurable RGB LED Driver with Automatic ΔV_O Detection and Quasi-Constant-Frequency Predictive Peak Current Control, Y. Zhang, H. Chen*, D. Ma, University of Texas at Dallas, *Linear Technology Corporation **МУП**

Session 22 – Tapa I

Digital Timing Generations Circuits

Friday, June 15, 3:25 p.m.
Chairpersons: A. Emami, CalTech
K. Sunaga, NEC Corp.

22.1 - 3:25 p.m.
Design of a 2.5-GHz, 3-ps Jitter, 8-Locking-Cycle, All-Digital Delay-Locked Loop with Cycle-by-Cycle Phase Adjustment, C.-Y. Cheng, J.-S. Wang, C.-T. Yeh, J.-S. Sheu, National Chung-Cheng University, *United Microelectronics Corp. **МУС**

22.2 - 3:50 p.m.
A 1.5GHz 1.35mW -112dBc/Hz In-band Noise Digital Phase-Locked Loop with 50fs/mV Supply-Noise Sensitivity, A. Elshazly, R. Inti, M. Talegaonkar, P.K. Hanumolu, Oregon State University **МУУ**

22.3 - 4:15 p.m.
A 61-dB SNDR 700 μm^2 Second-Order All-Digital TDC with Low-Jitter Frequency Shift Oscillators and Dynamic Flipflops, T. Konishi, K. Okuno, S. Izumi, M. Yoshimoto, H. Kawaguchi, Kobe University **МФЛ**

22.4 - 4:40 p.m.
A 7b, 3.75ps Resolution Two-Step Time-to-Digital Converter in 65nm CMOS Using Pulse-Train Time Amplifier, K. Kim, Y. Kim, W. Yu, S. Cho, KAIST **МФН**

Session 23 – Tapa II

Power Management Circuits

Friday, June 15, 3:25 p.m.

Chairpersons: H. Bergveld, NXP Semiconductors
H. Nakamoto, Fujitsu Labs, Ltd.

23.1 - 3:25 p.m.

A 0.45-V Input On-Chip Gate Boosted (OGB) Buck Converter in 40-nm CMOS with More Than 90% Efficiency in Load Range from 2µW to 50µW, X. Zhang, P.-H. Chen, Y. Ryu*, K. Ishida, Y. Okuma*, K. Watanabe*, T. Sakurai, M. Takamiya, University of Tokyo, *STARC мфп

23.2 - 3:50 p.m.

A Fully Electrical Startup Batteryless Boost Converter with 50mV Input Voltage for Thermoelectric Energy Harvesting, H.-Y. Tang, P.-S. Weng, P.-C. Ku, L.-H. Lu, National Taiwan University мфс

23.3 - 4:15 p.m.

Integrated All-silicon Thin-film Power Electronics on Flexible Sheets For Ubiquitous Wireless Charging Stations based on Solar-energy Harvesting, L. Huang, W. Rieutort-Louis, Y. Hu, J. Sanz-Robinson, S. Wagner, J.C. Sturm, N. Verma, Princeton University мфу

23.4 - 4:40 p.m.

A 2.98nW Bandgap Voltage Reference Using a Self-Tuning Low Leakage Sample and Hold, Y.-P. Chen, M.Fojtik, D. Blaauw, D. Sylvester, University of Michigan нлл

23.5 - 5:05 p.m.

A 635pW Battery Voltage Supervisory Circuit for Miniature Sensor Nodes, I. Lee, S. Bang, Y. Lee, Y. Kim, G. Kim, D. Sylvester, D. Blaauw, University of Michigan нлн