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2012 IEEE Silicon Nanoelectronics Workshop

Hilton Hawaiian Village, Honolulu, HI USA

June 10-11, 2012

Technical Program

Opening Remarks

Sunday, June 10, 8:30

Tsu-Jae King Liu, *University of California at Berkeley*, General Chair

Session 1: Plenary & Towards Zero Power Electronics

Sunday, June 10, 8:40

Co-chairs: Toshiro Hiramoto, *University of Tokyo* and Thomas Skotnicki, *STMicroelectronics*

- 8:40 1-1 (Plenary Invited) **Innovative thermal energy harvesting for zero power electronics**, S. Monfray¹, O. Pucasu^{1,2}, G. Savelli², U. Soupremanien², E. Ollier², C. Guerin², L.G. Fréchet³, E. Léveillé³, G. Mirshekari³, C. Maitre¹, P. Coronel², K. Domanski⁴, P. Grabiec⁴, P. Ancey¹, D. Guyomar⁵, V. Bottarel⁶, G. Ricotti⁶, F. Boeuf¹, F. Gaillard², and T. Skotnicki¹, ¹*STMicroelectronics, France* ²*CEA Liten, France* ³*Université de Sherbrooke, Canada* ⁴*ITE, Poland*, ⁵*INSA Lyon, France*, ⁶*STMicroelectronics, Italy*
- 9:10 1-2 (Plenary Invited) **New type steep-S device using the bipolar action**, D. Hisamoto, S. Saito, A. Shima, H. Yoshimoto, and K. Torii, *Hitachi, Ltd., Japan*
- 9:40 1-3 **Experimental Demonstration of Temperature Stability of Si-Tunnel FET over Si-MOSFET**, S. Migita, K. Fukuda, Y. Morita, and H. Ota, *AIST, Japan*
- 09:55 1-4 **Scale laws for enhanced power for MEMS based heat energy harvesting**, O. Pucasu^{1,2}, S. Monfray¹, F. Boeuf¹, G. Savelli³, F. Gaillard³, D. Guyomar², T. Skotnicki¹, ¹*STMicroelectronics*, ²*INSA Lyon*, ³*CEA Liten, France*

Session 2: Thermal Management & Nanoscale Memory

Sunday, June 10, 10:30

Co-chairs: Byung-Gook Park, *Seoul National University* and Tsu-Jae King Liu, *UC Berkeley*

- 10:30 2-1 (Invited) **Energy-Efficiency and Thermal Management in Nanoscale Devices**, A.D. Liao, Z.-Y. Ong, A.Y. Serov, F. Xiong, and Eric Pop, *University of Illinois at Urbana-Champaign, USA*
- 11:00 2-2 **Comparative Study of Tri-Gate- and Double-Gate-Type Poly-Si Fin-Channel Split-Gate Flash Memories**, Y.X. Liu¹, T. Kamei², T. Matsukawa¹, K. Endo¹, S. O'uchi¹, J. Tsukada¹, H. Yamauchi¹, Y. Ishikawa¹, T. Hayashida², K. Sakamoto¹, A. Ogura², and M. Masahara^{1,2}, ¹*AIST* ²*Meiji University, Japan*
- 11:15 2-3 **Variation-Aware Study of BJT-based Capacitorless DRAM Cell Scaling Limit**, M.H. Cho, W. Kwon, N. Xu, and T.-J.K. Liu, *University of California at Berkeley, USA*

- 11:30 2-4 **Investigation into the Effect of the Variation of Gate Dimensions on Program Characteristics in 3D NAND Flash Array**, J.Y. Seo, Y. Kim, S.H. Park, W. Kim, D.-B. Kim, J.-H. Lee, H. Shin, and B.-G. Park, *Seoul National University, Korea* ****
- 11:45 2-5 **A novel Gate-All-Around Ultra-Thin p-channel Poly-Si TFT Functioning as Transistor and Flash Memory with Silicon Nanocrystals**, H.-B. Chen¹, S.-H. Lin², J.-J. Wu¹, Y.-C. Wu², and C.-Y. Chang¹, ¹*National Chiao Tung University* ²*National Tsing Hua University, Taiwan ROC* ****

Session 3: Advanced Channel and Gate Stack Materials

Sunday, June 10, 13:30

Co-chairs: Kristin De Meyer, *IMEC* and Dong-Won Kim, *Samsung Electronics*

- 13:30 3-1 (Invited) **Graphene for More Moore and More Than Moore Applications**, M.C. Lemme, S. Vaziri, A.D. Smith, J. Li, S. Rodriguez, A. Rusu, M. Ostling, *KTH Royal Institute of Technology, Sweden* ****
- 14:00 3-2 **High Performance Ω -Gate Ge FinFET Featuring Low Temperature Si₂H₆ Passivation and Implantless Schottky-Barrier NiGe Metallic Source/Drain**, B. Liu¹, X. Gong¹, G. Han¹, P.S.Y. Lim¹, Y. Tong¹, Y. Yang¹, N. Daval², M. Pulido², D. Delprat², B.-Y. Nguyen², and Y.-C. Yeo¹, ¹*National University of Singapore, Singapore* ²*Soitec, France* ****
- 14:15 3-3 **High-performance pMOSFETs with High-k Gate Dielectric and Dislocation-free Epitaxial Si/Ge Super-lattice Channel**, L.-J. Liu¹, K.-S. Chang-Liao¹, C.-H. Fu¹, H.-C. Hsieh¹, C.-C. Lu¹, T.-K. Wang¹, P. Y. Gu², and M.J. Tsai², ¹*National Tsing Hua University*, ²*Industrial Technology Research Institute, Taiwan ROC* ****
- 14:30 3-4 **Counter Dipole Layer Formation in SiO₂/High-k/SiO₂/Si Gate Stacks**, S. Hibino, T. Nishimura, K. Nagashio, K. Kita, and A. Toriumi, *University of Tokyo, Japan* ****
- 14:45 3-5 **Simultaneous Carrier Transport Enhancement and Variability Reduction in Si MOSFETs by Insertion of Partial Monolayers of Oxygen**, R.J. Mears¹, N. Xu², N. Damrongplisit², H. Takeuchi¹, R.J. Stephenson¹, N.W. Cody¹, A. Yiptong¹, X. Huang¹, M. Hytha¹, and T.-J.K. Liu², ¹*Mears Technologies* ²*University of California at Berkeley, USA* ****
- 15:00 3-6 **Transport in Graphene on Boron Nitride**, D.K. Ferry, *Arizona State University, USA* ****

Session 4: Spintronic Devices

Sunday, June 10, 15:35

Chair: Stephen Goodnick, *Arizona State University*

- 15:35 4-1 (Invited) **Magnetic Tunnel Junction for Magnetoresistive Random Access Memory and Beyond**, H. Ohno, *Tohoku University, Japan*
- 16:05 4-2 **Systolic Architectures and Applications for Nanomagnet Logic**, M. Niemier¹, X. Ju², M. Becherer², G. Csaba¹, X.S. Hu¹, D. Schmitt-Landsiedel², P. Lugli², and W. Porod¹, ¹*University of Notre Dame, USA* ²*Technical University of Munich, Germany*
- 16:20 4-3 **Analysis of static noise margin and power-gating efficiency of a new nonvolatile SRAM cell using pseudo-spin-MOSFETs**, Y. Shuto, S. Yamamoto, and S. Sugahara, *Tokyo Institute of Technology, Japan*

Poster Session 1: Advanced Memory and Channel Materials

Sunday, June 10, 16:40 – 19:00

Chair: Yee-Chia Yeo, *National University of Singapore*

16:40 Poster introductions (1 minute each)

Session 5: Emerging Memory Devices

Monday, June 11, 8:30

Co-chairs: Simon Deleonibus, *LETI* and Malgorzata Jurczak, *IMEC*

- 8:30 5-1 (Invited) **Recent Progress of Resistive Switching Random Access Memory (RRAM)**, Y. Wu, S. Yu, X. Guan, and H.-S.P. Wong, *Stanford University, USA*
- 9:00 5-2 **Bidirectional Selection Device Characteristics of Ultra-Thin (<3nm) TiO₂ layer for 3D Vertically Stackable ReRAM Application**, J. Woo¹, J. Park², J. Shin², G. Choi¹, S. Kim², W. Lee², S. Park², D. Lee¹, E. Cha², and H. Hwang¹, Pohang¹*University of Science and Technology* ²*Gwangju Institute of Science and Technology, Republic of Korea*
- 9:15 5-3 **Co-existed Unipolar and Bipolar Resistive Switching Effect of HfOx-Based RRAM**, B. Chen, B. Gao, Y.H. Fu, R. Liu, L. Ma, P. Huang, F.F. Zhang, L.F. Liu, X.Y. Liu, J.F. Kang, and G.J. Lian, *Peking University, China*
- 9:30 5-4 **4kb nonvolatile nanogap memory (NGpM) with 1 ns programming capability**, T. Takahashi¹, S. Furuta¹, Y. Masuda¹, S. Kumaragurubaran¹, T. Sumiya¹, M. Ono¹, Y. Hayashi², T. Shimizu³, H. Suga³, M. Horikawa³, and Y. Naitoh³, ¹*Funai Electric Advanced Applied Technology Research Institute* ²*Tsukuba Device Solution Center* ³*AIST, Japan*
- 9:45 5-5 **Characteristics of Metal/Ferroelectric (PVDF-TrFE)/Graphene (MFG) Device**, H.J. Hwang, E.J. Paek, J.H. Yang, C.G. Kang, and B.H. Lee, *Gwangju Institute of Science and Technology, Korea*

Session 6: Single Electron Devices & Quantum Transport

Monday, June 11, 10:20

Co-chairs: Michiharu Tabe, *Shizuoka University* and Wolfgang Porod, *Notre Dame University*

- 10:20 6-1 (Invited) **Silicon Single-Electron Transfer Devices: Ultimate Control of Electric Charge**, A. Fujiwara, G. Yamahata, K. Nishiguchi, G.P. Lansbergen, and Y. Ono, *NTT Corporation, Japan*
- 10:50 6-2 **Reinvestigation of Dot Formation Mechanisms in Silicon Nanowire Channel Single-Electron/Hole Transistors Operating at Room Temperature**, R. Suzuki, M. Nozue, T. Saraya, and T. Hiramoto, *University of Tokyo, Japan* ...
- 11:05 6-3 **Quantum Transport Property in FETs with Deterministically Implanted Single-Arsenic Ions Using Single-ion Implantation**, M. Hori¹, T. Shinada¹, F. Guagliardo², G. Ferrari², and E. Prati³, ¹Waseda University, Japan ²Politecnico di Milano, ³CNR-IMM, Italy
- 11:20 6-4 **High-frequency properties of Si single-electron transistor**, H. Takenaka¹, M. Shinohara¹, T. Uchida¹, M. Arita¹, A. Fujiwara², Y. Ono², K. Nishiguchi², H. Inokawa³, and Y. Takahashi¹, ¹Hokkaido University ²NTT Corporation ³Shizuoka University, Japan
- 11:35 6-5 **Negative Differential Resistance Devices with Ultra-High Peak-to-Valley Current Ratio Based on Silicon Nanowire Structure**, S. Shin, M.W. Ryu, and K.R. Kim, *Ulsan National Institute of Science and Technology, Korea*
- 11:50 6-6 **Mapping of single donors in nano-scale MOSFETs at low temperature**, J. Verduijn^{1,2}, G.C. Tettamanzi¹, R. Wacquez³, B. Roche³, B. Voisin³, X. Jehl³, M. Sanquer³, S. Rogge^{1,2}, ¹University of New South Wales, Australia ²Delft University of Technology, The Netherlands ³CEA-LETI, France

Session 7: Nanoscale Phenomena

Monday, June 11, 13:30

Co-chairs: Kazuhiko Endo, *AIST* and Yukinori Ono, *University of Toyama*

- 13:30 7-1 (Invited) **A Single Atom Transistor**, M.Y. Simmons, *University of New South Wales, Australia*
- 14:00 7-2 **Statistical Variability Study of a 10nm Gate Length SOI FinFET Device**, B. Cheng¹, A.R. Brown², X. Wang¹, and A. Asenov^{1,2}, ¹University of Glasgow ²Gold Standard Simulations, United Kingdom
- 14:15 7-3 **Reduced Drain Current Variability in Fully Depleted Silicon-on-Thin-BOX (SOTB) MOSFETs**, T. Mizutani¹, Y. Yamamoto², H. Makiyama², T. Tsunomura², T. Iwamatsu², H. Oda², N. Sugii², and T. Hiramoto¹, ¹University of Tokyo ²Low-power Electronics Association & Project, Japan
- 14:30 7-4 **The Impact of the Carrier Transport on the Random Dopant Induced Drain Current Variation in the Saturation Regime of Advanced Strained-Silicon CMOS Devices**, E.R. Hsieh¹, S.S. Chung¹, C.H. Tsai², R.M. Huang², C.T. Tsai², and C.W. Liang², ¹National Chiao Tung University ²United Microelectronics Corporation, Taiwan ROC

- 14:45 **7-5 On the Statistical Trap-Response (STR) Method for Characterizing Random Trap Occupancy and NBTI Fluctuation**, J. Zou¹, C. Liu¹, R. Wang¹, X. Xu¹, J. Liu², H. Wu², Y. Wang¹, R. Huang¹, ¹*Peking University* ²*Semiconductor Manufacturing International Corporation, China*
- 15:00 **7-6 Statistical distribution of RTS amplitudes in 20nm SOI FinFETs**, X. Wang¹, A.R. Brown², B. Cheng¹, and A. Asenov^{1,2}, ¹*University of Glasgow* ²*Gold Standard Simulations, United Kingdom*

Poster Session 2: Nanoscale/Quantum Devices and Phenomena

Monday, June 11, 15:20 – 17:30

Chair: Thomas Skotnicki, *STMicroelectronics*

15:20 **Poster introductions** (1 minute each)

Poster Session 1: Advanced Memory and Channel Materials

Sunday, June 10, 16:40 – 19:00

- P1-1 Self-Improvement of Cell Stability in SRAM by Post Fabrication Technique**, A. Kumar, T. Saraya, S. Miyano, and T. Hiramoto, *University of Tokyo, Japan*
- P1-2 Improving the Endurance of Floating Gate NAND Flash Cells with Junction-Free Structure**, I. Joo^{1,2}, S. Hur¹, C. Lee¹, S. Lee¹, H. Park¹, J. Song¹, H. Lee¹, Y. Jun¹, and I. Chung², ¹*Samsung Electronics* ²*SungKyunKwan University, Korea*
- P1-3 Low Standby Power Charge Trap Flash Memory with Tunneling Field Effect Transistor**, M.S. Han¹, J.H. Lee², D. Seo¹, C.-D. Park¹, Y. Oh¹, and I.H. Cho¹, ¹*Myongji University*, ²*Seoul National University, Korea*
- P1-4 Charge-trap flash memory devices fabricated with nano-scale patterns on the Si₃H₄ trapping layer**, H.-M. An¹, K.H. Kim¹, H.-D. Kim¹, W.-J. Cho², and T.G. Kim¹, ¹*Korea University*, ²*Kwangwoon University, Korea*
- P1-5 Simulation of Charge Trapping Memory with Silicon Nanocrystals Embedded in Silicon Nitride Layer**, Y. Peng, X. Liu, G. Du, Y. Yang, and J. Kang, *Peking University, China*
- P1-6 Nanodot-type Floating Gate Memory with High-density Nanodot Array Formed Utilizing *Listeria Dps***, H. Kamitake¹, K. Ohara¹, M. Uenuma¹, B. Zheng¹, Y. Ishikawa¹, I. Yamashita^{1,2}, and Y. Uraoka¹, ¹*Nara Institute of Science and Technology* ²*Panasonic Corporation, Japan*
- P1-7 Impacts of Silicon Nanocrystal Incorporation on the Transfer Characteristics of Poly-Silicon nanowire SONOS Devices**, K.-H. Lee, H.-C. Lin, and T.-Y. Huang, *National Chiao Tung University, Taiwan ROC*
- P1-8 3-D Stacked NAND Flash Memory Having Lateral Bit-Line Layers and Vertical Gate**, J.-W. Lee, M.-K. Jeong, B.-G. Park, H. Shin and J.-H. Lee, *Seoul National University, Korea*

- P1-9 Effect of Cu Insertion Layer between Top Electrode and Switching Layer on Resistive Switching Characteristics**, S. Jung, J.-H. Oh, K.-C. Ryoo, S. Kim, J.-H. Lee, H. Shin, and B.-G. Park, *Seoul National University, Korea*
- P1-10 Self-compliance Unipolar Resistive Switching and Mechanism of Cu/SiO₂/TiN RRAM Devices**, D. Yu, L.F. Liu, P. Huang, F.F. Zhang, B. Chen, B. Gao, Y. Hou, D.D. Han, Y. Wang, J.F. Kang, and X. Zhang, *Peking University, China*
- P1-11 Stable Resistive Switching Characteristics Observed in SiN-based Resistive Switching Memory Devices by using RF-sputtering methods**, H.-D. Kim, S.M. Hong, H.-M. An, K.H. Kim, Y. Seo, M. Song, D. Li, and T.G. Kim, *Korea University, Korea*
- P1-12 Rectifying Characteristics and Implementation of n-Si/HfO₂ based Devices for 1D1R-based Cross-Bar Memory Array**, F. F. Zhang, P. Huang, B. Chen, D. Yu, Y.H. Fu, L. Ma, B. Gao, L.F. Liu, X.Y. Liu, and J.F. Kang, *Peking University, China*
- P1-13 Oxygen-induced High-*k* Degradation in TiN/HfSiO Gate Stacks**, T. Hosoi, Y. Odake, K. Chikaraishi, H. Arimura, N. Kitano, T. Shimura, and H. Watanabe, *Osaka University, Japan*
- P1-14 Metal/Ge Schottky Barrier Modulation With C-Containing Layer by Chemical Bath**, W. Wang, J. Wang, M. Zhao, R. Liang, and J. Xu, *Tsinghua University, China*
- P1-15 Orientation and Size Effects on Ballistic Electron Transport Properties in Gate-All-Around Rectangular Germanium Nanowire FETs**, S. Mori, N. Morioka, J. Suda, and T. Kimoto, *Kyoto University, Japan*
- P1-16 Quantum Transport Simulation of III-V MOSFETs based on Wigner Monte Carlo Approach**, Y. Maegawa, S. Koba, H. Tsuchiya, and M. Ogawa, *Kobe University, Japan*
- P1-17 Mechanisms of Ambient Dependent Mobility Degradation in the Graphene MOSFETs on SiO₂ Substrate**, Y.G. Lee, C.G. Kang, C. Cho, Y.H. Kim, H.J. Hwang, J.J. Kim, U.J. Jung, E. J. Park, M.W. Kim, and B.H. Lee, *Gwangju Institute of Science and Technology, Korea*
- P1-18 Electronic Band Structures of Graphene Nanomeshes**, R. Sako, N. Hasegawa, H. Tsuchiya, and M. Ogawa, *Kobe University, Japan*
- P1-19 Band Structure and Electron Transport in Multi-Junction Graphene Nanoribbons**, N. Hasegawa, R. Sako, H. Tsuchiya, and M. Ogawa, *Kobe University, Japan*
- P1-20 Graphene-Diamond-Silicon Devices with Increased Current-Carrying Capacity: sp²-Carbon-sp³-Carbon-on-Silicon Technology**, J. Yu¹, G. Liu¹, A.V. Sumant², and A. A. Balandin¹, ¹University of California at Riverside, ¹Argonne National Laboratory, USA
- P1-21 Selective Gas Sensing with a Single Graphene-on-Silicon Transistor**, A.A. Balandin¹, S. Romyantsev², G. Liu¹, M.S. Shur², and R.A. Potyrailo³, ¹University of California at Riverside ²Rensselaer Polytechnic Institute, ³GE Global Research, USA
- P1-22 Graphene Fillers for Ultra-Efficient Thermal Interface Materials**, K.M.F. Shahil, V. Goyal, R. Gulotty, and A.A. Balandin, *University of California at Riverside, USA*
- P1-23 Silicon Microfabrication Technologies for THz applications**, C. Jung-Kubiak, J. Gill, T. Reck, C. Lee, J. Siles, G. Chattopadhyay, R. Lin, K. Cooper and I. Mehdi, *Jet Propulsion Laboratory, California of Technology*

Poster Session 2: Nanoscale/Quantum Devices and Phenomena

Monday, June 11, 15:20 – 17:30

- P2-1 Simulation Study on Process Conditions for High-Speed Silicon Photodetector and Quantum-Well Structuring for Increased Number of Wavelength Discriminations**, S. Cho¹, H. Kim², M.-C. Sun², T.I. Kamins¹, B.-G. Park², and J.S. Harris, Jr.¹, *Stanford University, USA* ²*Seoul National University, Korea* ****
- P2-2 Nano-Transfer Printing of Functioning MIM Tunnel Diodes**, Mario Bareiß¹, B. Weiler¹, D. Kälblein², U. Zschieschang², H. Klauk², G. Scarpa¹, B. Fabel¹, P. Lugli¹, and W. Porod³, ¹*Technische Universität München, Germany* ²*Max Planck Institute for Solid State Research, Germany* ³*University of Notre Dame, USA* ****
- P2-3 Fabrication and evaluation of heavily P-doped Si quantum dot and back-gate induced Si quantum dot**, J. Kamioka¹, T. Kodera^{1,2}, K. Horibe¹, Y. Kawano¹, and S. Oda¹, ¹*Tokyo Institute of Technology* ³*University of Tokyo Japan* ****
- P2-4 Microwave manipulation of electrons in silicon quantum dots**, T. Ferrus¹, A. Rossi¹, T. Kodera^{2,3}, T. Kambara², W. Lin², S. Oda², and D.A. Williams¹, ¹*Hitachi Cambridge Laboratory, United Kingdom* ²*Tokyo Institute of Technology* ³*University of Tokyo Japan* ****
- P2-5 Charge sensing of a Si triple quantum dot system using single electron transistors**, R. Mizokuchi, T. Kodera, K. Horibe, Y. Kawano, and S. Oda, *Tokyo Institute of Technology, Japan* ****
- P2-6 Fabrication and characterization of Si/SiGe quantum dots with capping gate**, T. Kodera^{1,2}, Y. Fukuoka¹, K. Takeda², T. Obata², K. Yoshida², K. Sawano³, K. Uchida¹, Y. Shiraki³, S. Tarucha², and S. Oda¹, *Tokyo Institute of Technology* ²*University of Tokyo* ³*Tokyo City University, Japan* ****
- P2-7 Single Ge quantum dot placement along with self-aligned electrodes for effective management of single electron tunneling**, I. H. Chen, K. H. Chen, and P. W. Li, *National Central University, Taiwan ROC* ****
- P2-8 Single-electron transport through a single donor at elevated temperatures**, E. Hamid, D. Moraru, T. Mizuno and M. Tabe, *Shizuoka University, Japan* ****
- P2-9 The Interplay of Self-Heating Effects and Static RTF in Nanowire Transistors**, D. Vasileska, A. Hossain, and S.M. Goodnick, *Arizona State University, USA* ****
- P2-10 Effect of Interfacial States on the technological variability of Trigate MOSFETs**, E. González-Marín, F.G. Ruiz, A. Godoy, I.M. Tienda-Luna, F. Gámiz, *Universidad de Granada, Spain* ****
- P2-11 Evolution of Channel Trap Distribution under Bias Stress in Polysilicon Thin Film Transistors evaluated by Charge Pumping Method**, C.N. Manh¹, J.S. Chang¹, T.-Y. Jang¹, M. Hasan¹, H. Yang¹, J.K. Jeong¹, B. Kim², J. Ahn², K. Hwang², and R. Choi¹, ¹*Inha University* ²*Samsung Electronics Co., Ltd., Korea* ****
- P2-12 Physical Model for Random Telegraph Noise Amplitudes and Implications**, R.G. Southwick III¹, K.P. Cheung¹, J.P. Campbell¹, S.A. Drozdov², J.T. Ryan¹, J.S. Suehle¹, and A.S. Oates³, ¹*National Institute of Standards and Technology*, ²*University of Maryland USA* ³*Taiwan Semiconductor Manufacturing Company Ltd., Taiwan ROC* ****

- P2-13 Optoelectrical Lifetime Evaluation of Single Holes in SOI MOSFET**, W. Du¹, D.S. Putranto^{1,2}, H. Satoh¹, A. Ono¹, P.S. Priambodo², D. Hartanto², and H. Inokawa¹
¹Shizuoka University, Japan ²University of Indonesia, Indonesia
- P2-14 *Ab initio* analysis of donor state deepening in Si nano-channels**, D. Moraru¹, Y. Kuzuya¹, E. Hamid¹, T. Mizuno¹, M. Tabe¹, and H. Mizuta², ¹Shizuoka University, Japan ²University of Southampton, United Kingdom
- P2-15 Channel Length-Dependent Series Resistance?**, J.P. Campbell¹, K.P. Cheung¹, S.A. Drozdov², R.G. Southwick¹, J.T. Ryan¹, A.S. Oates³, J.S. Suehle¹, ¹National Institute of Standards and Technology, ²University of Maryland USA ³Taiwan Semiconductor Manufacturing Company Ltd., Taiwan ROC
- P2-16 Effects of Amorphous Silicon Atomic Density Variation on Series and Contact Resistances in Nanoscale Thin-Film Structures**, M.W. Ryu, S.-H. Kim, and K.R. Kim, Ulsan National Institute of Science and Technology, Korea
- P2-17 Evaluation of Scattering in Asymmetric Quasi-Ballistic DG-MOSFET**, G. Liu, G. Du, T. Lu, X. Liu, P. Zhang, and X. Zhang, Peking University, China
- Fabrication and Characterization of a Pi-Gate Ultrathin Body Junctionless poly-Si TFTs**
J. Wu, H. Chen, M. Han, Y. Wu, C. Chang
- P2-18 Orientational and Si-SiO₂ roughness topology dependence of electron mobilities in silicon gate-all-around nanowire FETs**, M. Bescond and E. Dib, Technologies Château-Gombert, France
- P2-19 Junctionless poly-Si TFTs**, J.-J. Wu¹, H.-B. Chen¹, M.-H. Han¹, Y.-C. Wu², and C.-Y. Chang¹, ¹National Chiao Tung University ²National Tsing Hua University, Taiwan ROC
- P2-20 Quantum Drift-Diffusion and Quantum Energy Balance Simulation of Nanowire Junctionless Transistors**, O. Badami, N. Kumar, D. Saha, and S. Ganguly, Indian Institute of Technology Bombay, India
- P2-21 Characteristics and Sensitivity of p-Type Junctionless Gate-All-Around Nanowire Transistor**, M.-H. Han¹, Y.-R. Jhan², J.-J. Wu¹, H.-B. Chen¹, Y.-C. Wu², and C.-Y. Chang¹, ¹National Chiao Tung University ²National Tsing Hua University, Taiwan ROC
- P2-22 Analysis of Hysteresis Characteristics of Fabricated SiNW Biosensor in Aqueous Environment with Reference Electrode**, J.H. Lee¹, J. Lee², M.-C. Sun¹, W.H. Lee², M. Uhm², S. Hwang², I.-Y. Chung³, D.M. Kim², D.H. Kim², and B.-G. Park¹, ¹Seoul National University ³Kookmin University ³Kwangwoon University, Korea
- P2-23 Investigation on Hump Effects of L-shaped Tunneling Field-Effect Transistors**, S.W. Kim¹, W.Y. Choi², H. Kim¹, M.-C. Sun^{1,3}, H. W. Kim¹, and B.-G. Park¹, ¹Seoul National University ²Sogang University ³Samsung Electronics Co., Ltd., Korea
- P2-24 Device Structure for the Characterization of Nanowire Thermocouples**, G.P. Szakmany, P.M. Krenz, A.O. Orlov, G.H. Bernstein, and W. Porod, University of Notre Dame, USA