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TABLE OF CONTENTS

Session A1L-A: Analog Circuits I

Chair: Mohamad Sawan, *Polytechnique Montréal, Canada*
Time: Monday, August 6, 2012, 10:10 – 11:50
Location: White Water

[Abstract] This paper introduces a flash analog-to-digital converter with high power efficiency. Traditional voltage comparator is replaced by a novel comparison scheme in time domain: analog signal is converted by pulse width modulation block; trigger makes decision by comparing the modulated pulse width. Prototype circuit is designed in a 65-nm logic CMOS technology, achieving a sampling rate of 125-MS/s and an effective number of bits of 4.72. The power consumption is 367-µW under the power supply of 1-V; therefore Figure of Merit at 111-fJ/conversion step is realized.

[Abstract] The paper presents the design of a 2.488 – 11.2 Gbps SerDes transceiver in a 40nm low-leakage CMOS process. The paper explores the architectural and circuit techniques used to meet the stringent requirements of the high-speed SerDes and to mitigate the performance impact of the low-leakage process. The transceiver makes use of a low jitter LC PLL to enable high-reliability system design. A system modeling approach is also described, which is used for optimizing the architectural trade-offs. The design has 520fs RJrms and consumes 30.1 mW/Gbps at 11.2 Gbps.

[Abstract] Geometric programming is a method used to produce globally optimal circuit parameters with high computational efficiency. This method is applied to short channel (180 nm) CMOS Low Noise Amplifiers (LNAs) with common source inductive degeneration to obtain optimal design parameters for minimizing the noise figure. Geometric programming (GP) compatible functions have been determined to calculate the noise figure of short channel CMOS devices by taking into consideration channel length modulation and velocity saturation effects. Optimal design parameters (i.e., channel width and noise figure) from GP optimization are validated by comparing them with simulations obtained from Agilent's Advanced Design Systems (ADS) software. Furthermore, tradeoff analyses have been performed to examine the influence of various design parameters such as quality factor and drain current on the design optimization. With the continuous downscaling of CMOS technologies, GP optimization offers high performance advantages in the optimal design of short channel CMOS LNAs.

[Abstract] Advanced CMOS technologies have demonstrated the reduced device dimensions can significantly increase the circuit sensitivity to transient radiation effects. This paper presents a radiation-tolerant ring oscillator Phase-Locked Loop (PLL) designed in a commercial 0.13 CMOS process. The PLL is designed for radiation-tolerant high-speed serial link applications. It operates over a frequency range of 1.1 GHz to 4.4 GHz with a RMS jitter of less than 2 ps. The phase frequency detector (PFD) and frequency divider are designed with a novel D-flip-clop (DFF) that is robust to single event radiation effects (SEEs). The voltage-controlled oscillator (VCO) is designed with two ring oscillators cross-coupled thus compensating each other with the radiation-induced transient currents. The PLL utilizes two independent charge pumps and loop filters to provide the control voltages for the two ring VCOs, respectively. Simulation results show that the proposed PLL demonstrates radiation immunity for critical charge values up to 250 fC and can recover quickly from radiation strikes on its sensitive nodes. The PLL operates under a 1.2 V power supply and consumes 40 mW of power.

[Abstract] This paper presents a programmable ultra-low frequency ring oscillator designed in a 0.5µm CMOS technology with 3.3V power supply. The oscillator tracks and memorizes the input reference frequency using a phase-locked loop (PLL) architecture. The PLL controls an on-chip nonvolatile memory using a floating-gate structure; the voltage on the floating-gate node is applied to the voltage-controlled oscillator (VCO) to generate the desired frequency. A high-voltage NMOS (breakdown voltage close to 40V) is introduced to realize the floating gate control. Transient simulations indicate that the circuit successfully tracks a desired frequency with maximum period jitter of 0.88% at the system output.

Session A1L-B: Digital Circuits I

Chair: Abhilash Goyal
Co-Chair: Pramod Meher
Time: Monday, August 6, 2012, 10:10 – 11:50
Location: Rapids

[Abstract] In this paper, new low-power and low-leakage domino circuit topologies are proposed using asymmetrically-doped FinFET devices. Asymmetric source/drain doping results in unequal currents for positive and negative drain-to-source voltages (VDS). Using the proposed device, leakage current reduces significantly while the performance is improved. The proposed device shows 10 times reduction in leakage current while other characteristics such as DIBL and SS are ameliorated. To show the efficacy of the proposed device, asymmetric FinFET is used to design several circuits such as high fan-in gates. Furthermore, it will be illustrated how to design a datapath using proposed device that results in improved robustness and power consumption.

[Abstract] Due to continuous technology scaling, the nodal capacitances reduction and power supply voltage lowering result in an ever decreasing minimal charge capable of upsetting the logic state of memory circuits. CMOS circuits operating under sub-threshold voltage region are more susceptible than ever to externally induced radiation that is likely to bring about the occurrence of soft errors. In this paper, a novel radiation hardened latch is presented for high performance sub-threshold voltage operation. The critical charge is increased five times than that of the conventional latch with only 10% of area increment including 46% of power reduction.

[Abstract] NAND multi-level cell (MLC) flash memories are widely used due to low cost and high capacity. However the increased number of levels in MLC results in larger interference and errors. The errors in MLC flash memories tend to be asymmetric and with limited-magnitude. To take advantage of the characteristics, we propose limited-magnitude parity check codes, which can reduce errors more effectively. A key advantage of the proposed method is that it has low complexity for encoding and decoding. Another useful feature of the proposed method is that the code rate and the block size can be chosen almost continuously unlike conventional error correcting codes.

[Abstract] This work is motivated to improve low voltage-operated 6T-SRAM cell yield by using an exponentially decayed boosted WL signal. The proposed scheme takes advantage of the DNM concept to improve the 6T cell yield and performance without the need to increase the cell area. A leakage current reduction benefit is added by optimizing the cell's access transistor channel length with the boost scheme without compromising the cell current. In low voltage regime, the boost WL signal peak and duration can be controlled to avoid read failures. A 4k bit SRAM sub-array of the conventional 6T SRAM cell is used as a Circuit Under Test (CUT) to investigate the effectiveness of the proposed scheme.

Session A1L-D: RF and Microwave Systems

Chair: Jim Browning, *Boise State University*
Time: Monday, August 6, 2012, 10:10 – 11:50
Location: Clear Water

[Abstract] Monolithic optoelectronic integrated circuits are a primary focus of research for high-speed optical communication system development. Standard silicon processes provide a cost effective way for electro-optic system integration. This paper presents a monolithic optical modulator and driver design based on 130nm SiGe BiCMOS technology. Post-layout simulation results demonstrate that the modulator achieves a switch frequency of 10GHz.

[Abstract] A creative method to reduce the voltage head room requirement in the design of double balanced mixer is introduced. Design of a novel high gain, low noise figure and low power CMOS mixer with fully integrated ESD protection is presented. The mixer was implemented in ST 90nm CMOS technology and was packed in a QFN package. With an operating frequency of 1.575 GHz this mixer was targeted for GPS front-end receiver application.

[Abstract] This paper presents a Class-D stage with 3rd harmonic suppression operating at 2VDD (i.e., twice the nominal supply voltage). A DLL-based phase generator is used to generate the phases of the driving signals and by modifying the driver stage 5th harmonic suppression is also possible. The output stage and drivers are based on inverters only, where the short-circuit current is eliminated in the output stage. Operating at 1 GHz, the simulated output power is +19.4 dBm utilizing a 1-V supply and a 5-Ω load, with Drain Efficiency (DE) and Power-Added Efficiency (PAE) of 72% and 52%, respectively, including power dissipation in the DLL-based phase generator and drivers. The 3rd harmonic is suppressed 23 dB (-33 dBc) compared to a conventional Class-D stage.

[Abstract] The demand for wireless-powered circuits are increasing rapidly, RFID and WSN are good examples. One of the most important components is the on-chip voltage rectifier. Research has been conducted intensively on the rectifier design, however not many of them considered the co-design with antennas and matching networks. This paper intends to fill this gap. An analysis on the co-design is presented. A new look-up table design methodology is proposed and simulations are done using Cadence to prove the methodology.

Session A1L-E: Invited Session I

Chair: Jose M. de la Rosa, *Institute of Microelectronics of Seville, IMSE-CNM (CSIC/Univ. of Seville), Spain*
Time: Monday, August 6, 2012, 10:10 – 11:50
Location: River Fork

[Abstract] This paper exposes a number of analog and digital techniques for performance enhancement of Doherty power amplifiers (PAs). After briefly introducing the operation principle of the Doherty PA, the gain and phase impairments between the main and auxiliary amplifiers as well as the problem of power drive waste into the auxiliary branch at the low power mode are analyzed. Due to the dynamic nature of these problems, analog-based approaches cannot completely compensate for them. The digital Doherty PA architecture is then pointed out as the most suitable topology that enables an optimal operation of the Doherty PA. This architecture allows for the implementation of advanced digital signal processing algorithms, such as adaptive input power distribution and dynamic phase alignment that are experimentally proven to bring substantial performance enhancement.

Session A1L-M: Neuromorphic Systems

Chair: Drago Strle
Time: Monday, August 6, 2012, 10:10 – 11:50
Location: Suite 214

[Abstract] Autonomic oscillatory activities exist in almost every living thing and most of them are produced by rhythmic activities of the corresponding neural. This paper proposes a neural oscillator based on the control of a Schmitt Trigger. The oscillator implements 3 neuron cells and 4 synapse circuits, and integrates them into a compact neural network with a source neuron driving two oscillating cells, which inhibit each other. The proposed neural oscillator, with tunable duty cycle and frequency, is simulated in Pspice 16 using 1.2um CMOS process

[Abstract] The Cellular Neural/Nonlinear Network (CNN) paradigm has recently led to a Bio-inspired (Bi-i) Cellular Vision system, which represents a computing platform consisting of sensing, array sensing-processing and digital signal processing. This paper illustrates the implementation of a novel CNN-based segmentation algorithm onto the Bi-i system. The experimental results, carried out for a benchmark video sequence, show the feasibility of the approach, which provides a frame rate of about 26 frame/sec. Finally, comparisons with existing CNN-based methods highlight that the proposed implementation represents a good trade-off between real-time requirements and accuracy.

[Abstract] Jump-resonance is a phenomenon observed in non-linear circuits where the output exhibits abrupt jumps when the frequency of the input signal is varied. Although past circuit designs have attempted to avoid this non-linear phenomenon, we propose to exploit the jump-resonance based hysteresis, observed in silicon cochlea, for encoding frequency and specifically formant trajectories in speech signals. Using experimental prototypes fabricated in a 0.5µm CMOS process, we show that the features extracted from a jump-resonance based silicon cochlea are more discriminative for speech based biometrics as compared to features extracted from a conventional silicon cochlea.

[Abstract] Detecting moving objects in a moving background or a dynamic scene is essential to the survival of some animals. The circuitry computing differential motion is found in the biological retina. An object-motion-sensitivity (OMS) ganglion cell remains silent under global motion of the entire image but fires when the image patch in its receptive field moves differently from the background. In this paper, we present a neuromorphic circuit that compares the motion speeds of the central receptive field and peripheral receptive field. We demonstrate that there is a response if motion speeds of the central and peripheral receptive fields are different. However, the response is suppressed if motion speeds of central and peripheral receptive fields are the same.

Session A2L-A: Analog Circuits II

Chair: Vishal Saxena, *Boise State University*
Time: Monday, August 6, 2012, 13:10 – 14:50
Location: White Water

[Abstract] A fourth-order Butterworth OTA-C lowpass filter based on voltage mode multiple loop feedback (MLF) inverse follow the leader feedback (IFLF) structure is implemented to support both MB-OFDM UWB and low data rate IR-UWB applications. The filter is implemented using a fully-differential linear operational transconductance amplifier (OTA) in 0.25um SOI CMOS. A positive feedback topology is forms a negative resistance load to enhance the OTA DC gain. Simultaneously, the linearity is increased by active biasing. Simulations including parasitics with a 2.5 V power supply show that the cut-off frequency of the filter ranges from 120MHz to 280 MHz and dynamic range are approximately 54 dB. The total power consumption is only 32 mW at the 250 MHz cut-off frequency.

[Abstract] This work shows how balanced transconductor-C low-pass ladder filters using a different arrangement of the transconductors to reduce distortion can also have stable common-mode natural frequencies, not requiring common-mode stabilization circuits. Simulated distortion results are presented, interesting sensitivity properties of these filters are discussed, and some limitations of the technique are mentioned.

[Abstract] This paper presents a successive approximation analog to digital converter with a configurable resolution of 8 or 11 bit. The resolutions are achieved by combining an 8 bit split capacitor array with a 3 bit resistive ladder allowing for a simpler layout and good power efficiency. Configurable buffers are included and enable a wide range of operation frequencies. Sample rates between 300S/s and 80kS/s were tested where at the lower frequency a total current consumption of just 8.4nA was measured. A configurable time domain comparator is employed to adapt the noise requirement to the desired resolution. The circuit is developed in a 130nm CMOS technology and occupies an active area of 0.0664mm2.

[Abstract] A new low voltage FGMOS OTA is proposed that can achieve high transconductance efficiency and offers flexibility in tuning that is suitable for gm-C ladder filters. OTAs with higher transconductance efficiency contribute to higher filter dynamic range for a given power consumption. Schematic simulations show efficiencies of up to 50 for a minimum DR of 63dB was achieved in an AMS 0.35um CMOS process with a supply voltage of 1.8V and power consumption of 56uW.

[Abstract] New techniques for Class-AB Operational Trans-conductance Amplifiers (OTAs) are presented. These new techniques are two topologies based on current boosting in class-AB stage which achieve considerable improvement of Slew Rate and Gain-Bandwidth while maintaining the same power consumption as the conventional design. Circuit level analysis and simulation results of proposed circuits in 0.18µm CMOS technology for gain, GBW, slew rate, and settling time are presented to prove the effectiveness of the proposed design method.

Session A2L-B: Digital Circuits II

Chair: Pramod Meher
Co-Chair: Abhilash Goyal
Time: Monday, August 6, 2012, 13:10 – 14:50
Location: Rapids

[Abstract] This paper describes a 16-bit Logarithmic Signal Processor and its implementation using Clocked Adiabatic Logic(CAL). The proposed architectures for Lin2Log and Log2Lin converters are based on a linear interpolation algorithm. The CAL-Logarithmic Signal Processor has been designed using an AMS 0.35um CMOS process and consumes an area of 7.3mm2. Spice simulations have shown that the circuit can operate at frequencies up to 250MHz and energy calculation have indicated 211.34 pJ power consumption at the maximum operating frequency.

[Abstract] To date, various optically reconfigurable gate arrays (ORGAs) have been developed to realize both fast reconfiguration and numerous reconfiguration contexts. Optically differential reconfigurable gate arrays (ODRGAs) present the advantageous capabilities compared with ORGAs: they have increased reconfiguration frequency per unit of laser power and reduced optical power consumption. Dynamic optically reconfigurable gate arrays (DORGA) can realize the highest gate density, but an important disadvantage of DORGAs is that their reconfiguration frequency is lower than that of ODRGAs and their optical power consumption is greater than that of ODRGAs. Therefore, a novel inversion/non-inversion dynamic optically reconfigurable gate array that adopts only the good factors from both architectures has been developed. This paper presents an inversion/non-inversion implementation for a newly fabricated 0.18 µm CMOS process optically reconfigurable gate array VLSI. Based on that implementation, three factors are discussed: gate density, reconfiguration frequency per unit of laser power, and optical power consumption.

[Abstract] Organic electronics have immense potential over a wide spectrum of applications. In the present scenario, an abundance of investigations are being followed on the transistor operation and its characterization. However, circuit level research focus is not that common. Therefore, we sensed the urgency to provide a complete assessment of the different circuit styles, which are, the diode-load, zero-Vgs, pseudo-E and pseudo-D, in ratioless and ratioed logic. A comparative evaluation of the collective circuit behavior of each design style is critical. The major parameters, such as, power consumption, noise margin of high and low level signal, circuit speed, on current and output voltage swing were measured and thereupon, analyzed to decide upon the optimum circuit style for cascading. The inverter, NAND and NOR logic gates, and a 5-inverter ring oscillator were further analyzed, using the pentacene OTFT model file, to realize the best architecture for integration in large scale circuits.

[Abstract] For a low-power sensor system, a hybrid Instruction Set Architecture (ISA) maintains the advantages of a 16-bit datapath while increasing the address space from 65 KB to 2 MB by using 24 address bits. Measured data from fabricated chips can indicate the energy used for specific operations by comparing similar instructions. This measured data indicates that the large address space is achieved with only a 2.5% increase in area, 3% increase in leakage, and a similarly small percent increase in active power. The ISA includes sixteen 24-bit registers and a unique combination of addressing modes to enable compact code.

Session A2L-D: RF and Optical/Photonic Systems

Chair: Roghoyeh Salmeh, *ATCO Electric*
Co-Chair: Robert Hay, *Boise State University*
Time: Monday, August 6, 2012, 13:10 – 14:50
Location: Clear Water

[Abstract] In this paper a novel microwave bandpass filter (BPF) with extended out-of-band rejection is presented. The filter is based on a novel reduced size microstrip resonator which consists of two parallel lines in combination with a shortcircuited stub. A BPF at 1.85 GHz with 11.11% fractional bandwidth (FBW) is designed, simulated and fabricated. Excellent agreements between simulated and experimental results were obtained. The electrical characteristic of this fabricated BPF allows its use in a microwave photonic filter demonstrating in this way a practical application.

[Abstract] Avalanche photodetectors have been fabricated in ON Semiconductor's C5 process without any special process or fabrication steps. The electrical and optical characteristics of APDs, with varying active area and guard ring configurations, are reported in this paper. Also reported are the details and considerations that went into laying out the APDs. It was found that substrate current was negligible and nearly independent of the geometrical shape of the substrate tie-downs around the perimeter of the APD structures. The measured APD breakdown is approximately 14 V. The devices show optical gains in excess of 1,000 at photocurrents of 10 uA.

[Abstract] This work develops a 2D/3D integrated image sensor that includes photodiodes, pixel circuits, correlated double sampling circuits, sense amplifiers, a multi-channel Time-to-Digital Converter (TDC), a column decoder, a row decoder, a controller and readout circuits. The photodiode of P-diffusion_ N-well_P-substrate is used to sense photos at 2D and 3D modes under different biased voltages. At 2D and 3D modes, a charge supply mechanism and a feedback pull-down mechanism in a pixel circuit are adopted to delay the saturation and accelerate the response, respectively. As well as a multi-channel TDC, rapid parallel reading at a 3D mode is accomplished by using a bus-sharing mechanism. Based on the TSMC 0.35μm 2P4M CMOS technology, a 352×288-pixel 2D and 88×72-pixel 3D integrated image sensor was implemented to have a die size of 12mm×12mm. The dynamic range at a 2D mode can reach 110dB and the depth resolution can be around 4cm at a 3D mode.

[Abstract] We study the effect on the microwave S-parameters of adding a conjugated polymer layer to a deoxyribonucleic acid-based (DNA-based) biopolymer within a variable capacitor (varactor) using a capacitive test structure. The conjugated polymer we are using in this work is P3HT and the DNA-based biopolymer is DNA-CTMA. The results are compared to both the baseline DNA-based biopolymer and the conjugated polymer layer added to a layer of polyvinyl alcohol. The addition of the conjugated polymer layer underneath the DNA-based biopolymer is found to most significantly improve the stability and dielectric tuning of the DNA-based biopolymer.

[Abstract] Measurement results of a linear current-controlled oscillator (CCO) is presented. Output frequency of a ring oscillator is sensed by a linear CMOS switched-capacitor frequency-detector (SCFD) that operates well over the frequency range of the oscillator operation. The feedback is completed by controlling the supply current of the ring oscillator using a negative impedance converter(NIC). This simple low-power circuit does not use operational amplifiers or resistors. The linearization technique is applicable to all types of oscillators. A prototype of this CCO is fabricated in TSMC 0.18µm CMOS process and it has a power consumption less than 3.6 mW in the frequency range of 140 MHz to 1.15 GHz from a supply voltage of 1.8 V. The measured phase noise is -93.44 dBc/Hz at 1 MHz offset from the carrier at the frequency of 501.13 MHz. It achieves 0.12% linearity over the entire tuning range. This CCO can be readily used in ultra-low power wideband and cognitive radios. A method of improving the settling time by a simple circuit modification of the frequency-detector is discussed with supporting post-layout simulation results.

Session A2L-E: Invited Session II

Chair: Mohamad Sawan, *Polytechnique Montréal, Canada*
Time: Monday, August 6, 2012, 13:10 – 14:50
Location: River Fork

[Abstract] Wireless implantable medical devices are expected to perform cryptographic processing at an absolutely low level of power consumption. This paper presents the design of an ultra-low power ASIC core implementing the PRESENT encryption algorithm. To minimize power consumption, subthreshold CMOS logic is adopted. To implement robust combinational logic (S-Boxes) in PRESENT at subthreshold, a multiplexor-tree architecture based on CMOS transmission gates is proposed. Our post-layout simulations show that our PRESENT core consumes around 50 nW at 0.35V supply voltage at 25 kHz clock frequency, proving the feasibility of ultra-low power encryption.

[Abstract] This paper deals with the problem of gathering electrical energy from sources readily available in the environment. In particular we focus on vibrations that are almost ubiquitous and that very often appear as random, weak and low frequency signals. The above listed features may significantly reduce the efficiency of traditional linear resonant and therefore alternative innovative strategies need to be explored. In this paper we present some devices that have been analytically modeled and experimentally verified for tackling this issue. The basic idea is centered on the use of bistable oscillators to realize vibration harvesters that can scavenge energy from broadband, weak, random vibrations: this idea will be expanded here toward some solutions where bistability is obtained by using magnets but also where it descends from purely mechanical devices. A brief review on solutions developed that exploit magnetic and non magnetic strategies for obtaining bistability is presented, finally the issue of MEMS fabrication for the devices conceived will be discussed.

[Abstract] Methods are reviewed for achieving high data rates in bio-implantable devices. Particular attention is given to cortical stimulator arrays for restoring vision. Error-correction codes (ECC) are shown to be essential to obtain reliable operation in next-generation high-rate implants. A survey of reported ECC implementations is presented, and power-vs-performance tradeoffs are revealed after re-scaling to remove differences in technology and clock speed. Recommendations are offered for realizing high-rate ECC circuits within the tight power constraints of implantable device applications.

[Abstract] In this paper a combined LNA-oscillator-mixer is presented, which exploits the non-linear behavior of a two-integrator oscillator. The LNA, oscillator, and mixer are merged in a single block, allowing current reuse. The result is a low area, low cost, and low power RF front-end in a standard CMOS technology. A common-gate LNA is used, which covers the WMTS frequency bands from 600 MHz to 1.4 GHz. A circuit prototype using UMC 130 nm CMOS technology is presented using a MOSFET-only design to optimize the circuit for power consumption and area. The circuit has 9.7 mW power, 1.2 V supply, and an area of 110 × 90 μm2.

[Abstract] Electronic noses (e-nose) have been studied for several years and extensively applied; however, they are limited by their volume and high manufacturing cost. Portable devices have become popular in recent years; therefore, it is crucial to integrate e-noses in portable devices (e.g., mobile phones). This study used TSMC 90nm 1P9M CMOS MSG technology to develop a front-end system-on-chip (SoC) for an electronic nose. The SoC contained interdigitated electrodes, multi-channel sensor interface circuits, an analog to digital converter, and a digital continuous restricted Boltzmann machine (CRBM). Various conducting-polymer materials were titrated on the interdigitated electrodes to form an on-chip sensor array. This SoC was controlled through an external microcontroller to perform odor identification and analysis. The simulation results of the SoC and gas classification show that this chip is suitable for portable applications and further integration.

Session A2L-M: Nanoelectronics

Chair: Wan Kuang
Co-Chair: Kris Campbell
Time: Monday, August 6, 2012, 13:10 – 14:50
Location: Suite 214

[Abstract] In this work, a novel design and optimization method for programmable gate macro blocks (PGMB) in the newly proposed Asynchronous Nanowire Reconfigurable Crossbar Architecture (ANRCA) is presented. ANRCA is based on a self-timed logic referred to as the Null Convention Logic (NCL). Since there is no global clocking and clock distribution network, all failure modes related to timing will be either eliminated or relaxed. The proposed architecture is anticipated to have higher manufacturability and robustness that are critical factors in nanoscale systems due to nondeterministic nature of nanoassembly. In order to facilitate efficient programming and flexible reconfiguration, a new hierarchical reconfigurable architecture for ANRCA is also proposed. Various configurable logic block structures have been considered and also their programming and reconfiguration issues are discussed.

[Abstract] The recently proposed asynchronous nanowire crossbar architecture is envisioned to enhance the manufacturability and robustness of nanowire crossbar-based configurable digital circuits by removing various timing-related failure modes. Even though the proposed clock-free nanowire crossbar architecture has numerous technical merits over its clocked counterparts, it is still subject to high defect rates inherently induced by the nondeterministic nanoscale assembly of nanowire crossbars. To address this issue, a novel post-configuration repair strategy specific to the asynchronous nanowire crossbar architecture has been proposed. The proposed repair strategy is to selectively test highly defect-prone ON-state programmed crosspoints and reconfigure the given logic function to circumvent the ON-crosspoints tested as faulty by utilizing redundant rows/columns.

[Abstract] In non-volatile logic, MTJs are used to store and compute by coupling with one another. In this paper we have developed a novel variability tolerant differential read for non-volatile logic by using certain inherent properties of the logic. The novel read circuit compares n similar valued bits with their n complements. Apart from being more robust to variations in MTJ, the novel read circuit provides a higher sense margin than an ordinary differential read. We have also investigated the factors that influence the sense margin in the novel read circuit and provided supportive simulation results.

[Abstract] Elastic or channel buffers can improve the overall power and area overhead of Network-on-Chip architectures by reducing or replacing large, power hungry router buffers. We design three fault tolerant schemes for our channel buffers which are used in a concentrated torus topology to reduce power consumption and improve throughput and latency. Our proposed fault tolerant techniques are evaluated using the Synopsys Design Compiler and our results show (i) an improvement in energy-delay product ranging from 20% to 43%, (ii) improvement in saturation throughput of 32% and (iii) an overall reduction in area overhead by 53-68% over other state-of-the-art electrical topologies.

[Abstract] A metallic CNT renders a short circuit between drain and source in a CNTFET. Technologies capable of removing metallic CNTs create open circuits which degrades SRAM cell performance and functionality. In this paper we present a design approach to tolerate removed metallic CNT in CNTFET SRAM. The proposed approach uses an MxN array of uncorrelated CNTs to form a CNTFET. An extremely high probability of having a functional memory array can be obtained with a modest semiconducting CNT probability (Psemi) of 90% and a 1x4 uncorrelated CNT array. Three optimization schemes are also proposed to minimize the impact of metallic CNT removal.

Session A3P-F: Analog and Mixed-Signal Circuits I

Chair: Paul Furth, *New Mexico State University*
Time: Monday, August 6, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] Sensing systems of implantable medical devices such as pacemakers, internal cardiac defibrillator (ICD), and cardiac resynchronization therapy (CRT) products have bandpass anti-aliasing filters with lower-pole frequency placed at sub-Hz. Today's medical devices use off-chip microfarad-range capacitors along with on-chip resistors to create such low-frequency pole. For this purpose, often up to twelve medically-graded hybrid capacitors are needed on the device substrate. These capacitors are major source of four drawbacks: reliability, real-estate (size), cost, and noise. This paper realizes a fully integrated Gm-C anti-aliasing filter, combining three techniques to reduce the operational amplifier transconductance into sub-nano-Siemens range: active linearization, current cancellation, and series-parallel active. Each filter consumes only 20nA.

[Abstract] Present paper proposes an injection locked oscillator under multiple injection sources. An injection locked frequency divider (ILFD) under multiple injections with harmonic components of 2nd and 3rd harmonic improves the phase noise performance of the oscillator substantially compared to the single source injection. Simulation results show that at the supply voltage of 2.4V, at the injected signal power of 0dBm the simulated phase noise of the free running ILFD oscillating at frequency of 2.72 GHz is -108.5dBc/Hz at 1.04MHz offset frequency and the phase noise of the locked oscillator output being -123.24dBc/Hz showing an improvement of 14.72dBc/Hz with 6.4mW of power consumption.

[Abstract] Sliding Discrete Fourier Transform (SDFT) based phase locking scheme (PLL) is employed to extract the modulation signal from the sinusoidal phase or frequency modulated carrier. Adaptive sampling control based SDFT PLL has been proposed for frequency demodulation. This PLL holds the unique advantage of wider operating range, which has been utilized in the frequency demodulation. Simulation studies prove the efficiency of the demodulation method in retrieving the frequency of modulation signal.

[Abstract] A new fully differential ultra low-voltage, ultra low-power down-converter mixer for ultra wideband application is presented in this paper. This mixer is designed using four-terminal MOS transistors. The radio frequency is applied to source and local-oscillator signal is applied to the gate with body of devices simultaneously. A DTMOS common source amplifier is employed increasing conversion gain. The proposed circuit is designed and simulated in the TSMC 0.18μm CMOS process. The simulation results show that the proposed mixer has a peak conversion gain of 12.3dB with 3dB RF frequency bandwidth from 2GHz to 10.5GHz with a fixed IF frequency of 100MHz. The third-order intermodulation-intercept point (IIP3) varies from -5.2dBm to -7.3dBm between 2-10.5GHz. The proposed mixer consumes only 1.28mW power with 0.5V supply voltage.

[Abstract] An ultra-low voltage, self-starting, switched-capacitor based charge pump is proposed for energy harvesting applications. The integrated linear charge pump topology presented in this work has been optimized for low-voltage start-up. The control signals for the charge-transfer switches (CTS), generated using two clock phases, reduce reverse currents and thus improve the efficiency of the converter. Adiabatic switching techniques have been employed to reduce the switching losses associated with the CTS gate control. This design has been implemented in a 130-nm CMOS process. Simulation results demonstrate a low startup voltage of 125 mV with efficiency of 62 % for a static current load of 0.1 uA.

Session A3P-G: Analog and Mixed-Signal Circuits II

Chair: Vishal Saxena, *Boise State University*
Time: Monday, August 6, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] An 8 bit, 1.5 b/stage fully differential (FD) multiplying digital to analog converter (MDAC) pipeline ADC for use in a smart RFID is presented in this paper. The FD Operational Transconductance Amplifier (OTA) in the MDAC utilizes a novel common mode (CM) amplifier, which is inherently stable demonstrating reduced common mode offset and improved compensation tracking across process. Furthermore, a simple offset cancellation technique robust to device leakage is introduced to correct error due to leakage induced input offset voltage drift. Monte Carlo simulation results show that for the input voltage range of ±400mV, ADC can achieve 8 ENOB with sampling frequency at 16 kHz. Total ADC power consumption is 5.1uA with 0.7V power supply. The ADC was submitted for fabrication in 180nm CMOS with results forth coming.

[Abstract] As an apt choice for long-term analog memory in standard CMOS processes, floating-gate transistors are key enablers for large-scale programmable analog systems. Such systems are often designed for battery-powered – and generally resource-constrained – applications, which require the memory cells to program quickly with low infrastructural overhead. In order to meet these needs, we present a new analog floating-gate memory cell. Our four-transistor memory cell offers both voltage and current outputs and has linear injection and tunneling characteristics. Furthermore, we present a simple programming circuit that forces the memory cell to converge to voltage targets within 100ms and with 8-bit accuracy.

Session A3P-H: Analog and Mixed-Signal Circuits III

Chair: Jose Silva-Martinez, *Texas A&M University*
Time: Monday, August 6, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] This paper presents a low-power maximum power point tracker (MPPT) and power management system (PM) for low-power photovoltaic (PV) cells integrated in a 0.5µm 2P3M CMOS process. The MPPT utilizes the fractional open circuit method that approximates the optimal operating voltage of the PV cell as a fraction of the cell's open circuit voltage. The system utilizes an inductive boost converter to provide DC-DC conversion to provide a suitable supply voltage from a low-voltage input. The PM multiplexes the system supply source between battery backing and harvested energy stored in supercapacitors. The measured power consumption of the chip was 11.3µW.

[Abstract] This array DLL is based on self-biased technique and achieves high process technology independence, fixed damping factor, fixed bandwidth to operating frequency range and input phase offset cancellation. The results show that the total delay time between the input and the output of the DLL (Delay Lock Loop) is one clock cycle and all of the delay cells provide precise output without false locking or harmonic locking. Test results show a timing jitter of less than 1pS for the DLL circuit and has very low phase sensitivity errors. The timing generator implemented as an array of delay locked loops has exponentially reduced the locking time as well avoids false locking or harmonic locking. An experimental proto type was simulated using 130nm technology with a supply voltage of 1.2V.

Session A3P-J: Analog and Mixed-Signal Circuits IV

Chair: Paul Furth, *New Mexico State University*
Time: Monday, August 6, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] A new approach to investigate noise spikes due to regeneration in a relaxation oscillator is proposed. Noise spikes have not been satisfactorily accounted for in traditional phase noise models. This paper attempts to explain noise spikes/jump phenomenon by viewing it as phase change in the physical world (for example, from gas to liquid or magnetization of ferromagnet). Both are due to regeneration (positive feedback in oscillator as well as alignment of spin due to positive feedback in ferromagnet). The mathematical tool used is the action path integral based on Lagrangian. As a first step towards this explanation in this paper, simulations on circuits using 0.18µm CMOS as well as simulations on ferromagnet (Ising model) were performed and both show jump phenomenon, illustrating the viability of this approach.

[Abstract] Restoration of the trapezoidal shape current pulse received via antenna transformer in inductive-coupling link is investigated. It is shown that the transformer output signal may be considered as a superposition of slow and fast components. The equivalent circuits for calculation of each component are given. The Lee load amplifier-comparator allows one to find an optimal suppression of the fast component. This simplifies the design of the comparator output stages. The output latch of the receiver includes confirmation circuits that allow one to reduce the output pulse jitter. The receiver is designed for realization in 90 nm CMOS technology.

[Abstract] This paper presents a power line communications (PLC) receiver in ICs with emphasis on robustness. The PLC receiver intends to control internal logic values of ICs through power pins. It employs a differential Schmitt trigger to increase noise immunity and tolerate supply voltage fluctuations. The receiver is designed and laid out in 0.18 µm CMOS technology. Post-layout simulation results show that the receiver can operate up to 22.2 percent of the supply voltage drop under the signal-to-noise ratio (SNR) of 10.2 dB. The receiver dissipates 2.4 mW under 1.8 V supply, which is lower than earlier PLC receivers.

[Abstract] In this paper, an offline calibration technique to compensate offset, gain and timing mismatch errors in a 2-channel gigasample per second (GSPS) time-interleaved(TI) Analog-to-Digital converter(ADC) is presented. Moreover, an equalization method estimating and compensating these mismatch errors in a 2-channel TI ADC is introduced. This equalization method, which can be implemented with low hardware overhead, requires only that the input signal is band-limited to the Nyquist frequency of the 2-channel TI ADC.

[Abstract] This paper proposes a state-space approach for implementation of a continuous-time adaptive notch filter with a gradient-based algorithm for a single sinusoid frequency estimation. Transient analysis of the proposed algorithm is carried out under the assumption of slow adaptation. Tracking characteristics are also investigated for linear chirp and sinusoidally-varying input signal frequency. Closed-form expressions for frequency tracking error for both cases are derived. Finally, simulation results are presented to verify the validity of the proposed algorithm and derived expressions.

Session A3P-K: Analog and Mixed-Signal Circuits V

Chair: Vishal Saxena, *Boise State University*
Time: Monday, August 6, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] A fully integrated low noise amplifier suitable for ultra-low voltage and ultra-low-power UWB applications is designed and simulated in a standard 0.18µm CMOS technology. Using the common gate, current reuse topology and forward body biasing technique, the proposed UWB LNA works at a very low supply voltage and low power consumption. The flat gain diagram of the LNA are achieved by the series inductors insertion between the cascaded stages of LNA. The proposed UWB LNA has a maximum power gain of 14.6 dB with a minimum noise figure of 3.7 dB, while consuming 3.1mW power with an ultra low supply voltage of 0.6 V.

[Abstract] An ultra-low-voltage ultra-low-power operational transconductance amplifier (OTA) using dynamic threshold MOS (DTMOS) technique is presented in this paper. The proposed topology based on a bulk and gate driven input differential pair employs a gain-stage in the Miller capacitor feedback path to improve the pole-splitting effect. The circuit is designed in the 0.18µm CMOS technology. The simulation results show that the amplifier has a 91dB open-loop DC gain and a unity gain-bandwidth of 111.4 KHz while operating at 0.4V supply voltage. This technique show remarkable enhancement in unity gain-bandwidth and also in DC gain compared to the bulk driven input differential pair technique. The total power consumption is as low as 386nW which makes it suitable for low-power bio-medical applications.

[Abstract] A single-channel 1.0-GS/s 8-bit Voltage-Buffer-Free Pipelined-Folding-Interpolating analog-to-digital converter is presented. Grouped T/H blocks are adopted to cancel the voltage buffer between the T/H block and pre-amplifiers array. A new full-digital T/H switch is proposed to cancel the bootstrapped capacitor, which can save the chip area grandly. An improved single-diode switch with an extra reset path is proposed as inter-stage sampling switches. The ADC implemented in 65nm CMOS technology achieves SNDR of 47.5 dB and SFDR of 57.8 dB for 487.3 MHz input frequency at the rate of 1.0GS/s. The power consumption is 75 mW with supply voltage of 1.2 V.

[Abstract] The current-splitting architecture for the current-steering DAC can reduce the area of the current source array greatly. A background calibration technique for current-steering digital-to-analog (DAC) with the current-splitting array is presented. The proposed calibration technique can eliminate mismatch errors for both the upper bits array and the lower bits array in the background. A 14-bit current-steering DAC is fabricated in a 0.18µm CMOS process. The SFDR can be improved more than 20dB. The DAC achieves more than 80dB SFDR at 2MHz for a 200MS/s sampling rate. The active area is 1.26mm2 and power consumption is 125mW.

Session A3P-L: Analog and Mixed-Signal Circuits VI

Chair: Vishal Saxena,
Time: Monday, August 6, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] Use of pulse time modulated (PTM) subcarriers in optical links represents an attractive alternative for transmitting analog and digital signals over optical fiber channels. A novel approach for the optical transmission of multiplexed audio and video signals using a pulse width modulated (PWM) electrical subcarrier over optical delays is reported in this paper.

[Abstract] The objective of the present paper is to give a summary of the theory of the bifrequency analysis for the class of linear time-varying (LTV) systems. The emphasis is on the frequency characterization of dynamic systems using the classical two-dimensional Laplace transform (2DLT). The merit of this powerful technique, which has not sufficiently been explored, is illustrated by examples.

[Abstract] This work is concerned with the transconductance-current dependence of sub-micrometer MOSFETs. The gm-I expression given by the Advanced Compact Model (ACM) is reviewed and simple modification is proposed. The modification yields an expression which (with proper parametrization) captures the gm-I dependence of short-channel MOSFETs. The proposed expression is “universal” in the sense that it is capable of modeling the gm-I dependence of long-channel MOSFETs, short-channel MOSFETs, and resistively-degenerated BJTs.

[Abstract] The proposed flash memory architecture utilizes rank modulation that uses the order of cell levels instead of absolute levels. A three row array of WTA circuits was used to determine the rank of 4-cell sets in simulation. This demonstrates the viability of the rank modulation scheme, and it prompted the design and fabrication of a larger prototype IC.

[Abstract] In this paper, logic gates realization using memristor based material implication gate has been presented. A new realization for two carry lookahead adder architectures based on memristors has been presented. The performance parameters of the implementations have been presented and discussed. Also, a comparison with the conventional memristor based ripple carry adder has been performed.

Session A4L-A: Analog Design Techniques I

Chair: Jose Silva-Martinez, *Texas A&M University*
Time: Monday, August 6, 2012, 16:00 – 17:40
Location: White Water

[Abstract] Sleep states are used in resource-constrained systems to conserve power, but they necessitate a wake-up circuit for detecting unpredictable events. In such systems, all information preceding a wake-up event will be forfeited. In this paper, we describe an analog memory system that adaptively samples and records an input signal while the rest of the system sleeps, thereby preserving the information that would otherwise be lost. This system does so while consuming less than 3.52 uW. We also show how the adaptive sampling rate can be utilized to approximate the original signal using a minimal number of samples.

[Abstract] A low-power switched-capacitor (SC) gain stage based on a capacitive charge-pump (CP) is proposed. It is shown that the CP gain stage achieves the same input-referred thermal noise as a conventional SC gain circuit, while consuming significantly lower power. The effect of parasitic capacitances on the CP gain circuit is discussed. Simulation results confirming the improved power/performance trade-off of the CP gain stage over the conventional approach are provided.

[Abstract] SHE (Selective Harmonic Elimination) method doesn't allow elimination of harmonics in real time. The switching angles are calculated offline using iterative computations and programmed into a digital processor. In this paper we propose a novel harmonic elimination technique where real time modulation is used to eliminate the undesired harmonics. The method uses sine-sine modulation as a base model. The switching angles determined through the model are perturbed to compute the angles necessary to eliminate the selected harmonics, thus reducing the complexity of computation. Using these switching angles, we are advancing a method of finding a modified carrier as a means to provide a low cost comparison-based solution to harmonic elimination. The reference sinusoid with the desired signal frequency is compared against the modified carrier that has same time period as the reference. Simulation/experimental studies verify the proposed method.

[Abstract] The sub-regulators for biasing circuits represent further development of Zener-diode voltage regulators. The line resistor is substituted by a line transistor which is controlled by the current in the Zener-diode equivalent circuit. Introducing this control link one obtains a feedback circuit which preserves the current in the Zener-diode equivalent. This approach improves rejection of power supply voltage variations in the output voltage. It also reduces the output impedance of the regulator which, in turn, reduces the influence of load variations. Introducing the feedback requires attention to the circuit stability, and the proposed electronic circuit provides a simple elimination of the stability problem. The example of sub-regulator design is given, and the simulations confirm the validity of the approach.

Session A4L-B: Digital Circuits III

Chair: Pramod Meher
Co-Chair: Abhilash Goyal
Time: Monday, August 6, 2012, 16:00 – 17:40
Location: Rapids

[Abstract] In this paper we first analyze the column sum boundaries of n-digit parallel decimal array multipliers (PDAM). A general form of the problem is formed and a heuristic solution is found with Genetic Algorithm (GA) for 16-digit multiplication. Then, for small n-digit multipliers the GA results are proved with exhaustive search. Finally, new tight boundaries on the column sums are used in a hardware implementation of a 16-digit PDAM. Inclusion of the proposed boundaries provides an 8% speedup or 20% less area.

[Abstract] A study of a simplification of the NULL Convention Logic is studied. The aim of such a simplification is to decrease the resources use especially by removing state-holding gates in combinational parts while ensuring data integrity. A model is also provided to understand the limits of the gain of such a modification. Moreover we discuss the impact on operating frequency and dynamic consumption.

[Abstract] This paper presents the all-digital phase-locked loop (ADPLL) with the local passive interpolation time-to-digital converter (LPI-TDC). Unlike the conventional LPI-TDC, the proposed TDC has a tristate inverter delay cell in only first delay chain, other delay cell is composed of only normal inverters that have same delay as tristate inverter. LPI-TDC based a tristate has the advantages of higher resolution and lower power consumption than conventional LPI-TDC. The resolution and power consumption decreases approximately 12% compared to the conventional LPI-TDC. The proposed ADPLL has been implemented using 0.18um CMOS process.

[Abstract] The fierce competition in today's global market has made trustworthy authentication an essential aspect for the implementation of valuable designs. To counter such threats, methodologies have been developed that require a unique signature-key for every fabricated chip. This paper presents a PUF design for trustworthy authentication of an FPGA. The uniqueness of the PUF responses is calculated as 49.0625%. Hamming distances for 128-bit responses are calculated and represented graphically. This work also involves an error correction process using BAMs to correct the error bits occurring due to considerable environmental changes. The proposed method drives the failure rates below 1ppm.

[Abstract] A compact lookup table (LUT) circuit using spin transfer-torque magnetic tunnel junction (STT-MTJ) devices combined with MOS transistors is proposed for a standby-power-free field-programmable gate array (FPGA). Since STT-MTJ devices essentially have an asymmetric characteristic in switching currents, one of two write-control transistors can be implemented with a small feature size, while the width of the other one is still large. By sharing the large size of write-control transistor, almost all the transistor size in the proposed LUT circuit becomes small. In fact, the effective silicon area of the proposed write-control transistors for a 6-input LUT circuit is reduced to 68 percent in comparison with that of a conventional nonvolatile LUT circuit without applying the asymmetric transistor sizing.

Session A4L-C: Sensing and Detection Circuits

Chair: Vishal Saxena, *Boise State University*
Time: Monday, August 6, 2012, 16:00 – 17:40
Location: Ivy

[Abstract] We present an integrated analog signal processor for resource-constrained sensing applications, such as wireless sensor networks, wherein sensors are remotely deployed in inaccessible locations. The processor, which is reconfigurable and operates at 27.8 microwatts, extends the capabilities of sensor nodes by performing spectral analysis and event detection in low-power circuits. The performance of the IC is demonstrated in an example sensing application (i.e. vehicle classification).

[Abstract] We present a fully-integrated analog CMOS image centroid computation sensor. A 40x40 pixel array is designed and fabricated in a 0.5um CMOS process. The proposed centroid computation circuit achieves 7 times improvement in bandwidth compared to similar circuits in the literature. Moreover, the incorporation of a linearized transconductor improves precision in the computed centroid. The sensor is designed to operate over a wide range of photocurrents from 10 pA to 1 uA. Test results of the proposed architecture verify its superior performance.

[Abstract] Achieving coherent sampling to accurately estimate spectral characteristics of a signal is a very challenging task. Though the Four point sine wave fitting method can be used to accurately estimate some spectral parameters of a non-coherently sampled signal, not all parameters can be estimated accurately. This paper proposes a method that can be used to accurately estimate ALL the spectral characteristics from the spectrum when a signal is not sampled coherently. The non-coherent fundamental and harmonics are accurately identified and replaced with their corresponding coherent signals to achieve accurate results. Simulation results show the effectiveness and robustness of the method.

[Abstract] This paper presents the design of an operational transconductance amplifier-C (OTA-C) low pass filter for a portable electrocardiogram (ECG) detection system. A fifth order Butterworth using ladder topology is utilized to reduce the effect of component tolerance and to provide a maximally flat response. The proposed filter is based on a novel class AB digitally programmable fully differential OTA circuit. Based on this, PSPICE simulation results for the filter using 0.25u m technology and operating under 0.8V voltage supply are also given. The filter provides a third harmonic distortion (HD3) of 0.91% for 100mVp-p sinusiodal input, input referred noise spectral density of 50 uVrms/square root Hz, total power consumption of 26u W and a bandwidth of 243Hz. These results demonstrate the ability of the filter to be used for ECG signal filtering which is located within 150Hz.

[Abstract] In this paper we present a novel all digital binary phase shift keying (BPSK) demodulator dedicated implantable biosensor. This demodulator offers the advantages of ultra-low power and low complexity structure which are very essential to develop wireless miniaturized implantable devices. As the continuation of our research approach to implement a glucose sensor implanted under skin, herein, we address the design and analysis of a demodulator integrated in a CMOS chip along with other required building blocks. In order to minimize the effect of transmitter frequency changes and to enhance the circuit robustness a digital self-calibration technique is also proposed. Simulation results show that the demodulator can tolerate a relatively large frequency shift of at least ±80% around the centre frequency in all process corners. The power consumption of the demodulator at a data transmission rate of 16 Mbps and a supply voltage of 1.8 V is as low as 27µW.

Session A4L-D: Bioengineering I

Chair: Esther Rodrigez-Villegas
Co-Chair: Sreeraman Rajan
Time: Monday, August 6, 2012, 16:00 – 17:40
Location: Clear Water

[Abstract] System design issues for integrated impedance spectroscopy measurement system that can be used to measure the impedance of an electrode-electrolyte interface caused by bio-chemical interface for the array of biosensors are discussed in this work. Using the approach presented in this article, it is possible to measure spatial and temporal distribution of bio-chemical interactions caused by in-vitro activity of a slice of the neurons in real time. Standard instrumentation cannot be used for such measurements because of many instruments needed, disturbances caused by long connecting wires, parasitic capacitances and resistance, and high cost, therefore, the miniaturized integrated array of instruments is needed. In this article, we describe and evaluate possible different approaches, system design issues and possible limitations for such integrated impedance spectroscopy instrument.

[Abstract] This paper describes the design of a phase synchronous detection system as a solution of the digital stage for high frequency bioimpedance computing in a four-electrodes-measuring configuration. The proposed design is implemented on reconfigurable hardware. The phase detection system is proposed as part of a bioimpedance measuring system, where biompedance value is obtained as a complex division of voltage and current in the measuring cell. The use of parallel processing to obtain such complex values allows high frequency bioimpedance measurements. Since the project is focused on the digital stage design of the bioimpedance measurement system, the phase delay between the biological tissue current and voltage is digitally generated with delay blocks. In this way bioimpedance value result is tested for a given delay, corresponding to a phase difference. According to obtained results, small measurement errors for wideband frequency range are achieved with the proposed system.

[Abstract] A novel scheme for amplification in neural recording systems is proposed in this work that allows us to remove the large `pseudo-resistors' needed to bias the typically used capacitive amplifier topology. Comparison and reset circuits are implemented with the core amplifier to fold the output waveform of amplifier into a preset output range for digitizing by an ADC. A reconstruction algorithm is then used in the digital domain to recover the amplified signal from the folded waveform. By removing the pseudo-resistors, higher robustness, less noise in LFP band and better matching and programmability of high pass corner can be achieved in the proposed design. Simulation and measurement results are presented from a prototype fabricated in 65nm CMOS. The presented scheme is general and can be used with any capacitive amplifier.

[Abstract] Affinity-based biological sensor field-effect transistors (BioFETs) exhibit a large amount of noise in their drain current under constant bias. In this work, we use SPICE to simulate the effect of sensor noise on a differential pair amplifier detection circuit. This is accomplished by the generation of a realistic noise signal with 1/f power spectrum which is applied to the back gate and reference electrode of a nanoribbon BioFET sensor. The resulting output signal from the transient simulation is time-averaged to obtain the noise rms amplitude. The ability to distinguish the sensor signal from the noisy environment is examined for various amounts of noise power and integration time. Corresponding minimum theoretical direct detection limits for of Biotin-Streptavidin attachment and DNA hybridization are also provided, along with discussion of possible methods to reduce the noise effects.

Session A4L-E: Special Session I: Continuous-Time Delta-Sigma Analog-to-Digital Converters

Chair: Vishal Saxena, *Boise State University*
Time: Monday, August 6, 2012, 16:00 – 17:40
Location: River Fork

[Abstract] This paper discuses the use of hybrid continuous-time/discrete-time Sigma-Delta (SD) modulators for the implementation of high-efficiency wideband analog-to-digital converters. Two alternative implementations of multi-rate cascade architectures are studied and compared with conventional single-rate continuous-time topologies. The effect of three error mechanisms is considered, namely: mismatch, finite dc gain error and finite gain-bandwidth product. In all cases, closed-form expressions are derived for the nonideal in-band noise power of all SD modulators under study, giving an analytical relation between their system-level performance and the corresponding circuit-level error parameters. Time-domain behavioral simulations are in good agreement with theoretical predictions, demonstrating the validity of the presented approach.

[Abstract] Single-bit SDM is not very suitable for wide bandwidth and high dynamic range applications even though they are the perfect choice in deep sub-micron digital process. This paper describes few novel approaches which achieves close to multi-bit modulator performance without losing the advantage of the single-bit modulator.

[Abstract] This paper demonstrates the effectiveness and robustness of amplifier finite gain bandwidth compensation within a wideband third order CT delta sigma modulator and the effects of process, mismatch and temperature on modulator stability. In many state of the art designs, GBW is kept safely above the sampling frequency of the modulator, which suffers a power penalty especially for high-speed designs. While gain errors and phase shifts in the loop filter due to finite GBW can be compensated for, its robustness is often questionable, especially if an additional excess loop delay is concerned. The robustness of such a compensation is analyzed for an exemplary CT DSM with an fs of 500MHz which has been designed in a 1.2V 90nm TSMC CMOS process.

[Abstract] Continuous-time delta sigma (CT-DSM) ADCs are established as the data conversion architecture of choice for the next-generation wireless applications. Several efforts have been made to simultaneously improve the bandwidth and dynamic range of 4 ADCs. We proposed using two-step quantizer in a single-loop CT-4 modulator to achieve higher conversion bandwidth. This paper presents a tutorial for employing the design technique through a 130n CMOS implementation. The proposed 640 MS/s, 4th order continuous-time delta sigma modulator (CT-DSM) incorporates a two-step 5-bit quantizer, consisting of only 13 comparators. The CT-4M achieves a dynamic range of 70 dB, peak SNDR of 65.3 dB with 32 MHz bandwidth (OSR = 10) while consuming only 30 mW from the 1.2 V supply. The relevant design trade offs have been discussed and presented with simulation results.

[Abstract] Blocker and jitter sensitivity of continuous-time sigma-delta (CT-DS) converters is discussed. The interaction between blockers and clock jitter and its effect on the ADC resolution is also investigated. It is observed that out-of-band (OOB) blockers and clock jitter in the feedback DAC degrade the ADC resolution by convolving with the OOB quantization noise, thereby increasing the in-band noise floor. Some techniques on how to improve the blocker and jitter tolerance of CT-SD ADCs are outlined. It is verified that blocker tolerance relaxes the baseband channel filtering requirements in the signal path of a broadband receiver. By monitoring the internal signals of the ADC and dynamically controlling a front-end programmable gain amplifier, saturation and overload is avoided in the presence of strong interferers. The proposed blocker mitigation technique avoids changing the ADC internal loop parameters dynamically, resulting in fast settling time performance with moderate penalties in SNDR and circuit complexity.

Session B1P-F: Digital Circuits IV

Chair: Abhilash Goyal
Co-Chair: Pramod Meher
Time: Tuesday, August 7, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] Various CMOS implementations of asynchronous NULL Convention Logic (NCL) gates have been compared in terms of area, speed, energy, power, supply voltage, and noise. Additionally, a new approach to design semi-static NCL gates has been introduced. Each gate type is used to realize a delay-insensitive 4×4 NCL multiplier and the simulation results are compared. It is shown that different realizations excel in different design parameters. This paper aims to provide NCL designers with the tradeoffs of using various NCL gate types.

[Abstract] Godson-2H is a complex SOC of Godson series, which is a 117mm2, 152 million transistors chip fabricated in 65nm CMOS LP/GP process technology. It integrates a 1GHz processor core and abundant high and low speed peripheral IO interfaces. Large scale and extremely strict low power requirements make great challenges in the chip design phase. To meet low power constraints in different application scenarios, most of state-of-art low power methods are carefully adopted. This paper describes the most effective low power design methods used in Godson-2H, which are dynamic voltage and frequency scaling, power gating and aggressive multi-voltage design.

[Abstract] Glitches due to soft errors can act as a severe deterrent to asynchronous circuit operations. To mitigate soft errors in quasi delay insensitive (QDI) asynchronous circuits, built-in soft error correction in NULL convention logic (NCL) has been introduced [9]. However, this technique cannot detect errors during the NULL phase of NCL pipeline, and also cannot avoid error propagation into the pipeline after its detection. This paper provides a modified approach to overcome these limitations with, on average, comparable power and latency costs. This work also analyzes the temperature variation effects on latency and power consumption of the proposed design. The modified NCL pipeline is implemented in IHP 90nm CMOS technology and analyzed under various operating temperatures. It is found that the proposed design survives well in the worst case operating temperatures and does not propagate soft errors

[Abstract] Modulo 2^n+1 multiplier is one of the critical components in the area of digital signal processing, residue arithmetic, and data encryption that demand high-speed and low-power operation. In this paper, a new circuit implementation of a high-speed low-power modulo 2^n+1 multiplier is proposed. It has three major stages: partial product generation stage, partial product reduction stage, and the final adder stage. The proposed structure introduces a new MUX-based compressor in the partial product reduction stage to reduce power and increase speed, and in the final adder stage, the sparse-tree-based inverted end-around-carry adder reduces the number of critical path circuit blocks, also avoids wire interconnection problem. The proposed multiplier is implemented using both 32nm CNTFET (Carbon-Nanotube FET) and bulk CMOS technology for performance comparison. The CNTFET-based design dramatically decreases the PDP (Power Delay Product) of the circuit. The simulation results demonstrate that the power consumption of CNTFET-based multiplier is at average 5.72 times less than its CMOS counterpart, while the PDP of CNTFET is 94 times less than the CMOS one.

[Abstract] A novel Asynchronous AES Round Function design is proposed in this paper, which offers increased Side-Channel Attack (SCA) resistance by combining the advantages of dual rail encoding and clock free operation. The design is based on a Delay Insensitive (DI) logic paradigm known as Null Convention Logic. By reducing switching activity and thereby Signal-to-Noise (SNR) ratio, the proposed design leaks far less side channel information than traditional approaches and this feature boosts SCA resistance of this approach. Functional verification and WASSO analysis simulations were carried out on both synchronous approach and the proposed NCL based approach using Xilinx simulation tools to validate the claims related to benefits of employing this novel dual rail design approach.

Session B1P-G: Digital Circuits V

Chair: Pramod Meher
Co-Chair: Abhilash Goyal
Time: Tuesday, August 7, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] This paper presents a novel multiplexer-based carry-skip algorithm for hybrid adder design based on the parallel-prefix computation technique. The hybrid adder combines both carry-lookahead and multiplexer-based carry-skip architectures to speed up the performance. The driving capability of the critical path is enhanced to boost the speed, while optimizing both area and power in the non-critical paths. Experimental results show that the proposed 64-bit hybrid adder achieves low cost (46 x 210 um2), low power (2.82 mW), and high speed (246.5 ps), where the UMC 90 nm CMOS process is simulated with 1.0V supply voltage.

[Abstract] The 3N encoding process can be simply to add the input data N to its 1-bit left-shifted value 2N using the combinational digital circuits, such as ripple carry adder (RCA) or carry look-ahead adder (CLA). This paper presents an efficient algorithm and its hardware implementation. Results show that the proposed RCA-like 16-bit encoder achieves 25% less in hardware cost and 50% faster in speed performance than the use of the conventional RCA. The proposed CLA-like 64-bit encoder achieves 1.73 ns which is approximately 20% faster than the use of the conventional CLA.

[Abstract] Modern FPGAs are built in 28nm technologies, where even combinational circuits are substantially vulnerable to soft errors. Such designs require soft error mitigation circuits in their data paths. Conventional soft error mitigation techniques such as triple modular redundancy are robust but their area overhead is three times as compared to normal design. In this paper a variant of automatic repeat request (ARQ) protocol is proposed, along with delayed redundancy to reduce area overhead. Synthesis results show an improvement of 9.1 and 10% in latency for Cyclone II and Stratix II FPGAs, respectively, with a 1.94 times improvement in resource utilization.

[Abstract] In this paper a novel modular superscalar execution core is presented for a medium grain reconfigurable hardware. The processor can be configured for varying path widths, reservation station depth, and reorder buffer size with minimal redesign effort. An analysis comparing the superscalar core with a five-stage execution core shows that a speedup of 2.073 can easily be achieved while increasing area by only 29%.

Session B1P-H: Digital Circuits VI

Chair: Abhilash Goyal
Co-Chair: Pramod Meher
Time: Tuesday, August 7, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] This paper describes a design for a variable fractional delay FIR filter implemented on reconfigurable hardware. The proposed design builds upon the traditional Lagrange interpolator FIR filter using either a software-based or hardware-based Lagrange coefficient computational unit along with reconfigurable hardware for real-time updating of the FIR coefficients. Furthermore, this proposed design implements a scaling filter order, permitting fractionally delayed signals of varying integer sizes, while simultaneously centering the filter over the sampled data. The resulting real-time VFD FIR filter is tested using the Xilinx System Generator toolkit as well as ModelSim.

[Abstract] As CMOS technology is scaled down more aggressively; the reliability mechanism (or aging effect) caused by progressive gate oxide breakdown (also called time dependent dielectric breakdown (TDDB)) has become a major reliability concern. The oxide breakdown is categorized into hard breakdown (HBD) and soft breakdown (SBD). With the present of HBD and SBD, it is difficult to control the ON current of the MOSFET device. Especially, HBD causes a catastrophic failure of the device and the entire circuits. In this paper, the TDDB effects on the delay and power of the nanoscale CMOS circuits are analyzed using ISCAS85 benchmark circuits, which are designed using a 45-nm CMOS predictive technology model. Based on the TDDB analysis, a new hard breakdown monitoring circuit has been proposed.

[Abstract] Due to the shrinking of dimension and decreasing of the supply voltage, processors based on deep submicron technologies are more susceptible to defects and errors. This paper presents a model to simulate the behavior of the Reed-Solomon decoder prone to transient faults. The simulation environment developed allows to analyze the influence of the different blocks on the reliability of the decoder. Identifying the most critical blocks of the processor allows the designer to implement a selective hardening strategy and then to minimize the additional costs associated to improve fault tolerance.

[Abstract] A fast-convergence and robust digital calibration approach for a 14-bit 200MS/s hybrid pipeline-SAR ADC, correcting errors not only from capacitor mismatch, gain error, op amp nonlinearity, and comparator offset, but also the reference DAC error and inter-stage mismatch errors. It is robust and permits higher error margin for analog design. The proposed algorithm has been verified with gate level simulation as well as FPGA implementation, where the proposed design achieves a DNL of -0.59/0.28 LSB, an INL of -0.59/0.34 LSB and an SNDR of 84 dB at input near Nyquist frequency of 90.55MHz

Session B1P-J: Digital Circuits VII

Chair: Pramod Meher
Time: Tuesday, August 7, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] This paper presents a design methodology considering both INWE (Inverse-Narrow-Width-Effect) and RSCE (Reverse-Short-Channel-Effect) by sizing transistor's width and length accordingly to achieve close-to-most energy-efficient digital circuit design. By using a fitted and modified INWE-aware, RSCE-aware and variation-aware model, fast estimation of width, length and nf for optimum finger can be obtained. Using such method, EDP (Energy-Delay Product) optimized gates for low-power cell library in a commercial 180nm CMOS process are developed. The proposed finger-based gates have the FO4 Delay and EDP reduced by 44%~72% and 31%~76% respectively compared with conventionally sized library gates.

[Abstract] This paper presents a method for computing elementary function using optimized number of most significant bits of coefficients along with truncated multipliers for designing linear and quadratic interpolators. The method proposed optimizes the initial coefficient values, which leads to minimize the maximum absolute error of the interpolator output by using a Chebyshev series approximation. The resulting designs can be utilized for any approximation for functions up and beyond 32-bits (IEEE single precision) of precision with smaller requirements for table lookup sizes. Designs for linear and quadratic interpolators that implement $f(x) = 1/x$ are presented and analyzed, although the method can be extended to other functions. This paper demonstrates that optimal coefficient values with high precision and smaller lookup table sizes can be optimally compared to standard coefficients for interpolators.

[Abstract] In this study we present 3T and 3T1D DRAM cells designed using FinFET technology. Overall, the 3T DRAM cell has a 43.6% faster write speed than the 3T1D cell and uses less dynamic current (30.4% less write current and 14.6% less read current). The FinFET 3T1D DRAM cell offers a 16.7% faster read speed and 48.6% less read leakage current than the 3T1D cell. The 3T DRAM cell offers less variation in delays, up to 37% less than the 3T1D cell for write delay, due to parameter corner simulations. Overall for a system, the 3T FinFET DRAM cell is more promising due to its low dynamic current and significantly shorter write speed which leads to a smaller maximum delay.

Session B1P-K: Digital Circuits and Applications

Chair: Sreeraman Rajan
Time: Tuesday, August 7, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] A low-voltage folded-switching mixer is implemented in 0.25µm SOI CMOS technology. The post-layout simulation of the designed mixer at 4.5 GHz has noise figure (NF) of 9.6 dB, input IP3 of -9 dBm, conversion gain (CG) of 10.9 dB and total current consumption including bias is 4.5 mA under a 1.5V supply voltage. The designed mixer can also operate under a 1V supply voltage with relatively small linear performance degradation. The chip area is 1.1×0.6 mm2. Due to the high-resistivity silicon substrate, buried oxide isolation and low threshold voltage, SOI CMOS technology offers significant performance improvements for mixers, which makes the designed mixer well suitable for low-voltage and low-power applications.

[Abstract] Electrowetting based digital microfluidic biochips are developed recently as an alternative for conventional laboratory methods in advanced biochemical applications. Here a unique design of an automated droplet detection analyzer to be coupled with a targeted biochip is proposed for providing detailed analysis result based on the data acquired through optical detection. This newly proposed design enables the detection analysis of samples based on predefined characterized results – and enhances the process of integration of multiple biochips. The circuit, synthesis and simulation of the proposed droplet analyzer for signals from Blood oxygen analysis for multiple samples in a single biochip is displayed.

[Abstract] With power becoming a precious resource in current VLSI systems, performance per Watt has become a more important metric than chip area. With a large number of applications benefitting from support for complex functional units like squaring and cubing, it becomes imperative that such functions be implemented in hardware. Implementing these functions using existing general purpose multipliers in a design may result in area savings in some cases but results in power and latency penalties. We propose to use dedicated hardware accelerators like squaring and cubing units to perform squares and cubes, respectively. We study the trade-off for computing squares and cubes using a general purpose multiplier versus dedicated units from a software perspective. We compare area and power requirements for various widths. We are able to reduce power consumption per computation by more than 50% in squaring units and more than 40% in cubing units using dedicated units. Depending on the requirements of the applications, dedicated squaring and cubing units can also aid multipliers in improving the performance and latency of various applications.

[Abstract] In this paper, an improved fixed-point hardware design of QR decomposition, specifically optimized for Xilinx FPGAs is introduced. A Givens Rotation algorithm is implemented by using a folded systolic array and the CORDIC algorithm, making this very suitable for high-speed FPGAs or ASIC designs. We improve the internal cell structure so that the system can run at 246MHz with nearly 24M updates per second throughout on a Virtex5 FPGA. The matrix size can be easily scaled up.

[Abstract] This paper presents the nonrecursive structure for the rotated comb (RC) filter which solves the implementation problems of the original RC filter. Additionally using the polyphase decomposition it is possible to move all filtering to a low rate. The multiplierless design is included.

Session B1P-L: Digital IC Design Methods

Chair: Sreeraman Rajan
Time: Tuesday, August 7, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] This paper presents an analysis of challenges in logic-on-logic stacked two-tier 3DIC implementation of a single-precision floating-point unit, using current industry-standard CAD tools. This paper also, provides insights into where the tools require improvements to enable fully optimized 3DIC design.

Session B2L-A: Analog Design Techniques II

Chair: Vishal Saxena, *Boise State University*
Time: Tuesday, August 7, 2012, 10:10 – 11:50
Location: White Water

[Abstract] A compact low-voltage analog divider is presented. The design is based on a four-quadrant multiplier and a differential transconductance amplifier as basic building blocks operating in voltage mode. A biasing control circuit to set the dc operational point that requires very few devices and offers continuous-time operation is included. Experimental results of a test chip in 0.5µm CMOS technology verify the proposed operation.

[Abstract] This paper reports a high performance bandgap voltage reference, in which the temperature is distinguished by a simple on chip thermometer. Four similar performance bandgap references operate in different temperature ranges with high preference. Two resistors made of different materials are used to compensate the quadratic temperature, and hence to efficiently reduce the temperature drift of the bandgap voltage reference. Finally the simulation results based on 0.35µm CMOS process indicate that the temperature coefficient of the proposed reference is 300ppm during the full temperature range (-65°C~150°C).

[Abstract] In this paper, we present a low-power, small-area and programmable bandgap reference, based on the reverse bandgap reference concept. It is implemented in a 65nm digital CMOS process with 1.2V power supply. It employs two switched capacitor amplifiers to weight temperature dependent voltages with opposite polarity. Programmability is achieved by adjusting a closed-loop gain of these two amplifiers. The implemented BGR generates three reference voltages, such as 0.591V (VREF1), 0.872V (VREF2) and 1.189V (VREF3). In simulation, with +/-10% supply voltage variation, the temperature coefficient (TC) of VREF1, VREF2 and VREF3 is less than 43ppm/deg, 28ppm/deg and 33ppm/deg, respectivley, in the temperature range from -40 deg to 100 deg. The average power consumption is less than 40uW for VREF1, 60uW for VREF2 and 110uW for VREF3. The layout area (excluding bonding pads) is 200um by 190um.

[Abstract] A reliability model for electromigration-induced failure in metal interconnects under time-dependent stress is introduced. In contrast to existing reliability models that are based upon the assumption that stress is constant throughout the useful life of a system, this model includes provisions for the more realistic situation where both thermal stress and current stress are time-dependent. A single parameter which can be represented as a real number is used to incorporate the total effects of the stress history making this approach applicable for dynamic power/thermal management algorithms.

[Abstract] A new approach for identifying the number of stable equilibrium points in supply-insensitive bias generators, references, and temperature sensors based upon self-stabilized feedback loops is introduced. This provides a simple and practical method for determining if these circuits require a “start-up” circuit and, if needed, for verifying that the startup circuit is effective at eliminating undesired stable equilibrium points in the presence of process and temperature variations. This approach is demonstrated by considering the well-recognized inverse Widlar bias generator/temperature sensor as an example.

Session B2L-B: Test Methods in Digital Logic

Chair: Semih Aslan
Time: Tuesday, August 7, 2012, 10:10 – 11:50
Location: Rapids

[Abstract] Advancement of VLSI technology helps semiconductor industry to manufacture Through-silicon-via (TSV) based 3D stacked ICs (SICs). During 3D assembly, multiple partial stack tests are necessary. In this paper, we address test architecture optimization for 3D stacked ICs implemented with hard dies. We consider two different test sets and derive optimal solutions to minimize over all test time when complete stack and multiple partial stacks, need to be tested. Results are performed for two handcrafted 3D SICs comprising of various SoCs from ITC'02 SoC test benchmarks. In this work we consider the test architecture optimization for 3D SIC where the die level test architecture is fixed and each die consists of one SoC. We show that decrease in total test length with the increasing number of test pins is more than increase in the number of test TSVs. Furthermore, we also present test schedules and corresponding test lengths for every multiple insertions.

[Abstract] Over the last years the complexity of SoC's has increased enormously. This increase leads to a high test effort against faults. Therefore, methods have been developed to speed-up fault testing to cope with the increasing number of possible faults. One method is to emulate fault attacks. To cope with the large amount of test data a method to check automatically if a fault injection was successful is required. In this paper a novel method is presented how automatically, on a fault emulation platform, can be proven if a fault forces the system to unintended behavior. The PIFEA hardware block is designed to check if the system execution flow is manipulated or if the system detects the fault and switches in a secure mode.

[Abstract] As more cores are being packed on a single chip, bus-based communication is suffering from bandwidth and scalability issues. As a result, the new approach is to use a network on-chip (NoC) as the main communication platform on a SoC. NoC provides the flexibility and scalability much needed in the era of multi-cores. NoC-based systems also provide the capability of multiple clocking that is widely used in many SoC nowadays. In this paper, a simulated annealing algorithm for thermal and power-aware test scheduling of cores in a NoC-based SoC using multiple clock rates is presented. Results on different benchmarks show the effectiveness of our technique.

[Abstract] Test points provide additional control to design logic and can improve circuit testability. Traditionally, test points are activated by a global test enable signal, and routing the signal to the test points can be costly. To address this problem, we propose a new test point structure that utilizes controllability don't-cares to generate test point activation signals. By generating the signals locally, routing problems can be alleviated, thus reducing test point overhead. To support the structure, we propose new methods for extracting don't-cares in the design: one relies on design assertions and the other one identifies unused states in state machines. Our empirical evaluation on real designs shows that don't-cares exist in many designs and can be used for reducing test point overhead.

[Abstract] The importance of reliability in majority voter is due to its application in both conventional fault-tolerant design and novel nanoelectronic systems. A better understanding of signal probability, functional/signal reliability and error bound of majority voter is discussed in this paper. We analyze these parameters by boolean difference. The equations derived in this paper present the characteristics of error propagations in majority voter, and reveal the conditions that TMR (Triple Module Redundancy) technique requires. The results show the critical importance of error characteristics of majority voter, as used in fault-tolerant designs.

Session B2L-C: RF and PLL Circuits

Chair: Jose Silva-Martinez, *Texas A&M University*
Time: Tuesday, August 7, 2012, 10:10 – 11:50
Location: Ivy

[Abstract] This paper describes a dithered time-to-digital converter (TDC) design for all-digital phase-locked loops (ADPLLs). Different from other modulated TDCs, the proposed TDC employs a delay-locked loop (DLL) to achieve both noise-shaped dithering and PVT-insensitive time resolution. Simulation results show that the proposed TDC significantly improves the fractional spur performance even with TDC nonlinearity considered. The TDC designed in 65nm CMOS occupies an area of <0.06mm² and consumes 2.2mW.

[Abstract] In this paper, we presents a low-spur phase locked loop (PLL) system for wireless applications. The low-spur frequency synthesizer randomizes the periodic ripples on the control voltage of the voltage-controlled oscillator (VCO) in order to reduce the reference spur at the output of the PLL. A new random clock generator is presented to perform a random selection of phase frequency detector (PFD) control for charge pump at locked state. The proposed frequency synthesizer was fabricated in TSMC 0.18-µm CMOS process. The PLL has achieved the phase noise of -105 dBc/Hz at 1MHz offset frequency and reference spurs below -72dBc.

[Abstract] This paper investigates phase jitter in an ultra-low power Phase-Locked Loop (PLL). Expressions for the cycle-to-cycle jitter caused by the ramp current noise as well as the voltage noise present on the two rails of the sawtooth are derived. The theoretical results reveal that the current noise establishes a lower bound for jitter. The PLL has been fabricated in 0.5 um CMOS technology and targets an output range of 10-150 kHz. The integrated circuit dissipates between 0.8-1.8 uW of power (Vdd=3 V) and yields relative phase jitter values between 0.11% and 0.14%.

[Abstract] In this work, we present a NMOS-switch high-swing cascode charge pump. The proposed design utilizes high-swing cascode current mirror to improve output current matching and a pull-up/pull-down mechanism to remedy the slow-node issue of a classic NMOS-switch current steering charge pump. The proposed NMOS-switch high-swing cascode charge pump has been designed using the IBM 0.13um CMOS technology. Simulation results show that the proposed charge pump design features much improved output current matching and also eliminates the slow-node problem when compared to original approach.

[Abstract] A calibration technique for compensation of the generated phase error at the band hopping instant is proposed for a fast-hopping DLL-based injection-locked frequency synthesizer for WiMedia UWB band group #1. This technique makes the accuracy of the phase error compensation immune to process variations and so the VCDL nonlinearity. Simulated in 65-nm CMOS technology, the average synthesizer hopping time is 4 ns for all process corners. The phase noise performance at 1 MHz offset from 4488 MHz carrier is -121 dBc/Hz and the adjacent spur level from the Monte Carlo simulation is -37 dBc. Excluding the CML divider, the synthesizer consumes 7.7 mW from a 1.2 V supply.

Session B2L-D: Control Systems, Mechatronics and Robotics

Chair: Kumar Yelamarthi
Time: Tuesday, August 7, 2012, 10:10 – 11:50
Location: Clear Water

[Abstract] This paper describes a radio frequency identification (RFID) and sonar-guided tour guide robot, CATE (Central's Automated Tour Experience), an embedded system equipped with an RFID reader for localization, and sonar and IR sensors for obstacle detection and avoidance. CATE can guide the visitor through a predefined tour of the building, or create a new route on-the-fly. While in predefined tour mode, CATE completes the tour by avoiding obstacles using sonar and infrared sensor input. It will also provide audio and video information through an onboard computer, and can collect feedback from the user through a touch screen display. It has been successfully implemented and is under final stages of testing.

[Abstract] In this paper we present a methodology for the development of a circuit to control the reading frequency of a First In First Out (FIFO) memory based on the monitoring of its filling level, with applications in data communication protocol justification architectures for tributary signal mapping and demapping.

[Abstract] Control of miniature mobile robots in unconstrained environments is an ongoing challenge. Miniature robots often exhibit nonlinear dynamics and obstacle avoidance introduces sigificant complexity in the control problem. Furthermore, miniature robots have strict power and size constraints, drastically reducing on-board processing power and severely limiting the capability of digital implementations of nonlinear model predictive controllers. To accommodate the demands of this application area, we describe the architecture of a mixed-signal mobile robot control system using randomized receding horizon control. We compare the proposed mixed-signal implementation with purely digital control systems in terms of power requirements and precision and find that the mixed-signal implementation offers significant reductions in power consumption at an acceptable loss of precision.

[Abstract] Electrostatic loudspeakers (ESLs) are capable of very low distortion and have desirably flat frequency response within the audio frequency range. In this paper, a novel approach is proposed for audio amplification using a high-voltage direct-digital solid-state class-D amplifier as a method that replaces impedance matching ESL audio transformers. Optical coupling is used to achieve isolation from the high-voltage side. The proposed stacked MOSFET output stage provides a solution to the voltage swing limitations of the available switching power MOSFETs. An example digital amplifier having 14-bit ADC precision PWM with fc = 50 kHz was implemented at 750 V delivering 28W into Ra =20kOhms;. The digital modulator was realized on a Xilinx Virtex4 Sx35-10ff668 at Fs = 100 MHz clock.

[Abstract] In this paper an extended geometric concept of nonlinear electronic circuits with fast switching behavior, i.e. with jumps in their state space, is given. Furthermore the developed geometric approach is adapted to MNA based systems of equations. This new method enables the simulation of such ill-conditioned circuits without regularization and presents an implementation approach for common circuit simulators like SPICE.

Session B2L-E: Invited Session III

Chair: Jose M. de la Rosa, *Institute of Microelectronics of Seville, IMSE-CNM (CSIC/University of Seville), Spain*
Time: Tuesday, August 7, 2012, 10:10 – 11:50
Location: River Fork

[Abstract] Printed electronics is an emerging technology that would likely complement conventional silicon-based electronics in numerous applications. In this paper, we review the different printing/patterning technologies for realizing printing electronics, and the major challenges thereof are delineated. We discuss why printed electronics based on Additive processing (fully-printed) has higher potential for ubiquity than Subtractive processes (non-fully printed). We present our printing process based on fully-printed screen printing, and the characteristics of the ensuing printed transistors and an op-amp. Of specific interest, to the best of our knowledge, the carrier mobility of our fully-printed transistor is the fastest of all reported full-printed transistors, and the fully-printed op-amp is the first fully-printed circuit.

[Abstract] The aim of this contribution is to show why sources of non-idealities are actually a concept of reason in order to define tradeoffs in the design of analog circuits. A tradeoff is commonly picked up from an analytical design-model, which tries to explain a phenomenon under study using physical theories underlying the role of non-idealities in the design of accurate analog-circuits. Since accuracy is commonly used as a measure rule for minimizing the unwanted effect of non-idealities on the circuit performance, this paper underlines that non-idealities reported in open literature shown that any analog circuit is designed in a custom way, where just some idealities are minimized in order to fulfill specific design specifications, i.e. sources of non-idealities do not necessarily include all existing ones but those affecting the circuit's performance.

[Abstract] This paper presents an overview of the co-design technique for broadband RF ESD protection circuit designs. The unique mixed-mode ESD simulation design methodology allows full-chip design optimization and prediction of broadband RF ICs with full low-parasitic ESD protection, which were validated experimentally using ultra wideband (UWB) RF ICs and RF switch circuits in CMOS technologies.

[Abstract] Currently embedded system design is more an art than a science, lacking adequate support for sound top-down design, significant co-design, and effective integration of nonfunctional properties such as cost, reliability, security, and safety into the design process. We describe a top-down design process which employs constraint graphs to address these issues. We demonstrate the effectiveness of this method through the development of a family of designs for a camera.

[Abstract] Advancements in silicon photonics technology are enabling large scale integration of electro-optical circuits and systems. To fully exploit this potential, automated techniques for design space exploration and physical synthesis for integrated optics must be developed. This paper investigates how conventional VLSI physical design automation techniques can be adapted for integrated optics applications. We present an overall methodology for cell-placement, global routing, and detail routing for physical synthesis of optical circuits. In addition, we highlight optics-specific constraint models, design rules and optimization criteria that will have to be accounted for in physical design automation.

Session B3L-A: Analog Design Techniques III

Chair: Vishal Saxena, *Boise State University*
Time: Tuesday, August 7, 2012, 13:10 – 14:50
Location: White Water

[Abstract] A design method for an over-10G-b/s buffer circuit for generating precise delay is proposed. A simple small-signal equivalent circuit model is introduced to investigate the delay characteristics of a current mode logic (CML) buffer circuit with load resistances. By setting the transconductance generator gm and output resistance in a MOSFET model as a function of drain current, the design equations for the delay and gain are derived. To confirm the validity of the design method, we fabricated buffer chain IC with the 65nm-MOSFET process and compared the measured and estimated delay. The agreement between the measurements and calculations is good enough, confirming the validity of the method.

[Abstract] This paper presents a bias technique for IM3 null tracking in bipolar amplifiers which is insensitive to temperature, supply voltage, and component variation. Theory, design concepts, and simulations are provided to show this bias circuit can accurately track the IM3 null. The technique is applicable for a range of bipolar BiCMOS technologies, and has potential application in amplifiers where high IP3 is required with a moderate noise figure.

[Abstract] This paper presents a new low-power, low-voltage Resistance-to-Period Converter (RPC) for signal conditioning of resistive sensors whose equivalent resistance varies in more than one decade. Designed in a low cost 0.18µm CMOS process, the proposed RPC attains a good compromise between linearity and power consumption, which makes it suitable for portable applications. Simulation results show that the linearity error is less than 1.6% for an input resistance range from 10k Omega; to 100k Omega; with power consumption lower than 46µ W at 1.2 V supply.

[Abstract] This paper presents a novel architecture of ultra-low offset comparator latch using on-chip calibration to compensate the process variation. The proposed technique compensates the variation in process parameters such as W/L, uCox and threshold voltage independently by considering the intrinsic behavior of the MOS transistor. Monte Carlo post-layout HSPICE simulations were carried out with 100 runs to evaluate the performance of the comparator latch. Experimental results show that when comparing with state-of-the-art pre-amplifier-less architectures, the standard deviation of the input voltage offset is reduced by more than 75% over a range of 400mV difference of the common mode input voltage.

[Abstract] Motivated by emerging meandering winding magnetometer (MWM) array based Non-Destructive Evaluation (NDE) applications, this paper presents a new approach for on-chip inductive impedance measurement to enable MWM-array applications to be happened in field, in real-time, and during targets' operation. Different from state of art solutions which rely on high precision analog processing functions to achieve high accuracy, the proposed approach innovatively incorporate bridge circuit, feedback, and resonance concepts to achieve impedance measurement on a single chip. Behavior level simulation demonstrated the measurement algorithm and feasibility of the proposed method.

Session B3L-B: Design Trends in Programmable Logic

Chair: Manuel Jimenez, *University of Puerto Rico at Mayaguez*
Time: Tuesday, August 7, 2012, 13:10 – 14:50
Location: Rapids

[Abstract] This paper presents a novel design of a Configurable Logic Block (CLB) for a Field Programmable Gate Array (FPGA) based on a computing scheme in nanoscale technology called the Quantum-dot Cellular Automata (QCA). In QCA technology, the cells made of quantum dots transmit information from one cell to the other based on Coulombic repulsion between the electrons. The main goal behind the design of the CLB is to ultimately design a miniscule nano FPGA without transistors for the 'beyond CMOS era' of the 2020s.

[Abstract] This paper proposes a rolled architecture for the implementation of the 128 bit AES (Advanced Encryption Standard) algorithm. The design comprises of modified T-boxes. The efficient utilization of area and the increase in speed up to 1.454 Gbps is achieved on Xilinx's Virtex-4 Field Programmable Gate Array (FPGA). The clock frequency of the design is 113.63 MHz. Reduction in terms of memory is achieved by using 24 bit words instead of 32 bits words in T-boxes. The design employs BRAMs available on the device for T-Boxes and round keys generated in the Key expansion module. The latency achieved is 10 clock cycles and for every new key same amount of clock cycles are required before start of encryption.

[Abstract] In the presence of process variation, conventional worst-case timing analysis is no longer able to fully realize the benefit of scaling and integrating. As a result, statistical static timing analysis (SSTA) is essentially needed in high-level synthesis (HLS) stage. This paper presents the first work to develop a design framework of SSTA for HLS based on transparent latches. An integer linear programming-based formal approach is provided to simultaneously solve scheduling and functional unit binding to minimize the scheduling length while meeting the timing-yield requirement. Experiments demonstrate the effectiveness of the proposed approach.

[Abstract] Thermal hotspots are a destructive phenomenon occurring in contemporary microprocessors. High power density of microprocessors and excessive use of certain microprocessor components by applications are considered the primary causes of increased temperature. Dynamic Thermal Management Techniques used in mitigating excessive temperatures results in throttling of clock speed, which degrades the performance of the microprocessor. In this paper we propose a simple but novel technique to reduce hot spots in microprocessors. We propose to lower the power density of selected high temperature components by increasing the chip area of that component. We select thermally susceptible components that have small footprints and increase the area of such components, thereby reducing the occurrence of hotspots. The overall chip area increase is minimal and our research has shown that the associated delay penalty is negligible.

[Abstract] Magnetic Tunnel Junction devices represent state in the form of a magnetic field that is accessed as a resistance. Read circuits are needed to sense this state and to produce a digital logic voltage output. We designed a resistance-to-voltage read circuit for this purpose. This paper presents area, transient response, power, and jitter characterizations in a 3M2P 0.5um process and compares these results to a second implementation in a 5M1P 0.18um process. We then evaluate the quality of phase measurements between read circuits for assessing clock skew in systems that use magnetic global clocking.

Session B3L-C: Linear/Non-Linear Circuits I

Chair: Miguel Velez
Co-Chair: Arturo Sarmiento-Reyes
Time: Tuesday, August 7, 2012, 13:10 – 14:50
Location: Ivy

[Abstract] This paper presents a low voltage adjustable CMOS Schmitt trigger using DCG-FGT transistor. Simple circuit is introduced to provide flexibility to program the hysteretic threshold in this paper. The hysteresis can be controlled accurately at a large voltage range. The proposed Schmitt trigger has been designed using 90nm 1.2V CMOS technology and simulated using Eldo with PSP device models. The simulation results show rail-to-rail operation and independently adjustable switching voltages VTH- (low switching voltage) and VTH+ (high switching voltage).

[Abstract] This paper presents a design methodology for a low-frequency oscillator which consists of a current-starved (CS) voltage-controlled oscillator (VCO) and a frequency divider. The frequency divider is used to reduce frequency in an area efficient manner. We derive a model for the effective capacitance of a CSVCO so that design tradeoffs between area, power, and phase noise can be readily explored. The methodology supports optimization over these performance metrics, with adjustable weighting factors that emphasize their relative importance. Design examples in 0.5µm CMOS technology with 3.3 V supply are presented.

[Abstract] This work presents an analysis of digital predistortion (DPD) architectures for RFDAC based direct digital to RF transmitter (DRF). The nonlinearity of the DRF frontend is determined by circuit simulation. Direct learning and indirect learning structures using least mean square (LMS), normalized LMS (NLMS), and recursive least square (RLS) estimation algorithm are evaluated with respect to the lowest normalized mean square error (NMSE) and the error vector magnitude (EVM) and spectral emissions when processing broadband OFDM based IEEE 802.11a (WLAN) signals. MATLAB simulations show the possibility to reduce out-of-band emissions by 8dB, the best EVM with predistortion is 2.50%, the EVM without predistortion is 4.27%. Afterwards, the impact of quantization and delay is evaluated showing a strong dependence of the resulting EVM from the delay in a digital circuit.

[Abstract] Chaos synchronization is an important research topic in the field of nonlinear circuits and systems. This paper presents a new synchronization scheme, where two chaotic discrete-time systems synchronize for any invertible scaling matrix. Specifically, potentially different linear combinations of response system states synchronize with each drive system state. The proposed observer-based approach presents some useful features: i) it enables exact synchronization to be achieved in finite time; ii) it exploits a scalar synchronizing signal; and iii) it can be applied to a wide class of discrete-time chaotic (hyperchaotic) systems. An example is reported, which shows that exact synchronization is effectively achieved in finite time, for two arbitrary scaling matrix, via a scalar synchronizing signal only.

[Abstract] The paper gives a critical analysis of recently proposed cut-insertion theorem. It is shown that all cut-insertion equivalent networks can be obtained using a simple extension of the substitution theorem. For example, using two voltage sources connected in parallel between a chosen and reference node, then cutting the wire between the voltage sources one concludes that a wire with a known voltage and known current can be substituted by a two port where one input is connected to the impedance seen by the voltage source operating at the second port. The calculation of this impedance is difficult; in the general case one have to solve an algebraic equation of the fifth degree. Hence, when the network with cut-inserted two-port is represented as a feedback system the parameters of this system may be defined for very simple networks only, when the degree of the defining equation is lessened. An example shows these difficulties.

Session B3L-D: Pattern Recognition

Chair: Hector Perez-Meana
Co-Chair: Hua Tang
Time: Tuesday, August 7, 2012, 13:10 – 14:50
Location: Clear Water

[Abstract] In this work, emotion-inspired age and gender recognition systems are developed. In the beginning, speakers' utterances with emotions of angry, happy, calm and sad are analyzed to identify their ages and genders where the recognition engine adopts a Support Vector Machine (SVM). According to the experimental results, the accuracies of the age and gender recognitions under a low arousal emotion tend to be worse and better than those under a high arousal emotion, respectively. In practical applications, a specific emotion may not appear in a speaker's utterance. Hence, according to the emotional arousal intensity, speech frames of a speaker's utterance are classified into two groups which are above and below the mean of arousal intensities of speech frames. After that, the age and gender recognitions are conducted at speech frames with higher and lower arousal intensities. Our experiments reveal that the proposed emotion-inspired age and gender recognition systems can be better that those without considering arousal intensities by 8.5% and 9.5% improvements, respectively.

[Abstract] Facial recognition using spatial domain Diagonal Principal Component Analysis (DiaPCA) algorithm produces better recognition accuracy compared to the Two Dimensional PCA (2DPCA). Transform Domain – 2DPCA (TD2DPCA) retains the high recognition accuracy of the 2DPCA while considerably reducing storage requirements and computational complexity. In this work, the Transform Domain PCA implementation of the DiaPCA (TDDiaPCA) is presented. All the test results, for noise free and noisy images, consistently confirm the considerable storage and computational savings for different spatial domain pre-processing scenarios while retaining the high recognition rate. The performance is evaluated using ORL, Yale and FERET databases. Sample results are given.

[Abstract] Face detection and recognition has been introduced in many real world applications. Several algorithms have been implemented for either detection or recognition. In this paper, a novel algorithm, which simultaneously detects and recognizes facial images employing the same method, is presented. The proposed algorithm is based on a new 2D representation for the Histogram of Oriented Gradients (2D-HOG) in conjunction with 2DPCA for feature extraction. Experimental results conducted on existing datasets, FERET, ORL, UMIST, JAFFE, and MIT-CMU dataset, achieved better accuracy and running time compared with existing techniques

[Abstract] In this paper, we present an approach to estimate camera intrinsic and extrinsic parameters for roundabout traffic scenes. Unlike many previous works on camera calibration for roadway scenes based on the parallel line method, our work addresses camera calibration at roundabout scenes by using a circle. The proposed method can estimate tilt angle, focal length, and camera height by matching the ellipse equation extracted from an image with the perspective-transformed equation of the corresponding circle. The pan angle is not required in our method and only one image is needed for camera calibration. The method is validated with real world roundabout traffic scenes and the results are comparable to those from the parallel line method in terms of accuracy.

Session B3L-E: Special Session III: Performance Drivers in CMOS Transceiver Designs

Chair: Ranjit Garpurey, *University of Texas at Austin*
Time: Tuesday, August 7, 2012, 13:10 – 14:50
Location: River Fork

[Abstract] This paper presents low-power design techniques for wideband LNA's and wide-tuning frequency generation circuits operating at mm-wave. Transformer neutralization techniques enable the design of current-reuse and low-voltage LNA's. Transformer-based VCO's with resonance mode switching are introduced to achieve very wide tuning range. The design and characterization of several prototype circuits is presented to validate these concepts.

[Abstract] One emerging trend of implementing phase locked loop (PLL) based frequency synthesizers is to leverage digital signal processing in the loop filtering for more flexibility, scalability and smaller silicon area. This paper examines the pros and cons of such digital-intensive PLL architecture, and discusses techniques to minimize its overhead in terms of implementation cost and performance degradation. A hardware prototype in 65nm CMOS that synthesizes frequencies over 600-800 MHz is shown to prove the effectiveness the proposed overhead minimization techniques.

[Abstract] Stacked-FET PAs have emerged as a promising circuit technique for high-power CMOS PAs at millimeter-wave bands. A common-source and a 3-stack PA realized in 45-nm CMOS SOI is compared at 45-GHz. The saturated output power increases from 10 dBm to more than 18 dBm respectively for 1- and 3-stack PAs. Compression and EVM/ACP measurements for QAM modulation are presented to discuss the linearization requirements of millimeter-wave stacked-FET PAs.

[Abstract] A CMOS PA system intended for long-distance sensor communication is presented. The PA utilizes a dynamic-VDD and operates directly off of a super-capacitor energy-storage element, obviating the need for a voltage regulator. A power-combining PA impedance scaling approach has been implemented to eliminate energy loss from a high-current voltage regulator. The device integrates a 2-to-1 power combiner with a set of pre-drivers and an output stage. The PA monitors the output power, and digitally modulates the PA load impedance. The entire power control loop is integrated in a 90nm, 9-metal-layer TSMC process and delivers 24dBm of output power at 1.9GHz, making it suitable for sensor data communication over distances of several hundred meters. During a TX-burst, the PA VDD varies from 2.5V to 1.4V, while the power control loop maintains constant output power with an accuracy of 1.6dB.

[Abstract] Recent advances in ADCs have enabled the development of low power receivers for wireless communication applications. In this paper we will discuss a specific class of ADCs, namely sigma delta ADCs. A brief overview of challenges in the design of these ADC's will be discussed along with the recent advances in overcoming these challenges. Two specific examples in the context of wide and narrow bandwidth systems will be discussed that demonstrate the viability of the recent techniques each ADC achieving best in class figure of merit in their respective bandwidths.

Session B4P-F: Analog and Mixed-Signal Circuits VII

Chair: Jose Silva-Martinez, *Texas A&M University*
Time: Tuesday, August 7, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] A new KHN filter employing two OTAs two grounded capacitors and one resistor is proposed. The q and cutoff frequency of the filter are orthogonal and the cutoff frequency can be tuned without changing the passive components. The results are verified by spice simulations.

[Abstract] Design and simulated results of a fully integrated 5-GHz CMOS LNAs are presented. To design these LNAs, the parasitic input resistance of a MOSFET are converted to 50 Omega; by a simple L–C network, hence eliminating the need for source degeneration. As it is analytically shown, this is because the former methods enhance the gain of the LNA by a factor that is inversely proportional to MOSFET's input resistance. By employing the folded cascode technique, the proposed LNA can operate at a reduced supply voltage, high gain and ultra power consumption. The proposed LNAs deliver 3 dB power gain more than conventional folded cascode, while consuming 1.3 mW dc power with an ultra low supply voltage of 0. 6V.

[Abstract] This paper presents a novel bias circuit for achieving process and temperature invariant resistor using a MOSFET operating in triode region. The proposed circuit comprises of an enhanced process tracking circuit and complementary to absolute temperature (CTAT) voltage generators. The proposed circuit has been designed and optimized in 180nm mixed-mode CMOS technology. Exhaustive Montecarlo simulations show that the ON resistance of the MOSFET (RON) varies only by ± 7.6 with process and ± 1.2 with temperature ranging from 0°C to 100°C. The proposed bias circuit reduces variation in (RON) by a factor of 3.4 as compared to a fixed bias MOSFET. The proposed circuit consumes 130µW power.

[Abstract] A voltage mode Field Programmable Analog Array (FPAA) is presented in this paper. The FPAA is an array consisting of 30 Digitally Programmable Second Generation Current Conveyors (DPCCII-). The FPAA is made from seven configurable analog blocks (CABs) formed with DPCCII-. The CABs are directly connected to each other through direct wiring. This direct wiring methodology is realized because the DPCCII-outputs can be set to zero using a three-bit digital codeword. The FPAA is realized using 90nm CMOS technology model. The standby DC power consumption of the FPAA is 72.3mW from balanced supply voltage ±0.5V. A tunable second order universal filter is realized using the proposed FPAA. The filter cutoff frequency is tuned from 2MHz to 3.5MHz.

[Abstract] In this paper, two types of a soft error hardened 10T SRAM cells with high static noise margin (SNM) are proposed for low voltage operation. The proposed NMOS stacked SRAM cell operates normally with higher read SNM near to sub-threshold region compared to prior works. Simulated results using 0.18um standard CMOS process demonstrate that proposed NMOS stacked-10T cell has high read SNM and high soft error resilience of at least 100 times higher than unprotected standard 6T SRAM cell for a single event transient (SET).

Session B4P-G: Analog and Mixed-Signal Circuits VIII

Chair: Teresa Serrano Gotarredona
Time: Tuesday, August 7, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] This paper presents a differential amplifier design with gain enhancement using positive feedback. Comparing with the standard complementary metal-oxide-semiconductor (CMOS) differential amplifier, the new circuit has improved specifications, such as higher small-signal voltage gain, output voltage swing, and large bandwidth. In addition, the circuit has a built-in tuning capability for adjustable gain or tuning out the process-voltage-temperature (PVT) variations. This paper also presents a comparison of noise and power dissipation that was performed using Spice simulation.

[Abstract] Two fully integrated low noise amplifiers using gm-boosting technique for ultra-low voltage and ultra-low-power GPS applications are designed and simulated in a standard 0.18µm CMOS technology. By employing the folded cascode and forward body bias technique, the proposed LNAs can operate at a reduced supply voltage and power consumption. The proposed LNA delivers a power gain (S21) of 17.6 dB with a noise figure of 3 dB, while consuming only 1.1mW dc power with an ultra low supply voltage of 0.45 V. A gm-boosting technique is used for increase the LNA gain and reduce noise figure at the cost of a little circuit power consumption for the LNA with a gm-boosting, a remarkable gain of 20.8 dB gain is achieved with a dc power of 1.3 mW and noise figure 2.9dB. The supply voltage figure of merit(FOM1) and the tuning-range figure of merit(FOM2) are optimal at 46.22 dB/V and 9.61(v.mw)-1 for gm-boosting technique, respectively.

[Abstract] In this paper we present the fixed expansion layer (FEL) feedforward neural network designed for balancing plasticity and stability in the presence of non-stationary inputs. Catastrophic interference (or catastrophic forgetting) refers to the drastic loss of previously learned information when a neural network is trained on new or different information. The goal of the FEL network is to reduce the effect of catastrophic interference by augmenting a multilayer perceptron with a layer of sparse neurons with binary activations. We compare the FEL network's performance to that of other algorithms designed to combat the effects of catastrophic interference and demonstrate that the FEL network is able to retain information for significantly longer periods of time with substantially lower computational requirements.

[Abstract] In this work we model single photon avalanche diodes (SPADs) as communication channels. We apply classical shannon results for a Gaussian channel to typical SPAD circuits. Thus we look at the information rate and the bit energy of the circuit. By considering the noise sources for a generic SPAD sensor we develop the information rate model as a function of the excess bias voltage and perimeter gate voltage. We find that when considering only the dark count rate that there is a single optimum excess bias voltage that gives the maximum information rate. We conclude there is an excess voltage, gate voltage pair that optimises the information rate.

Session B4P-H: Linear/Non-linear CAS

Chair: Arturo Sarmiento-Reyes
Time: Tuesday, August 7, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] The paper considers a new class of filters with transfer functions using the polynomials introduced by the British physicist Sir G.G. Stokes. The filters are transitional between Bessel and Butterworth ones. When one compares the step-responses of Bessel, Stokes, and Butterworth filters of the same order and the same -3dB bandwidth then the result is following. The Bessel filters have a certain delay and (practically) no overshoot in their step-transient response. The Stokes filters have larger delay than Bessel filters and a small overshoot. Finally, the Butterworth filters have largest delay and largest overshoot. The paper illustrates these properties and describes the data required for synthesis of the Stokes filters.

[Abstract] This paper presents a highly-linear, low power, low noise amplifier (LNA) using a novel nonlinearity cancellation technique by employing the folded cascode topology. The circuit functionality is analyzed using Volterra series analysis. The linear LNA was designed and simulated in a TSMC 0.18µm CMOS process at 5GHz frequency. By employing the new technique, the IIP3 is improved by more than 14dB compare to conventional folded cascode LNA reaching to +1dBm without any significant effect on the other LNA parameters. The proposed LNA also delivers a voltage gain (S21) of 12.4 dB with a noise figure of 3.9 dB, while consuming only 1.27 mW dc power with a low supply voltage of 0.6 V.

[Abstract] Loop Gain in analog feedback circuits is used to define stability of the design. The usual approach opens the loop, a process likely to lead to approximate results that remain un-quantified due to improper handling of loading and feed-forward effects. In this paper a new approach is outlined using driving point impedance and signal flow graphs that fully accounts for these effects and showing a symmetrical, dual loop result.

[Abstract] This study presents an efficient approach to compute the DWT transform with Adaptive Load Balancing Algorithm (ALBA) which is applied on standard form on parallel general-purpose computers. This technique does not introduce any restriction on the size of the input data or on the transform parameters. Complete use of the available processor parallelism, modularity, and scalability are achieved. Theoretical and experimental evaluations and comparisons are given with respect to traditional parallelization. In this work, wavelet transform is implemented on a single core/multi-core system and developed in C# using .Net framework 4.0.

Session B4P-J: RF, Microwave, and Optical/Photonic Systems

Chair: Robert Hay, *Boise State University*
Time: Tuesday, August 7, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] A method for effective synthesis of multiple downconversion local oscillator (LO) frequencies within a harmonic rejection mixer (HRM) is presented that employs principles similar to direct digital frequency synthesis. The proposed method reduces the tuning range required of the downconversion oscillator in broadband applications. A passive HRM that implements the proposed LO synthesis method and is robust to both gain and phase mismatch is designed in 130 nm CMOS and covers the 48-860 MHz band with a master clock frequency of 0.77-1.72 GHz. Based on Monte Carlo simulations, while considering device mismatches over a 3 spread, harmonic rejection better than 63 dB is observed for all selectable LO frequencies.

Session B4P-K: Bioengneering II

Chair: Esther Rodrigez-Villegas
Time: Tuesday, August 7, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] Trends in the medical industry have created a growing demand for implantable medical devices. In particular, to provide doctors a means to continuously monitor biometrics over long time scales. To make medical implants more attractive, there is a need to reduce their size and power consumption. Small medical implants would allow for less invasive procedures, greater comfort for patients, and increased patient compliance. This work investigates how to reduce the amount of data needing to be both acquired and transmitted thereby alleviating the demand on the energy source through two techniques. The first is to employ compressive sampling to sample slower than the Nyquist rate. Leveraging the fact that tremor data is sparse in the frequency domain, we can implement the CS technique before the ADC to save energy and decrease the size of the memory. The second technique is to use adiabatic charging of the capacitors contained in the SAR ADC.

[Abstract] In this paper we present a far field RFID front end for smart biological sensing consisting of RF to DC converter, Low Drop Out regulators (LDO) which provides supply for control and signal conditioning, the Phase Lock Loop (PLL), demodulator and modulator for effective communication. The RF front harvests up to 42μW at -3dBm, the clock data recovery PLL consumes 2.86μW providing a systems clock of 5.12MHz.

[Abstract] This paper presents a low power circuit design for an electronic nervous system composed of central pattern generator (CPG) to control a biomimetic robot that mimics the lamprey swimming system. The circuit has been designed using 65nm CMOS technology model at 0.8V supply. The design challenges of narrow voltage design margin and high sensitivity to parameter variation are addressed by circuit optimization techniques as well as amplitude and time parameter scaling. The electronic CPG consists of electronic neurons connected through electronic synapses, where the behaviors of the neuron and synapse adopt Hindmarsh-Rose (HR) dynamics to replicate biological neurons and a first order chemical synapse model is utilized to achieve active synapses. The simulation results validate the electronic CPG performance at 0.8V supply voltage with parameter variation tolerance of 5% dissipating 3.28mW. The die size of the chip is 1.1mm2 including I/O pads.

Session B4P-L: Power Electronic Converter Modeling and Simulation

Chair: G.R. Branner
Time: Tuesday, August 7, 2012, 14:50 – 16:00
Location: Poster Area

[Abstract] In this paper a modeling method is investigated that finds the non-linear equation parameters of a photovoltaic (PV) module in order to obtain the desired PV model using any circuit simulator. This modeling method adjusts the I-V curve at three remarkable points: the open circuit voltage, the short circuit current, and the maximum power point [1]. Three models are realized using this technique namely, the single-diode model, the two-diode model, and the three-diode model. The evaluation study of the accuracy of these three models showed relative errors ranging from 32% to 50%. Further, this technique is improved by adjusting the I-V curve at more than three points depending on the number of unknowns to be found for each model, which showed a reduction in the relative error ranging from 0.37% to 38%. Finally, a study of the parameters obtained from the modeling algorithm on the performance of the proposed single-diode model is presented.

[Abstract] This paper proposes high accuracy modeling approach for photovoltaic (PV) arrays. The I-V characteristic of PV cell is described by nonlinear equation that's complicated to be solved by the ordinary mathematical methods. The main theme of this contribution is to use a robust algorithm to solve for all single diode model parameters. This technique uses two adjustment steps depending on comparing modeling results to the experimental data provided by the commercial datasheets. Based on the single-diode model, the parameters are determined in the sense of minimum model error. The proposed model is then validated with experimental data of Solarex MSX60 solar module. The superiority of this technique is proved by computing the absolute errors to have a maximum error as 1.3% of module short circuit current. Finally, the proposed model is used to study the effect of different parameters variations on the PV module.

[Abstract] In this paper we show two different schemes to implement a field programmable circuit that can connect n capacitors as a charge-pump of, eventually, any topology and switching pattern. Capacitor connectivity is configured by means of registers that control multiplexers that, in turn, select the phase signal that controls each switch. It is also shown that, with any of these schemes, dynamic configuration of the circuit may be achieved by simply adding additional control phases.

[Abstract] As Network-on-Chip (NoC) architectures become more relevant, research into emerging technologies to replace power hungry metallic interconnects has become critical. We propose a practical wireless architecture called GLOW, a global wireless interconnect for NoCs. With our ultra-low power transceivers centered at a 100 GHz carrier frequency, we present a wireless topology with a maximum bandwidth of 80 GHz. Both frequency and spatial division multiplexing (FDM and SDM) are used in GLOW on a near-term 64-core architecture. We are able to achieve a power savings up to 56% compared while improving speedup by 2.1x on average on real benchmarks.

Session B5L-A: Sigma-Delta Modulators

Chair: Jose Silva-Martinez, *Texas A&M University*
Time: Tuesday, August 7, 2012, 16:00 – 17:40
Location: White Water

[Abstract] A 1 GS/s Continuous-time Delta-Sigma modulator (CT- M) with 31 MHz bandwidth, 76.3 dB dynamic range and 72.5 dB signal-to-noise is reported in a 0.13 m CMOS technology. The design employs an excess loop delay (ELD) of more than one clock cycle for achieving higher sampling rate. The ELD is compensated using a fast-loop formed around the last integrator by using a sample-and-hold. Further, the effect of this ELD compensation scheme on the signal transfer function (STF) of a feedforward CT- architecture has been analyzed and reported. In this work, an improved STF is achieved by using a combination of feed-forward, feed-back and feed-in paths and power consumption is reduced by eliminating the adder opamp. This CT- M has a conversion bandwidth of 31 MHz and consumes 34 mW from the 1.2V power supply. The relevant design trade-offs have been investigated and presented along with simulation results.

[Abstract] In this paper, an approach for decreasing the area and power consumption of an integrated transmission line sigma delta modulator (ITLSDM) is presented. The architecture is based on complementary-cross-coupled bandpass filter (C-BPF) with an auxiliary negative transconductance (ANG). A closed form formula is derived to specify the characteristics compared to a SDM based on NPN cross-coupled bandpass filters (N-BPFs). The matching requirements for the loop transmission lines are relaxed by using C-BPFs. The simulation results for a 4th order BP-ITLSDM realized in a 0.25um BiCMOS technology show a reduction of 53% in the current consumption and 46% in the die area of a resonator compared to the N-BPF method. The improvement factor is more obvious for higher order BPSDMs.

Session B5L-B: Communications and Hardware Implementations

Chair: Hao Chen, *Boise State University*
Time: Tuesday, August 7, 2012, 16:00 – 17:40
Location: Rapids

[Abstract] This work discusses a scalable hardware implementation of the Pease FFT algorithm, in which structural regularity from the Kronecker formulation is exploited to perform a complete folding of the transform. An address generator approach is proposed for both data permutation and phase factor scheduling throughout the stages. In this article we briefly review the Pease algorithm in Kronecker products, remarking its regularity. Then we explain how the algorithm was mapped onto hardware. A particular implementation on an FPGA target is described analyzing its resource consumption and computation speed perspectives.

[Abstract] This work presents a novel signal processing algorithm framework for the FPGA implementation of the discrete ambiguity function which is used as a tool for the modeling and simulation of randomly time-variant linear channels in multiple input multiple output, orthogonal frequency division multiplexing, communication systems applications. The discrete ambiguity function was implemented using, both, a Xilinx IP core for the efficient computation of the discrete Fourier transform, and a new scalable implementation of the Pease FFT algorithm which takes advantage of structural symmetries and regularities exhibited in the FFT formulations when presented in Kronecker products form. Important results show that this new scalable core outperforms the Xilinx IP core when it comes to latency and number of slices used.

Session B5L-C: Special Session V: Future Applications in Communications, Signal Processing, and Networking

Chair: Yong-Moon Chung, *Yonsei University*
Time: Tuesday, August 7, 2012, 16:00 – 17:40
Location: Ivy

[Abstract] Machine-to-machine (M2M) communication between devices has significant differences with conventional human-to-human (H2H) communications. M2M-based features offer a new paradigm for future communication and network services, and can enable various convergence services in support of ubiquitous businesses and complex manufacturing industries. In this paper, a summary on the progress of global M2M standardization is presented. This paper also introduces M2M technical issues and discuss on the necessity of M2M vertical handover (VHO) and technical requirements in support of M2M VHO and fast handover for proxy mobile IPv6 (FPMIPv6) VHO between heterogeneous M2M protocol networks to enable end-to-end M2M network connectivity.

[Abstract] The tendency over the last few decades has been for more and more of the analog front end of transmitters and receivers to be taken over by digital components. While some suggest that eventually the entire analog front end will be replaced by digital components (or even a truly software radio) we argue in this paper that it is unlikely that this will occur in the near future. We then identify key analog components that are difficult, if not impossible, to replace and discuss what is likely to occur on both the analog and digital side of the interface in the near future.

[Abstract] 6LoWPAN (IPv6 over Low-power Wireless Personal Area Network) is a standard defined by IETF (Internet Engineering Task Force), which enables IPv6 transmission over IEEE 802.15.4 based WPANs (Wireless Personal Area Networks) to support many types of services, including WSNs (Wireless Sensor Networks). 6LoWPAN technology is rapidly gaining popularity for its extensive applicability, ranging from healthcare to environmental monitoring. In order to provide more reliable and effective IPv6 connectivity on top of LoWPAN, the 6LoWPAN WG (Working Group) has defined some key technologies. This paper introduces the 6LoWPAN technology and its applications, and discusses on possible technology that can enhance the energy efficiency of 6LoWPAN. One possible technology that is considered for combination with 6LoWPAN is the virtual multiple input and multiple output (V-MIMO) technology. The technical details of V-MIMO and its possible combination with 6LoWPAN are described in this paper.

[Abstract] With the emergence of demands of virtual infrastructure, cloud storage, hyper-computing, semantic search, collective intelligence, and semi-structured mining, the entrepreneur, developer, and everyday consumer would be unrecognizable when viewed by their counterparts even as recent as the beginning of the millennia. Adoption of XaaS (anything-as-a-service) has allowed the ushering of "anytime-anywhere-any-size" with social and entertaining aspects for the consumer, breadth-expansion capabilities for the software developer, and multidimensional marketing/sales channels for the entrepreneur. What is presented here is the dilation of these services through the increased abstraction with yet another layer of web services. One theoretical entry point is the ESB (enterprise service bus) which represents a robust architecture for a wide matrix of web services. Within it, there can exist concentric ESBs that ultimately serve as an XaaS for XaaS itself.

[Abstract] In this work we discuss, problems associated with aggregating data within a sensor network. Clearly, if one or more sensors are faulty, their data is questionable. in situations where data is aggregated together to form information, the accuracy of the information will also be questionable if some of the data is faulty. We briefly discuss some "simple statistical functions", which may need to be computed using sensor data. We construct some approximation methods for aggregated statical functions within a sensor network.

Session B5L-D: Signal Processing Applications

Chair: Magdy Hanna
Time: Tuesday, August 7, 2012, 16:00 – 17:40
Location: Clear Water

[Abstract] This paper proposes a rank minimization based approach to a novel image inpainting. We utilize the 2-D autoregressive (AR) model to describe the gray level of image, and formulate the image inpainting problem as the signal recovery problem by estimating the model order. This problem is described as the rank minimization problem, which is NP hard in general. To solve the problem approximately, this paper provide an algorithm utilize null space based alternation optimization (NSAO). Numerical examples show that the proposed algorithm recovers missing pixels well.

[Abstract] In this paper a design method based on spectral transformations is proposed for a particular class of 2D IIR filters, namely multi-directional filters. The design starts from an analog prototype with specified parameters. Applying an appropriate frequency transformation to the 1D transfer function, the desired 2D filter is directly obtained in a factorized form. The approach is mainly analytical but also uses numerical approximations and is simple, efficient and versatile. For two-directional filters, an example is given of extracting lines with two different orientations from a test image.

Session B5L-E: Special Session II: Speaker Recognition

Chair: G. Sapijaszko, *University of Central Florida*
Time: Tuesday, August 7, 2012, 16:00 – 17:40
Location: River Fork

[Abstract] Fault Tolerant Adaptive Filters (FTAFs) rely on inherent learning capabilities of the adaptive process to compensate for transient (soft) or permanent (hard) errors in hardware implementations. This paper investigates fault tolerant transform domain adaptive noise canceling filters to cancel noise from corrupted speech signals. Two transform domain adaptive FIR architectures are compared, one based on the conventional FFT and one on the Modified Discrete Fourier Transform (MDFT), both without zero padding. Results support the fact that the MDFT-based FTAF architecture is able to overcome certain fault conditions that cannot be properly handled with a conventional FFT-based FTAF architecture.

[Abstract] Currently there is a considerable tendency in developing Automatic Speech Recognition (ASR) systems which are capable of tracking the human speech done in local specific languages and identifying them because the people prefer to work with computers using their native language. In Sri Lanka, a sizable portion of the population are discouraged to use computers simply because language problem and difficulty of using the conventional interfaces. Consequently there is a great demand for a computer interface which can be work in Sinhala. This paper presents an approach to identify Sinhala speech based on Dynamic Time Warping (DTW) and the Mel Frequency Cepstral Coefficients (MFCC). The correct recognition was achieved in several phases and each phase is described in detail.

[Abstract] For centuries, researchers around the world have attempted to develop a natural interface between human and computer that enables the computer to speak and understand the natural language as the humans do. Even speech recognition systems for some recognized languages have been developed to some extent; still people prefer to work with their native language. On the other hand, speaker dependability has been a major issue in many cases and majority of users prefer if the recognizer is independent of speaker because in a speaker dependent platform, each user has to undergo training phase as the recognizer does not keep reference templates for each potential user. In this research, Genetic Algorithm (GA) was successfully applied with Mel Frequency Cepstral Coefficients (MFCC) to identify separately pronounced Sinhala words in both speaker independent and speaker dependent platforms.

Session C1P-F: Programmable-logic Based Digital Design

Chair: Semih Aslan
Time: Wednesday, August 8, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] Time-Correlated Single Photon Counting (TCSPC) can provide not only the time information of a photon, but also the photon density information. Based on the conclusion of usual time interval measuring methods, this paper chooses the scheme of Time-to-Digital Converter (TDC) based on delay line structure, meeting the TCSPC system's requirement for high timing resolution. This TDC contains two delay lines and a main counter. After finishing the framework of the TDC using Verilog, we confirm the architecture of the delay element by simulation and on-board test. Using the histogram from FPGA, the TDC system implement is for time resolution below 200 ps.

[Abstract] The paper describes two scrambler architectures developed in programmable logic and compares the performance of these circuits.

[Abstract] A flexible and efficient fixed to floating point conversion tool is presented for digital signal processing and communication systems. Fixed point numbers are heavily used in digital systems because they require less hardware, verification time and design effort compared to floating point number systems. However, floating point numbers offer better precision. Some digital designs may use a hybrid number system wherein fixed and floating point numbers can be used together to improve accuracy. The proposed design tool converts fixed-point numbers to floating-point numbers, including IEEE-754 floating point number standard. This tool generates Verilog RTL code and its testbench that can be implemented in FPGA and VLSI systems. The proposed design tool can increase productivity by reducing the design and verification time.

[Abstract] Linear Feedback Shift Registers (LFSRs) and Cellular Automata (CA) are commonly used in the implementation of pseudo-random number generators (PRNGs). However, these designs typically cannot produce high quality random numbers due to adjacent bit correlations and the appearance of repetitive structures in the bit sequences. This paper explores the implementation of a hybrid configuration which combines the bit streams from an LFSR and a CA. In particular, designs that are suitable for implementation on a Field Programmable Gate Arrays (FPGAs) are investigated. The proposed configurations take advantage of the FPGA's ability to realize compact LFSR implementations. Site spacing is utilized to lessen the effect of adjacent bit correlations and hence improve the random number quality. The concept of entropy is one figure of merit employed to evaluate the quality of the random numbers. The suite of statistical tests found in the DIEHARD program is also used in this regard. Hybrid LFSR/CA with varying degrees of site spacing are presented which were found to pass all the DIEHARD tests.

Session C1P-G: Digital Signal Processing and Communications I

Chair: Semih Aslan
Time: Wednesday, August 8, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] Wireless Body Area Networks (WBANs) consist of small intelligent wireless sensors attached on or implanted in the body. These wireless sensors are responsible for collecting, processing, and transmitting vital information such as: blood pressure, heart rate, electrocardiographic (ECG), electroencephalography (EEG) to provide continuous health monitoring with real-time feedback to the users and medical centers. In order to fully exploit the benefits of WBANs for important applications such as Electronic Health (EH) and Mobile Health (MH), the power consumption must be minimized. Our simulation results show that sampling rate can be reduced to 25% and power consumption to 35% without sacrificing performances by employing the CS theory to WBANs.

[Abstract] Based on a pure l_2 norm, the l_2-sensitivity for canonical forms in one-dimensional (1-D) and two-dimensional (2-D) separable-denoninator state-space digital filters is analyzed more precisely by taking into account 0 and 1 elements. First, l_2-sensitivity measures are explored for a controllable canonical form as well as an observable canonical form in state-space digital filters. Next, an l_2-sensitivity measure is investigated for a canonical form in 2-D separable-denominator state-space digital filters. Finally, numerical examples are presented to compare the resulting l_2-sensitivity measures with the conventional ones.

[Abstract] This paper presents a data-aided Carrier Frequency Offset(CFO) estimation algorithm targeting the Wideband OFDM systems. Utilizing 3 consecutive preambles and processing them at frequency domain, the algorithm is robust to both Frequency Independent (F-I) and Frequency Dependent (F-D) I/Q Mismatch (I/Q-M). To evaluate the effectiveness of the proposed CFO estimation technique, we conduct extensive simulations based on Multi-Band OFDM Ultra-Wide Band wireless transmission. Compared to the ideal case when the CFO has been perfectly estimated, the performance loss at 8% Packet Error Rate (PER) is less than 0.5 dB.

[Abstract] This work presents Genetic Algorithms and Simulated Annealing optimization methods applied in Wireless Sensors Networks localization through the use of Artificial Neural Networks (ANNs). These optimization methods were used aiming the adjustment of the main ANNs structure parameters such as number of hidden layers, number of nodes per hidden layer and transfer functions of each layer. Results using the best ANN structure found after optimization using GA had a root mean square error of 0.41 meter against the 0.61 meter reached through the SA algorithm.

Session C1P-H: Digital Signal Processing and Communications II

Chair: K.K. Kim
Time: Wednesday, August 8, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] We have presented a novel clock and data recovery scheme for 10Gbps source synchronous link in 65nm CMOS technology. In this design, a quadrature clock generation circuit based on a open loop delay line is proposed, avoiding the complex design of DLL and PLL. The simulated phase error is only 0.36 degree comparing to ideal quadrature clocks. A novel clock and data recovery algorithm is also implemented to effectively suppress the input data jitter. The overall power consumption is 25mW for 1.2V power supply.

[Abstract] A data lane circuit for a forwarded clock receiver is proposed in 65nm CMOS. This design is comprised of a continuous time linear equalizer which can compensate the channel loss over 8dB and cancel system offset within 1mV, a configurable half-rate digital CDR. The data rate of the receiver is 6.4Gb/s. The whole power consumption of the data lane is 24.5mW for 1.2V supply.

[Abstract] Random-access packet-based communication schemes are suitable for wireless sensor networks since medium access in their applications is often uncoordinated while sensor nodes communicate bursty flows of data. Preamble detection is an important task in packet-based communication protocols. The implementation of a previously proposed preamble detection scheme for low-power, wide-band, asynchronous packet communications which includes built-in characterization features is presented here. The baseband transmitter design was fabricated on IBM's 130-nm digital CMOS process and the baseband receiver design was prototyped on a Xilinx FPGA. Silicon prototypes of the fabricated design were successfully tested. The performance of the preamble detector measured at hardware speed is reported.

[Abstract] It is very important to detect power quality disturbances effectively in power quality monitoring. In industrial and commercial power systems, voltage sags, voltage swells, transients, and interruptions are main disturbances which affect sensitive equipments. This paper presents a signal processing technique which combines filter bank system and adaptive filter for power quality disturbances detection and localization. In this method, the filter bank system which has binary tree structure is designed for decomposing input power signal to subband signal components. In each subband, adaptive filters are operated as predictor, and the residual values of each adaptive predictor are used to detect power quality disturbances. The usefulness of the proposed method is demonstrated by synthesized signals harmonically.

Session C1P-J: Digital Signal Processing and Communications III

Chair: K.K. Kim
Time: Wednesday, August 8, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] The conventional soft-decision based noise estimation algorithms normally assume that noise exists, only when speech is absent. Consequently, the estimated noise spectra are not updated in the segments of speech presence, but only in those of speech absence. This assumption often results in several problems such as delay and bias of noise spectrum estimates. In this paper, we propose a solution by using speech enhancement residue (SER) to compensate the estimation bias in the presence of speech. The proposed method can be naturally combined with the improved minimum controlled averaging (IMCRA) method to consistently update noise spectra. The experimental results show that the SER-based IMCRA can reduce the relative segmental estimation errors for various types of noise at different SNR levels, especially for car internal noise.

[Abstract] In this paper, we present a novel approach to the problem of estimating and tracking the direction-of-arrival (DOA) of signals with known waveforms and unknown gains impinging on symmetric sparse subarrays. Unlike the conventional methods, which estimate the DOA based on the spatial signature of the signal with known waveform, the proposed method partitions the whole least square (LS) problem into multiple linear regression models of which each obtains a pair of DOA and gain. Here, we exploit a simple and efficient QR-decomposition-based recursive least square (QRD-RLS) technique to solve each linear regression model. Thanks to the unitary transformation for symmetric array configuration, we can decouple the pair of DOA and gain easily. Finally, several numerical examples showing the performance of the method are provided.

[Abstract] In this paper, we present a system using an Android smartphone that collects, displays sensor data on the screen and streams to the central server simultaneously. Bluetooth and wireless Internet connection are used for data transmission among the devices. Also, using Near Field Communication (NFC) technology, we have constructed a more efficient and convenient mechanism to achieve automatic Bluetooth connection and automatic application execution. This system is beneficial on body sensor networks (BSN) developed for medical healthcare applications. For demonstration purposes, the accelerometer, temperature sensor and electrocardiography (ECG) signal data are used to perform the experiments. Raw sensor data is interpreted to either graphical or text notation to be presented on the smartphone and the central server. Furthermore, a Java-based central server application is used to demonstrate communication with the Android system for data storage and analysis.

[Abstract] A method to design low-complexity FIR Hilbert transformers with narrow transition bands and small ripples is presented in this paper. The proposal is based on a strategic combination of the Frequency-Response Masking (FRM) and Frequency Transformation (FT) techniques. The FT technique is employed to divide the overall filter in several identical simple subfilters, whereas the FRM technique is employed to design every subfilter reducing further the complexity of the overall filter. By applying simple rounding to the subfilter coefficients, the overall design achieves a very low number of multiplications per output sample. Design examples show that the proposed method has a lower computational complexity than other existing methods.

Session C1P-K: Image Processing Applications

Chair: Kurtis Cantley
Time: Wednesday, August 8, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] Data hiding is a technique that embeds an imperceptible and statistically undetectable signal to the digital content. Reversible watermarking is able to restore the original signal without distortion after data extraction, this property is useful in several application as military communications, medical diagnostics and legal evidence. In this paper, a reversible audio watermarking scheme using an interpolation technique is proposed. From experimental results the high capacity and auditive transparency of the proposed scheme are shown. Moreover, a multi-embedding approach is explored. Accordingly, a new subject for research is discovered.

[Abstract] In this paper we propose a new framework to obtain 3D shape information of thin film rapidly. The conventional equipments based on reflectometry are not suitable for obtaining 3D overall shape information of thin film rapidly since they require more than 30 minutes to measure the absolute thickness for 170 points. The proposed framework is based on an image analysis method that extracts contour lines from interference fringes images using Canny edge detector. The absolute thicknesses for contour lines are measured and then a height map from the contour lines is obtained by interpolation using modified Borgefors distance transformation. The extracted height map is visualized using the DirectX 3D terrain rendering method. The proposed framework can provide 3D overall shape information of thin film in about 5 minutes since relatively small number of real measurement for contour lines is required.

[Abstract] Minimization of computational errors in the fixed-point data path is often difficult task. Many signal processing algorithms use chains of consecutive additions. We propose the analyzing technique that can be applied to fixed-point data path synthesis, with taking advantage of allocating the chains of consecutive additions in order to predict growing width of the data path and minimize the design complexity and computational error.

[Abstract] This paper presents a new computer vision design flow for real time detection and recognition of traffic signs. Autonomous traffic sign detection can play a crucial role in many applications related to transportation safety and geographical information systems. The challenges that need to be addressed include the necessity for robust and accurate detection as well as the high computational requirements of the algorithms. Therefore, we develop a three stage algorithm that is based on i) detection of traffic sign locations using HSV color space, ii) detection of traffic signs using discriminative features and iii) recognition of traffic signs using interest point descriptors. The results show a robust detection and recognition performance for multiple signs and the algorithm can be executed in real-time.

[Abstract] Reversible watermarking, a technique that can recover an undistorted original image from a watermarked one, has drawn considerable attention in recent years. However, most of the current reversible watermarking algorithms based on histogram shifting have underflow and overflow problems in regards to the watermarked image due to the histogram shift. In order to nip these problems in the bud, in the proposed algorithm the lower and upper bound pixel levels are modified into the nearest neighbor pixel levels and the position information of the modified pixel levels are embedded in the watermarked image. In addition, to increase the data hiding capacity while keeping high visual quality of the watermarked image we allows multi-level data hiding using a rotated even-odd difference image. The simulation results demonstrate that the proposed algorithm generates a superior performance in the PSNR values and the embedding capacity.

Session C1P-L: Video Processing and Transmission

Chair: Hideaki Okazaki
Time: Wednesday, August 8, 2012, 9:00 – 10:10
Location: Poster Area

[Abstract] This paper presents a fast fractional motion estimation (FME) and the associated VLSI architecture for H.264/AVC multiview video coding. The proposed FME automatically turns off the mode P8x8 by exploiting the results of integer motion estimation and similarity between views. In addition, the fraction-pel refinement of integer motion or disparity vector in any partition may be skipped according to the difference of their rate-distortion cost. This algorithm accelerates the FME by nearly 50% with negligible PSNR degradation and bitrate increase. The resultant FME can process a macroblock within 612 clock cycles, enough to achieve real-time coding for the stereoscopic HD1080p video sequences operating at frequency of 300 MHz.

[Abstract] This paper presents an enhanced fast motion estimation method where a search point sampling technique is combined with the adaptive search range algorithm (ASRA) based on the probabilities of motion vector differences, which is our previous work. Since the ASRA is based on reduction of search ranges for less computational complexity rather than sub-sampling of search points that is adopted by the most of fast algorithms, it results in smaller search areas where all points are considered as search points. Therefore, the conventional fast algorithms based on search point sampling techniques such as three-step search algorithm can be easily employed to the ASRA. As a result, we propose an algorithm where a part of the points within the search areas determined by the ASRA are sampled as the search points. Experimental results show that the proposed method reduces complexity of our ASRA by about 60% without quality degradation.

[Abstract] This work is to explore a frequency-domain down-sizing method which preserves picture quality and consumes low complexity in a video decoder. The conventional frequency-domain down-sizing methods usually yield a drift error owing to frequency-domain coefficient truncation and motion compensation using small reference frames. The proposed method can overcome this drawback by using non-zero coefficient compensation and adaptive block-size decoding. In a Group of Pictures (GOP), an I frame and P frames close to the I frame are decoded at a full frame size and then are performed by downscaling. The motion vectors of the other P frames are pre-decoded first and then are analyzed to understand their referring relationship. Based on this relationship, the blocks which are referred and not referred by the other moving blocks are decoded at full and small block sizes, respectively. Additionally, B frames are decoded at an adaptive block size. The simulation results demonstrate that the proposed method can attain the same picture quality and 11%-29% complexity reduction than the conventional method conducting at a full frame size.

[Abstract] The problem of recognizing the objects movement in a sequence of video images has been addressed using different models. Such models attempt to describe the general characteristics of such movements, which requires an accurate estimation the optical flow, or velocity of the images. That is the approach of the object movement defined as the projection of the 3D surfaces points speeds on a 2D plane. Among the several approaches proposed to this end, the optical flow estimation methods proposed by Horn-Schunck and Lucas-Kanade are some of the most widely used. These methods strongly depend on the use of a smoothing Gaussian function. This paper improves the performance of both methods replacing the Gaussian function by a set of functions, called Atomic functions, that present frequency responses with higher attenuation of its side lobes. The performances of conventional and proposed modifications are evaluated comparing the disparity map of the optical flow images obtained, using the SSIM method.

Session C2L-A: Data Conversion Techniques I

Chair: Jose Silva-Martinez, *Texas A&M University*
Time: Wednesday, August 8, 2012, 10:10 – 11:50
Location: White Water

[Abstract] A low power interface circuit for multisensory system is presented in this paper. A SAR capacitance-to-digital converter (CDC) and a SAR analog-to-digital converter (ADC) are combined together so that capacitance or voltage from different sensors can be measured by the same circuit and converted to digital signal directly. A dynamic comparator with self-calibration is designed to achieve zero-static power. Bootstrapped switches and bottom-plate sampling are used to reduce the non-idealities of sample/hold circuit. The 11bit converter is designed in 0.18um CMOS process with a core area of 0.1764 mm2. It consumes 6.7μW and achieves an energy efficiency of 18.8 fJ/conversion-step as a CDC.

[Abstract] A 10-bit 30mW 250MS/s dual-channel SHA-less pipeline ADC with op-amp-sharing between two channels and a new timing scheme to eliminate sampling timing skew is presented in this paper. The proposed timing scheme uses a single-edge sampling clock to achieve double sampling without introducing timing skew. It is applicable to SHA-less ADC front-end and meanwhile allows the first-stage flash comparator and encoder to be operated in the clock idle time without affecting the MDAC settling time. It is also applicable to bottom-plate sampling thus avoiding the signal-dependent charge injection. The proposed op-amp sharing technique with switch-embedded dual-input pair eliminates the memory effects without introducing extra capacitance to the op-amp, facilitating the ADC to operate at high sampling rates. The gain and offset errors between the channels are calibrated in digital domain. Simulation results show that the ADC designed in a 018-μm CMOS process achieves a maximum SNDR of 61.84 dB (ENOB = 9.98) and a peak SFDR of 78.1 dB at 250 MS/s. The ADC core consumes 32 mW at 250 MS/s under a 1.8-V supply voltage.

[Abstract] This paper presents a new asynchronous binary search analog to digital converter (ADC). Proposed asynchronous binary search ADC enables higher speed operation of binary search algorithm by resolving two bits in each step. Using two bit flash quantizers in each stage of the proposed binary search ADC the conversion speed improves by two times compared with conventional binary search ADC architectures. New sampling scheme and dynamic offset cancellation technique for the comparator have been adapted to realize a low power and high speed converter. The proposed single channel 6-bit 1GS/s ADC was designed in 65nm CMOS process. Simulation results show that the ADC reaches a peak SNDR of 36.12dB consuming 1.35mW from a single 1.2V power supply. It achieves of 29fJ/conv.code FoM.

[Abstract] This paper investigates the tradeoffs in the design of a charge-redistribution D/A converter (DAC) in successive approximation register A/D converters. A new capacitive DAC is also introduced. It is shown that the proposed circuit can reduce the power dissipation by a factor 16, and chip area by a factor of 4 compared to a conventional DAC.

[Abstract] We show the design of a current mode ramp analog to digital converter (ADC) in standard 0.13μm 1poly, 8 metal CMOS process. The ADC is a low-power and area-saving solution for multi-frequency cell impedance measurement. It uses two-step conversion to boost the conversion time by a factor of 32 while keeping a constant practical clock frequency. The ramp ADC samples current signals at different frequencies and converts them into digital signals simultaneously. The main blocks of the ADC is current-mode ramp generator, current comparator, a delay locked loop (DLL) and a gray-code counter.

Session C2L-B: Digital Signal Processing I

Chair: Wasfy Mikhael, *University of Central Florida*
Time: Wednesday, August 8, 2012, 10:10 – 11:50
Location: Rapids

[Abstract] Since having orthonormal Hermite-Gaussian-like eigenvectors of the DFT-IV matrix G is essential for developing a fractional discrete Fourier transform of type IV (FDFTIV), some methods for the generation of those eigenvectors are analyzed in a detailed simulation study involving evaluating the execution time, orthonormality error and approximation error. Since six of the nine methods included in the study necessitate knowledge of the orthogonal projection matrices on the eigenspaces of the DFT-IV matrix, explicit expressions are derived for those matrices. Based on this contribution it is no longer essential to generate the eigenvectors of a nearly tridiagonal matrix S which commutes with matrix G as a way for obtaining eigenvectors of the latter. The simulation results show the tradeoff between the speed of execution and the numerical robustness of the computation of the various techniques.

[Abstract] We propose a signal denoising method based on the undecimated wavelet transform. The proposed method uses the well-known Stein`s Unbiased Risk Estimator (SURE). A derivation of SURE with trimmed thresholding of the undecimated wavelet transform coefficients is given and an adapted algorithm is developed to solve the resulting minimax problem. The result is a denoising method with better performance than the traditional thresholding techniques with soft thresholding. We illustrate the advantage of the derived wavelet denoising procedure on an ECG signal contaminated with background white Gaussian noise. The results show that the proposed method compares favorably with other methods.

[Abstract] This paper presents the adaptive noise cancellation model as a method for isolating the seismic response of an infrasound sensor. The technique is applied to a real-world data set, and the results demonstrate its effectiveness in isolating the seismic response. The technique provides access to two previously unattainable signals: the isolated seismic response and the infrasound response uncorrupted by any seismic noise. Once separated, these signals open the doors to many new and exciting applications, including augmentation of co-located seismic measurements, more precise calibration of fielded infrasound sensors, and even a lowered noise floor for better detection of infrasonic events.

[Abstract] A facial recognition technique employing Frequency Domain Thresholding and Quantization (FD-TQ) is presented in this paper. The algorithm has attractive properties with respect to storage requirements and computational complexity in both the training and testing modes, which make the technique particularly suitable for large data bases. The new algorithm is applied to ORL, Yale and FERET data bases. The experimental results confirm the significant reduction in the storage and computational requirements compared with recently reported techniques, without sacrificing the recognition accuracy.

Session C2L-C: Invited Session V

Chair: Mohamad Sawan, *Polytechnique Montréal, Canada*
Time: Wednesday, August 8, 2012, 10:10 – 11:50
Location: Ivy

[Abstract] Analog/Mixed-Signal (AMS) Power Systems-on-chip (SOC) require variety of current-based tests to be performed, with large dynamic range: from leakages in micro-ampere levels to high power load regulations and current limit test in multiampere levels. Limitations associated with automatic test equipment (ATE) incur high test cost in the form long test times and additional hardware required to multiplex high power resources to device-under-test pins. In our work we propose a framework for forcing and measuring currents on-chip via combo-DFT (built-in current sensor, current DAC, recycling and ATE co-test methodologies) and achieves >50% reduction in manufacturing test time and 50% reduction in ATE resource requirements.

Session C2L-D: Power Electronic Circuits I

Chair: Donald Lie
Time: Wednesday, August 8, 2012, 10:10 – 11:50
Location: Clear Water

[Abstract] This paper presents a novel fully integrated onchip switched-capacitor (SC) DC-DC converter that supports programmable regulated load voltage ranging from 2.6V to 3.2V out of 5V input supply. MOS capacitors are used for flying capacitors (600pF) and load capacitor (400pF) in this implementation. To minimize the bottom-plate parasitic capacitor related loss while maximizing the load current driving capability, the proposed 4-to-3 step-down topology utilizes two differently sized conventional 2-to-1 step-down topologies, each of which has different value of flying capacitor. In addition, the proposed implementation reduces switching loss and control circuit loss since the internally generated output voltage of the bottom 2-to-1 block is used as the supply for the control circuits throughout the small internal LDO regulator.

[Abstract] This paper proposes a control system to widen the bandwidth of piezoelectric transducers (PZTs) for vibration energy harvesting while extracting maximum power. A straightforward complex conjugate match achieves maximum power transfer only at a single frequency while requiring an impractically large inductance. The proposed system intends to address these problems. It incorporates a bi-directional DC/DC converter with feed-forward control to achieve a complex conjugate match over a wide range of frequencies. Analysis of the proposed system and simulation results are presented to verify validity of the proposed method.

[Abstract] Adiabatic charging and discharging of a capacitor with an inductor current by controlling switching transistors is demonstrated experimentally. First, we designed an eight-step charging and discharging circuit. The switching transistor ratio is designed to range from zero to one in one-eighth steps. By changing the switching transistor ratio stepwise, output voltage is generated stepwise. Using the stepwise voltage, adiabatic charging and discharging can be performed. In N-step charging, it is clarified that the energy dissipation is reduced to 1/N from the measurement of the power supply current, compared with the conventional charging and discharging of a capacitor.

[Abstract] Accurate measurement of reverse recovery parameters (RRPs) in high-speed, high-power switches and rectifiers is a fundamental task in their test and characterization process. Performing such tests at a wafer-level in laterally diffused MOSFETs (LDMOS) presents several challenges with respect to their test in packaged devices. The handling of prober parasitic impedances, current injection constraints, and automated signal synchronization top the list of issues that need to be addressed. Moreover, making the tests amenable for automated execution just adds more constraints to the problem. This paper proposes a solution for automatic characterization of wafer-level LDMOS RRPs that include reverse recovery time (trr), reverse recovery current (Irr), and storage charge (Qrr). Its implementation has enabled accurate automated parametric wafer-level LDMOS tests at currents as high as 15A and dI/dt's of up to 173A/us.

[Abstract] Due to the steadily-increasing demands on more powerful electronic gadgets, an accumulator's operating lifetime plays an essential role for the usability of battery-powered devices. To avoid an insufficient utilization of a cell's energy and/or lifetime, a reliable and reasonably accurate knowledge of its internal parameters like the state-of-charge (SoC) is indispensable. The determination of the SoC is often directly related to the estimation of a battery's open-circuit voltage (OCV). In this paper, different OCV estimation methodologies are compared with respect to their inherent accuracy. Additionally, the observability-Gramian-based OCV estimation method is extended to deal with expanded kinds of cell currents. Moreover, interpolation-based methodologies are presented which considerably reduce the average OCV estimation error over the entire SoC range, compared to state-of-the-art implementations.

Session C2L-E: Special Session IV: Integrated Power Management Circuits

Chair: Paul Furth, *New Mexico State University*
Time: Wednesday, August 8, 2012, 10:10 – 11:50
Location: River Fork

[Abstract] An input-adaptive dual-output charge pump (DOQP) with variable fractional conversion ratio and low dropout regulators (LDRs) in cascade is implemented for the power management unit (PMU) of implantable energy harvesting devices. The charge pump has one step-down and one step-up output adaptively converted from a 1.8 to 4.0V harvested energy source, and the outputs of the LDRs are 1V and 3V respectively. To improve the overall efficiency, conversion ratios of k/6 (k=2,…-, 12) are realized by 1/2- and 1/3-capacitors using an interleaving scheme. The PMU is designed using a 0.13um 3.3V CMOS process, and attains the peak efficiency of 81.3% and efficiency better than 55% for a wide input range.

[Abstract] Energy and power in tiny batteries are often insufficient to sustain the demands of a wireless microsystem for extended periods. Piezoelectric transducers are viable alternatives because they draw power from a vast tank-free supply of ambient kinetic energy in vibrations. Unfortunately, small devices alone seldom dampen vibrations enough to fully harness what is available, which is why investing energy to increase the electrical damping force that transducers impose is so important. This paper introduces and evaluates three investment schemes and 0.35-µm CMOS switched-inductor circuits that increase this force to generate more output power.

[Abstract] We explore the application of split-length compensation to the design of a three-stage low dropout (LDO) voltage regulator. Initially, we review three basic compensation techniques, Miller, cascode, and split-length, and demonstrate their use in a multi-stage amplifier. It is found that stable designs are possible using single Miller compensation, whereas both cascode and split-length compensation require a Miller compensation network in parallel. Finally, we compare the three compensation techniques in terms of quiescent current, area, dropout voltage, unity-gain frequency, line and load transient response, and power supply rejection. For the LDO architecture selected, it is found that cascode and split-length compensation offer very similar performance, with the exception of quiescent current and area. Cascode compensation required 24% less total compensation capacitance, whereas split-length compensation used 14% less quiescent current.

[Abstract] This paper demonstrates an auto-reconfigurable single-inductor triple-input dual-output (SITIDO) regulator that can obtain power from three independent sources (two energy harvesters and an internal battery) and provide dual output regulations. An input power conditioning scheme is developed to configure the converter automatically to either the energy-harvesting mode (SIDIDO/SISIDO boost configuration) or the battery-powered mode (SISISO buck configuration) based on the available power from different sources. A sub-threshold dual-mode controller is also adopted to optimize the converter power efficiency over a wide load range, minimize cross regulation between different outputs, and provide the predictable output noise spectrum. Implemented in a standard 0.35-um CMOS process, the proposed converter achieves a power efficiency of > 66% over an output range from 0.3 mW to 33 mW with the peak power efficiency of 88%.

Session C3L-A: Data Conversion Techniques II

Chair: Vishal Saxena, *Boise State University*
Time: Wednesday, August 8, 2012, 13:10 – 14:50
Location: White Water

[Abstract] Excess Loop Delay (ELD) induced feedback DAC nonideality is a dominant factor causing error in the transfer function of CT Sigma Delta modulators and eventually leading to instability. This paper will present a novel technique which aims to track the amount of excess loop delay, and compensate by using digital logic elements and an RC feedback network. A 2nd order CT Sigma Delta modulator with 1-bit DAC was built at transistor-level in 65nm CMOS to demonstrate the efficiency of the method. The Cadence simulation results show that, by using the proposed technique, the modulator can track the ELD up to 50% of the clock period duration and compensate it, leading to 69.2dB SNDR when compared with the ideal value of 70dB SNDR.

[Abstract] A sampling switch with an embedded Digital-to-Skew Converter (DSC) is presented in this paper. The proposed switch eliminates time-interleaved ADCs' skews by adjusting the boosted voltage. A similar bridged capacitors' charge sharing structure is used to minimize the area. The circuit is fabricated in a 0.18 μm CMOS process and achieves sub-1ps resolution and 200ps timing range at a rate of 100MS/s. The power consumption is 430μ W in maximum. Measurement result also includes a 2-channel 14-bit 100MS/s TI-ADCs with the proposed DSC switch's demonstration.

[Abstract] For high-accuracy digital-to-analog converter (DAC), delay difference depending on output voltage is one of the major nonlinearities that deteriorate the dynamic performance. In this paper, an improved output-dependent delay cancellation (ODDC) technique is proposed. The proposed ODDC is implemented in simple circuit architecture and has advantages of significant improvement on the dynamic performance in a wide frequency range without increasing the noise floor. ODDC can eliminate the switching instant variations caused by output voltage of DAC through tuning the bulk voltage of switches in the deep N-well. The algorithm of ODDC technique is derived. A 1GS/s 14 bits current-steering DAC with proposed ODDC is simulated and the SFDR can be improved significantly with proper circuit parameters.

[Abstract] A cryogenic CMOS D/A converter, core part of a Silicon quantum computer controller, produces voltage signals to generate electric fields for Silicon quantum bits initialization. In low temperature, the converter has to overcome several constraints before it is ready to work. These include CMOS operating region choice, anomalies of CMOS behavior, component mismatch degradation, technology choice and above all fulfilling the application requirements in cryogenic domain. In this paper, we explore these background requirements and critical issues that lead us to design a self calibrated ±1.5V 10 bit cryogenic D/A converter in 0.5µm CMOS Silicon-on-Sapphire process and briefly explain its architecture and design challenges. The differential nonlinearity (DNL) and integral nonlinearity (INL) of this converter are ±0.25 and ±0.4 least significant bit (LSB) respectively while its average power dissipation is 25mW and it occupies 1.2mm2 die area.

[Abstract] A simple and fast wireless technique for accurate tuning of the resonators in high speed bandpass sigma delta modulators (BPSDMs) is presented. A commercially available antenna is employed to detect the radiation of on-chip resonators in the oscillation mode. The antenna is used for the calibration of the resonators at first. After adjusting the tuned frequency of resonators, it is reused as the front-end part of an RF receiver. The proposed architecture accelerates and simplifies the tuning process. Moreover, an extra oscilloscope for storing and post processing of demultiplexed data, which is typically used in giga herz applications, is not required. Distinguishing between multi signal tones and disturbing tones in the spectrum is easier compared to conventional approaches.

Session C3L-B: Digital Signal Processing II

Chair: Maher Rizkalla, *IUPUI*
Co-Chair: Elettra Venosa
Time: Wednesday, August 8, 2012, 13:10 – 14:50
Location: Rapids

[Abstract] The fractional discrete Fourier transform of type IV (FDFT-IV) is a generalization of the discrete Fourier transform of type IV (DFT-IV). The paper presents a fully-fledged definition for the FDFT-IV which necessitates the availability of orthonormal eigenvectors of the DFT-IV matrix G. This definition is shown to outperform the simple definition which is just a linear combination of the signal, its DFT-IV and their flipped versions.

[Abstract] For two-dimensional (2-D) state-space digital filters described by the Fornasini-Marchesini second local state-space model, the joint optimization of high-order error feedback and realization for minimizing roundoff noise at filter output subject to l_2-scaling constraints is investigated. We present linear-algebraic techniques that convert the problem at hand into an unconstrained optimization problem, and present an efficient quasi-Newton algorithm to solve the unconstrained optimization problem iteratively, in which closed-form formulas are derived for fast and accurate gradient evaluation. A numerical example is presented to illustrate the utility and effectiveness of the proposed algorithm.

[Abstract] A Revised and more numerically accurate version of the Direct Batch Evaluation by constrained Optimization Algorithm (RDBEOA) of orthonormal eigenvectors of the DFT matrix F is presented. The superior numerical properties of the RDBEOA stem from the fact that it performs the singular value decomposition (SVD) of a matrix whose elements have almost half the range of values of the elements of the matrix to which the SVD is applied in the previous Direct Batch Evaluation by constrained Optimization Algorithm (DBEOA). Having more accurate Hermite-Gaussian-like (HGL) orthonormal eigenvectors of matrix F is a main requirement in the development of the discrete fractional Fourier transform (DFRFT).

[Abstract] This paper introduces the modified comb nonrecursive structure for the decimation factor which can be represented as a power of two and three. The structure has an improved alias rejection characteristic, decreased passband droop and a low power consumption. The implementation results are also included.

[Abstract] This paper presents an improvement of interpolation-based (k,n)-threshold secret image sharing (SIS) scheme, where a secret data payload is optimized using Lagrange Interpolation operated in GF(28). A secret data can be not only images but also any type of files, such as documents and executable files, which is hidden using Least Significant Bit (LSB) steganography into n innocent-looking images called camouflage images. In order to recover the secret data, at least k (≤n) camouflage images are required. The proposed scheme provides an authentication mechanism by parity-bit checking and lossless recovery of the secret data using GF(28) operation. Controlling the value of k, the size of camouflage images can be controlled to avoid a pixel expansion occurred in conventional SIS schemes.

Session C3L-C: Special Session VI: Digitally Enhanced Interleaved Data Converters

Chair: Charna Parkey
Time: Wednesday, August 8, 2012, 13:10 – 14:50
Location: Ivy

[Abstract] Even though time-interleaved analog-to-digital converters (ADCs) help to achieve higher bandwidth with simpler individual ADCs, gain, offset, and time-skew mismatch between the channels degrade the achievable resolution. Of particular interest is the time-skew error between channels which results in nonuniform samples and thereby introducing distortion tones at the output of the time-interleaved ADC. Time-varying digital reconstructors can be used to correct the time-skew errors between the channels in a time-interleaved ADC. However, the complexity of such reconstructors increases as their bandwidth approaches the Nyquist band. In addition to this, the reconstructor needs to be redesigned online every time the time-skew error varies. Design methods that result in minimum reconstructor order require expensive online redesign while those methods that simplify online redesign result in higher reconstructor complexity. This paper proposes a technique that can be used to simplify the online redesign and achieve a low complexity reconstructor at the same time.

[Abstract] TI-ADCs can offer a significant increase in the sample rate however their usage is limited due to the fact that their performance is strongly degraded by timing and gain mismatches between the channels. To assist in the mismatch estimation we inject a pilot tone between the signal spectrum and DC. The mismatches form an aliased copy of the pilot tone at high frequency where it is used for the estimation and canceling process. Modern software defined radio architectures are based on perfect reconstruction (PR) up and down converter channelizers. In this paper we present a novel architecture for estimating time and gain mismatches in two channel TI-ADCs which is based on PR channelizers and can be naturally embedded in modern digital radio receiver architectures. The PR polyphase channelizer engines provide us a compact and unique solution for filtering the aliased high frequency tone which is used for the mismatch estimation, canceling the low frequency tone and for down converting the corrected signal spectrum to base-band while adjusting its sample rate to the reduced bandwidth.

Session C3L-D: Power Electronic Circuits II

Chair: Hua Tang
Co-Chair: Donald Lie
Time: Wednesday, August 8, 2012, 13:10 – 14:50
Location: Clear Water

[Abstract] This paper presents the steady-state analysis of series resonant converter (SRC) using the extended describing function (EDF) method. The EDF method is used to express non-linear terms of switching waveforms as linear descriptors to develop a linear model of the converter. The converter under consideration consists of a half-bridge inverter and a full-wave rectifier. The steady-state analysis in the frequency-domain is presented. The characteristics such as input-to-output-voltage transfer function and input impedance are obtained by first harmonic approximation of the converter state variables. Experimental results are given for a laboratory prototype of the SRC operating at 24 VDC input, 10 VDC output, output power of 15 W, and at a switching frequency of 110 kHz to verify the theoretical analysis.

[Abstract] This paper introduces the integration of Class DE inverter with loosely coupled inductors for near-field wireless power transfer (WPT) applications. The benefits of using Class DE inverter in the inverter stage of the WPT system are the low transistor voltage stress and zero-voltage switching (ZVS) of the transistors. The step-by-step integration of circuits using Class DE inverter, tuned loosely coupled planar inductors, and the rectifier are given. The planar inductors are embedded into furniture-like wooden structures to simulate real-world applications. A detailed procedure to design a Class DE inverter-based WPT system using loosely coupled inductors is given. The design is illustrated with an example for low power application. Simulation and experimental results are given for the Class DE inverter operating at 300 kHz.

[Abstract] The performance of Active Power Filter (APF) is decided by the reference current estimation technique. This estimation is not straightforward in practice due to the distorted and unbalanced supply; nonlinear and unbalanced load. To address such practical situations, a new sliding DFT (SDFT) based technique involving instantaneous symmetrical components and p-q theory is proposed. With this method, the harmonic, fundamental frequency unbalanced and reactive current components are determined. The feature that the SDFT could provide the 90-degree shifted signal together with the symmetrical components is utilized for the purpose of determining the unbalanced current component. Fundamental reactive current is obtained using the widely used instantaneous p-q theory. The effectiveness of the proposed technique is demonstrated through the simulation results pertaining to three phase system with distorted and unbalanced supply.

[Abstract] One of the major factors that limit the powering distance in any RF energy scavenging sensor is the intrinsic threshold of the voltage-multiplier or voltage-boosting circuits. In this paper we present a passive matching network that overcomes the threshold-voltage limitation by enhancing the quality-factor of the voltage-multiplier front-end. We first derive the figures-of-merits comparing the theoretical improvements that can be achieved by the proposed matching network over a conventional parallel matching network. Using measured results from prototypes fabricated in a 0.5-µm CMOS process we show that for a fixed transmission power, the proposed approach significantly increases the powering distance of a 13.56MHz RF scavenging sensor.

Session C3L-E: Invited Session IV

Chair: Mona Zaghloul
Time: Wednesday, August 8, 2012, 13:10 – 14:50
Location: River Fork

[Abstract] This paper presents a low vision assistance system for individuals with blind spots in their visual field. The system uses face detection and tracking to identify prominent faces in the visual field and redisplays them in regions that are visible by the user. As part of the system performance evaluation, we compare algorithms for face detection and tracking on an Android smartphone, a netbook and a high-performance desktop computer representative of cloud computing. We examine processing time and energy consumption to determine the tradeoff of processing on a smartphone compared to compressing and transmitting to a cloud-desktop for processing.

[Abstract] This paper introduces the first fully digital implementation of 1-D, 2-D and 3-D multiscroll chaos using the sawtooth nonlinearity in a 3rd order ODE with the Euler approximation. Systems indicate chaotic behaviour through phase space boundedness and positive Lyapunov exponent. Low-significance bits form a PRNG and pass all tests in the NIST SP. 800-22 suite without post-processing. Real-time control of the number of scrolls allows distinct output streams with 2-D and 3-D multiscroll chaos enabling greater controllability. The proposed PRNGs are experimentally verified on a Xilinx Virtex 4 FPGA with logic utilization less than 1.25%, throughput up to 5.25 Gbits/s and up to 512 distinct output streams with low cross-correlation.

[Abstract] This paper presents a novel precoding approach for MIMO broadcast channels, in which is performed on both sides of the wireless link. The aim of the proposed approach is to avoid the same precoding vectors choice when all users use a common codebook. In the proposal approach, firstly, we focuss on the brute codeword selection at the transmitter side, thus there is zero probability to choose the same vector for more than one user. However, this solution leads an exhaustive search, especially when the number of user and the codebook size increase. To overcome this issue, secondly, we adopt the genetic algorithm in order to reduce the codeword search complexity. Compared with zero-forcing beamforming (ZFBF), the conducted simulation results for the critical scenario of low SNR, show that our scheme is better then ZFBF with the assumption of both perfect and partial channel state information at the transmitter.

[Abstract] A well known circuit – due to Lazzaro – for WTA neural applications is considered. It is a current mode low voltage network based on subthreshold MOS devices. The authors show that the circuit model does not guarantee by itself that all transistors keep staying in the subthreshold region. To this goal, supplementary conditions on the range of input and bias currents are derived. This results in a synthesis procedure which is simple and flexible and takes into account an input-output performance as well. Numerical examples are also given.

[Abstract] We report a SPICE compatible closed form compact memristor model, for the temporal evolution of resistance in a memristor under the action of a programming voltage. This compact model compares well to published transition time formulae and known memristor behavior. We use the SPICE equivalent of the model in a novel Wien-Bridge oscillator signal conditioning circuit application.

[Abstract] This paper presents a design example of an ultra-low power analog front-end (AFE) integrated circuits (IC) and system for biomedical sensing applications. The low-power 0.18-um CMOS AFE IC design includes a low noise instrumentation amplifier (INA), a band-pass filter (BPF), a variable gain amplifier (VGA), and a successive approximation register (SAR) analog-to-digital converter (ADC). The AFE IC architecture is analyzed on the system level to minimize total power consumption. The INA, Gm-C filter and the SAR ADC circuits are not only designed for high power efficiency and integration, but also optimized for an ECG sensing system to save on the overall power consumption. SPICE simulations of the AFE IC channel validate the ultra-low power IC design methodology for heartbeat detection with less than 5 uW/channel.