

2012 7th International Workshop on Reconfigurable Communication– centric Systems-on-Chip

(ReCoSoE 2012)

**York, United Kingdom
9-11 July 2012**



**IEEE Catalog Number: CFP1226P-PRT
ISBN: 978-1-4673-2570-7**

TABLE OF CONTENTS

Translating Java for Resource Constrained Embedded Systems	1
<i>Gary Plumbridge, Neil Audsley</i>	
Accuracy Evaluation of GEM5 Simulator System	9
<i>Anastasiia Butko, Rafael Garibotti, Luciano Ost, Gilles Sassatelli</i>	
Designing Formal Reconfiguration Control using UML/MARTE	16
<i>Sebastien Guillet, Florent De Lamotte, Nicolas Le Griguer, Eric Rutten, Guy Gogniat, Jean-Philippe Diguët</i>	
Distributed Control for Reconfigurable FPGA Systems: A High-level Design Approach	24
<i>Chiraz Trabelsi, Samy Meftali, Jean-Luc Dekeyser</i>	
Invited Paper: On-Chip Monitoring for Adaptive Heterogeneous Multicore Systems	32
<i>Diana Goehring, Mounir Chemaou, Michael Huebner</i>	
On Implementability of Polymorphic Register Files	39
<i>Catalin Ciobanu, Georgi Kuzmanov, Georgi Gaydadjiev</i>	
Invited Paper: Acceleration of Computationally-Intensive Kernels in the Reconfigurable Era	45
<i>Kyprianos Papadimitriou, Charalampos Vatsolakis, Dionisios Pnevmatikatos</i>	
Programming Strategies for Runtime Adaptability	50
<i>Joao M. P. Cardoso</i>	
RIVER Architecture: Reconfigurable Flow and Fabric for Parallel Stream Processing on FPGAs	58
<i>Dominic Hillenbrand, Christian Brugger, Jie Tao, Shufan Yang, Matthias Balzer</i>	
Adaptive Parallelism Exploitation under Physical and Real-Time Constraints for Resilient Systems	66
<i>Fabio P. Itturriet, Gabriel L. Nazar, Ronaldo R. Ferreira, Alvaro F. Moreira, Luigi Carro</i>	
Dynamically Reconfigurable Flux Limiter Functions in MUSCL Scheme	74
<i>Mohamad Sofian Abu Talip, Takayuki Akamine, Yasunori Osana, Naoyuki Fujita, Hideharu Amano</i>	
A Flexible Approach for Compiling Scilab to Reconfigurable Multi-Core Embedded Systems	81
<i>Timo Stripf, Oliver Oey, Thomas Bruckschloegl, Ralf Koenig, Michael Huebner, Juergen Becker, George Goulas, Panayiotis Alefragis</i>	
ENOSYS FP7 EU Project: An Integrated Modeling and Synthesis Flow for Embedded Systems Design	89
<i>Etienne Brosse, Imran R Quadri, Andrey Sadovykh, Frank Ierommimon, Dimitrios Kritharidis, Rafael Catrou</i>	
Smart Technologies for Effective Reconfiguration: The FASTER Approach	94
<i>M. D. Santambrogio, D. Pnevmatikatos, K. Papadimitriou, C. Pilato, G. Gaydadjiev, D. Stroobandt, T. Becker, W. Luk, A. Bonetto, A. Cazzaniga</i>	
MADES FP7 EU Project: Effective High Level SysML/MARTE Methodology for Real-Time and Embedded Avionics Systems	101
<i>Imran R. Quadri, Etienne Brosse, Ian Gray, Nicholas Matragkas, Leandro Soares Indrusiak, Matteo Rossi</i>	
Automatic Run-Time Manager Generation for Reconfigurable MPSoC Architectures	109
<i>Gianluca Durelli, Christian Pilato, Andrea Cazzaniga, Donatella Sciuto, Marco D. Santambrogio</i>	
Membrane-based Design and Management Methodology for Parallel Dynamically Reconfigurable Embedded Systems	117
<i>Pamela Wattebled, Jean-Philippe Diguët, Jean-Luc Dekeyser</i>	
A RTRM Proposal for Multi/many-core Platforms and Reconfigurable Applications	125
<i>Patrick Bellasi, Giuseppe Massari, William Fornaciari</i>	
Hardware Acceleration of Combined Cipher and Forward Error Correction for Low-Power Wireless Applications	133
<i>Francois Philipp, Conrad Klytta, Manfred Glesner, Elvio Dutra</i>	
A Heterogeneous Modules Interconnection Architecture For FPGA-Based Partial Dynamic Reconfiguration	140
<i>Miao He, Yanzhe Cui, Mohammad H. Mahoor, Richard M. Voyles</i>	
Power Management Techniques in an FPGA-Based WSN Node for High Performance Applications	147
<i>M. Lombardo, J. Camarero, J. Valverde, J. Portilla, E. De La Torre, T. Riesgo</i>	
Exploiting FPGA-Aware Merging of Custom Instructions for Runtime Reconfiguration	155
<i>Siew-Kei Lam, Thambipillai Srikanthan, Christopher T. Clarke</i>	
Systematic Design and Evaluation of a Scalable Reconfigurable Multiplier Scheme for HLS Environments	163
<i>Dimitris Bekiaris, Efsthios Sotiriou-Xanthopoulos, George Economakos, Dimitrios Soudris</i>	
MPSoCDK: A Framework for Prototyping and Validating MPSoC Projects on FPGAs	171
<i>Renaud Van Langendonck, Angelo Kuti Lusala, Jean-Didier Legat</i>	

A Solution to the Data Re-ordering Problem for Multi-Pipeline Streaming Applications on Clustered MPSoC	179
<i>Daniela Genius, Khouloud Zine El Abidine</i>	
Using Genetic Algorithms to Map Hard Real-Time on NoC-based Systems	187
<i>Adrian Racu, Leandro Soares Indrusiak</i>	
Fault-Tolerant Network Interface for Spatial Division Multiplexing Based Network-on-Chip	195
<i>Anup Das, Akash Kumar, Bharadwaj Veeravalli</i>	
Transport Layer Aware Design of Network Interface in Many-Core Systems	203
<i>Mohammad Fattah, Masoud Daneshlab, Pasi Liljeberg, Juha Plosila</i>	
Security Enhancements for FPGA-based MPSoCs: a Boot-to-runtime Protection Flow for an Embedded Linux-based System	210
<i>Pascal Corret, Florian Devic, Guy Gogniat, Benoit Badrignansz, Lionel Torres</i>	
Communication-Centric High Level Synthesis Metrics for Low Vertical Channel Density 3-Dimensional Networks-on-Chip	218
<i>Haoyuan Ying, Thomas Hollstein, Klaus Hofmann</i>	
Fast Integration of Hardware Accelerators for Dynamically Reconfigurable Architecture	224
<i>Clement Foucher, Fabrice Muller, Alain Giulieri</i>	
A Framework for Self-reconfigurable DCTs based on Multiobjective Optimization of the Power-Performance-Accuracy Space	231
<i>Daniel Llamocca, Marios Pattichis, Cesar Carranza</i>	
Partially Reconfigurable TVWS Transceiver for Use in UK and US Markets	237
<i>R. A. Elliot, M. A. Enderwitz, K. He, F. Darbari, L. H. Crockett, S. Weiss, R. W. Stewart</i>	
High-level Model of Sensor Architecture for Hardware and Software Design Space Exploration	243
<i>Nicolas Serna, Francois Verdier</i>	
Fast Spiking Neural Network architecture for low-cost FPGA devices	251
<i>Taras Iakymchuk, Alfredo Rosado, Jose V. Frances, Manuel Bataller</i>	
Hardware Implementation of GMDH-Type Artificial Neural Networks and its use to Predict Approximate Three-dimensional Structures of Proteins	257
<i>Andre L. S. Braga, Janier Arias-Garcia, Carlos Llanos, Marcio Dorn, Alfredo Foltran, Leandro S. Coelhox</i>	
GLB - Efficient Global Load Balancing Method for Moderating Congestion in On-Chip Networks	265
<i>Masoud Daneshlab, Masoumeh Ebrahimi, Juha Plosila</i>	
A MARTE Subset to Enable Application-Platform Co-simulation and Schedulability Analysis of NoC based Embedded Systems	270
<i>Leandro Soares Indrusiak, Imran Quadri, Ian Gray, Neil Audsley, Andrey Sadovykh</i>	
Embedded UML Design Flow to the Configurable LE1 MultiCore VLIW processor	277
<i>Mark Milward, David Stevens, Vassilios Chouliaras</i>	
Energy and Power Estimation of Coarse-Grain Reconfigurable Array based Fast Fourier Transform Accelerators	285
<i>Waqar Hussain, Tapani Ahonen, Roberto Airoidi, Jari Nurmi</i>	
Design Methodology for Fault-Tolerant Heterogeneous MPSoC under Real-Time Constraints	289
<i>Mohsin Amin, Mihkel Tagel, Gert Jervan, Thomas Hollstein</i>	
Author Index	