

2012 Proceedings of the European Solid-State Device Research Conference

(ESSDERC 2012)

**Bordeaux, France
17 – 21 September 2012**



**IEEE Catalog Number: CFP12543-PRT
ISBN: 978-1-4673-1707-8**

Table of Contents

A1L-A	PLENARY: Biopsychically Inspired Cognitive Control	
Date:	Tuesday, August 28, 2012	
Time:	09:00 - 10:00	
Room:	Casino	
Chair:	Jerzy Sasiadek	
	Biopsychically Inspired Cognitive Control for Autonomous Agents Based on Motivated Learning	N/A
	J. Jim Zhu ² , Xudan Xu ¹	
	¹ Beihang University, China; ² Ohio University, United States	
A1L-A	JOINT PLENARY: Future IC Technology	
Date:	Tuesday, September 18, 2012	
Time:	09:40 - 10:40	
Room:	Amphitheater A	
Chair:	Yann Deval; <i>IMS Lab</i>	
	Future Silicon Technology	1
	Kinam Kim	
	<i>Samsung Electronics Co., LTD., Korea, South</i>	
A3L-A	JOINT PLENARY: The Industrialization of the Silicon Photonics: Technology Road Map & Applications	
Date:	Tuesday, September 18, 2012	
Time:	14:00 - 15:00	
Room:	Amphitheater A	
Chair:	Jean-Baptiste Begueret; <i>IMS Lab</i>	
	The Industrialization of the Silicon Photonics: Technology Road Map and Applications	7
	Maurizio Zuffada	
	<i>STMicroelectronics, Italy</i>	
B1L-A	JOINT PLENARY: Facing the Challenges of 450mm Manufacturing	
Date:	Wednesday, September 19, 2012	
Time:	08:15 - 09:30	
Room:	Amphitheater A	
Chair:	Yann Deval; <i>IMS Lab</i>	
	Facing the Challenges of 450mm Manufacturing	No Paper
	Maria Marced	
	<i>TSMC, United States</i>	
B4L-A	JOINT PLENARY: Solid-State and Bio Systems Interface	
Date:	Wednesday, September 19, 2012	
Time:	14:00 - 15:00	
Room:	Amphitheater A	
Chair:	Thomas Skotnicki; <i>STMicroelectronics</i>	
	Solid-State and Biological Systems Interface	14
	Nan Sun ³ , Yong Liu ² , Ling Qin ¹ , Guangyu Xu ¹ , Donhee Ham ¹	
	¹ Harvard University, United States; ² IBM T. J. Watson Research Center, United States; ³ University of Texas at Austin, United States	

Table of Contents

C1L-A	JOINT PLENARY: Advancing Very Large Scale High Performance Heterogeneous Integration	
Date:	Thursday, September 20, 2012	
Time:	08:30 - 09:30	
Room:	Amphitheater A	
Chair:	Didier Belot; <i>STMicroelectronics</i>	
	Advancing High Performance Heterogeneous Integration Through Die Stacking	18
	Liam Madden, Ephrem Wu, Namhoon Kim, Bahareh Banijamali, Khaldoon Abugharbieh, Suresh Ramalingam, Xin Wu <i>Xilinx, Inc., United States</i>	
C4L-A	JOINT PLENARY: Graphene for Microelectronics: Can it make a difference?	
Date:	Thursday, September 20, 2012	
Time:	14:00 - 15:00	
Room:	Amphitheater A	
Chair:	Thomas Zimmer; <i>IMS Lab</i>	
	Graphene for Microelectronics: Can It Make a Difference?	25
	Max C. Lemme <i>KTH Royal Institute of Technology, Sweden</i>	
A5L-A	ESSDERC PLENARY: Nanostructure Devices for Logic & Memory and Beyond	
Date:	Tuesday, September 18, 2012	
Time:	16:30 - 17:30	
Room:	Amphitheater A	
Chair:	Carlos Mazure; <i>Soitec</i>	
	Nanostructure Devices for Logic and Memory and Beyond	28
	Sandip Tiwari <i>Cornell University, United States</i>	
B5L-A	ESSDERC PLENARY: Modeling Circuits with Spins & Magnets for All-spin Logic	
Date:	Wednesday, September 19, 2012	
Time:	15:10 - 16:10	
Room:	Amphitheater A	
Chair:	Sorin Cristoloveanu; <i>Grenoble INP</i>	
	Modeling Circuits with Spins and Magnets for All-Spin Logic	36
	Behtash Behin-Aein ¹ , Angik Sarkar ² , Supriyo Datta ² ¹ <i>GlobalFoundries Inc., United States</i> ; ² <i>Purdue University, United States</i>	
C5L-A	ESSDERC PLENARY: Organic Complementary Circuits	
Date:	Thursday, September 20, 2012	
Time:	15:10 - 16:10	
Room:	Amphitheater A	
Chair:	Cor Claeys; <i>IMEC</i>	
	Organic Complementary Circuits - Scaling Towards Low Voltage and Submicron Channel Length	41
	Hagen Klauk <i>Max Plank Institute for Solid State Research, Germany</i>	

Table of Contents

B3L-A JOINT ESSDERC/ESSCIRC Session on Compact Modeling	
Date:	Wednesday, September 19, 2012
Time:	11:00 - 12:20
Room:	Amphitheater A
Chair(s):	Hervé Jaouen; <i>STMicroelectronics</i> Christian Enz; <i>CSEM</i>
	BSIM - Industry Standard Compact MOSFET Models46
	Yogesh Singh Chauhan, Sriramkumar Venugopalan, Mohammed Ahasan Ul Karim, Sourabh Khandelwal, Navid Paydavosi, Pankaj Thakur, Ali Niknejad, Chenming Hu <i>University of California, Berkeley, United States</i>
	Evaluation of the BSIM6 Compact MOSFET Model's Scalability in 40nm CMOS Technology.....50
	Maria-Anna Chalkiadaki ¹ , Anurag Mangla ¹ , Christian C. Enz ² , Yogesh Singh Chauhan ³ , Mohammed Ahasan Ul Karim ³ , Sriramkumar Venugopalan ³ , Ali Niknejad ³ , Chenming Hu ³ ¹ <i>École Polytechnique Fédérale de Lausanne, Switzerland</i> ; ² <i>École Polytechnique Fédérale de Lausanne / Centre Suisse d'Electronique et de Microtechnique, Switzerland</i> ; ³ <i>University of California, Berkeley, United States</i>
	4-Port Isolated MOS Modeling and Extraction for mmW Applications54
	Benjamin Dormieu ² , Patrick Scheer ² , Clement Charbuillet ² , Sebastien Jan ² , Francois Danneville ¹ ¹ <i>IEMN, France</i> ; ² <i>STMicroelectronics, France</i>
C3L-A Joint ESSDERC/ESSCIRC Session on Variability / Reliability	
Date:	Thursday, September 20, 2012
Time:	11:00 - 12:20
Room:	Amphitheater A
Chairs:	François Marc; <i>University Bordeaux I</i> Angel Rodriguez Vázquez; <i>IMSE-CNM</i>
	Variability Aware Cell Library Optimization for Reliable Sub-Threshold Operation58
	Tobias Gemmeke, Maryam Ashouei <i>Holst Center / imec, Netherlands</i>
	Advancements on Reliability-Aware Analog Circuit Design62
	Bertrand Ardouin ³ , Jean-Yves Dupuy ¹ , Jean Godin ¹ , Virginie Nodjiadjim ¹ , Muriel Riet ¹ , François Marc ² , Gilles Amadou Koné ² , Sudip Ghosh ² , Brice Grandchamp ² , Cristell Maneux ² ¹ <i>III-V Lab, France</i> ; ² <i>Université de Bordeaux, France</i> ; ³ <i>XMOD Technologies, France</i>
A2L-E High Mobility Devices	
Date:	Tuesday, September 18, 2012
Time:	11:00 - 12:20
Room:	Room E2
Chairs:	Emmanuel Dubois; <i>IEMN - UMR CNRS</i> Nadine Collaert; <i>IMEC</i>
	Design Challenges for Nano-Scale Devices69
	Marc Belleville, Olivier Thomas, Alexandre Valentian, Fabien Clermidy <i>CEA-LETI, France</i>

Table of Contents

Study of Carrier Transport in Strained and Unstrained SOI Tri-Gate and Omega-Gate Si-Nanowire MOSFETs	73
Masahiro Koyama ² , Mikaël Cassé ¹ , Remi Coquand ³ , Sylvain Barraud ⁴ , Hiroshi Iwai ⁶ , Gérard Ghibaudo ⁵ , Gilles Reimbold ³ ¹ CEA LETI, France; ² CEA-LETI, France; ³ CEA-LETI-MINATEC, France; ⁴ CEA-LETI-MINATEC and CEA-INAC, France; ⁵ IMEP-LAHC, MINATEC, INPG, France; ⁶ Tokyo Institute of Technology, Japan	
Stability and Performance Optimization of InGaAs-OI and GeOI Hetero-Channel SRAM Cells	77
Vita Pi-Ho Hu, Ming-Long Fan, Pin Su, Ching-Te Chuang <i>National Chiao Tung University, Taiwan</i>	

A2L-F High-k Dielectrics and Applications

Date:	Tuesday, September 18, 2012
Time:	11:00 - 12:20
Room:	Room F1
Chairs:	Emmanuel Augendre; Anton Bauer; <i>Fraunhofer</i>
Two-Step Annealing Effects on Ultrathin EOT Higher-K (K = 40) ALD-HfO2 Gate Stacks	81
Yukinori Morita, Shinji Migita, Wataru Mizubayashi, Meishoku Masahara, Hiroyuki Ota <i>Advanced Industrial Science and Technology, Japan</i>	
Thin Germanium Dioxide Film with a High Quality Interface Formed in a Direct Neutral Beam Oxidation Process	85
Akira Wada ¹ , Seiji Samukawa ¹ , Rui Zhang ² , Shinichi Takagi ² ¹ Tohoku University, Japan; ² University of Tokyo, Japan	
(100)- and (110)-Oriented nMOSFETs with Highly Scaled EOT in La-Silicate/Si Interface for Multi-Gate Architecture	89
Takamasa Kawanago, Kuniyuki Kakushima, Parhat Ahmet, Yoshinori Kataoka, Akira Nishiyama, Nobuyuki Sugii, Kazuo Tsutsui, Kenji Natori, Takeo Hattori, Hiroshi Iwai <i>Tokyo Institute of Technology, Japan</i>	
CMOS Compatible ALD High-K Double Slot Grating Couplers for on-Chip Optical Interconnects	93
Maziar M. Naini, Christoph Henkel, Gunnar B. Malm, Mikael Östling <i>KTH Royal Institute of Technology, Sweden</i>	

A2L-G Emerging Device Modeling

Date:	Tuesday, September 18, 2012
Time:	11:00 - 12:20
Room:	Room F2
Chairs:	Massimo Rudan; <i>Università di Bologna</i> Cristell Maneux; <i>IMS Bordeaux</i>
Transport in Amorphous Materials with Applications to Phase-Change Memories	97
Carlo Jacoboni ¹ , Enrico Piccinini ² , Fabrizio Buscemi ² ¹ Università degli Studi di Modena e Reggio Emilia, Italy; ² Università di Bologna, Italy	
Geometry Based Resistance Model for Phase Change Memory	101
K. C. Kwong, Philip K. T. Mok, Mansun Chan <i>Hong Kong Univeristy of Science and Technology, Hong Kong</i>	

Table of Contents

Drain-Conductance Optimization in Nanowire TFETs	105
Elena Gnani, Susanna Reggiani, Antonio Gnudi, Giorgio Baccharani <i>Università di Bologna, Italy</i>	

A4L-E Variability

Date: Tuesday, September 18, 2012
Time: 15:10 - 16:10
Room: Room E2
Chairs: Hervé JAOUEN; *STMicroelectronics*
Ray Huetting

Comprehensive Statistical Comparison of RTN and BTI in Deeply Scaled MOSFETs by Means of 3D 'Atomistic' Simulation	109
Salvatore Maria Amoroso, Louis Gerrer, Stanislav Markov, Fikru Adamu-Lema, Asen Asenov <i>University of Glasgow, United Kingdom</i>	

Statistical Variability in 14-nm Node SOI FinFETs and its Impact on Corresponding 6T-SRAM Cell Design.....	113
Xingsheng Wang ² , Binjie Cheng ² , Andrew Brown ¹ , Campbell Millar ³ , Asen Asenov ² ¹ <i>Gold Standard Simulations Ltd., United Kingdom</i> ; ² <i>University of Glasgow, United Kingdom</i> ; ³ <i>University of Glasgow, Gold Standard Simulations Ltd., United Kingdom</i>	

Sensitivity-Based Investigation of Threshold Voltage Variability in 32-nm Flash Memory Cells	117
Valentina Bonfiglio, Giuseppe Iannaccone <i>Università degli Studi di Pisa, Italy</i>	

A4L-F Advanced FETs

Date: Tuesday, September 18, 2012
Time: 15:10 - 16:10
Room: Room F1
Chairs: Giorgio Baccharani; *University of Bologna*
Max Lemme; *KTH*

Scaling of Trigate Nanowire (NW) MOSFETs Down to 5 nm Width: 300 K Transition to Single Electron Transistor, Challenges and Opportunities	121
Veeresh Deshpande ² , Sylvain Barraud ² , Xavier Jehl ² , Romain Wacquez ² , Maud Vinet ² , Remi Coquand ¹ , Benoit Roche ² , Benoit Voisin ² , François Triozon ¹ , Christian Vizioz ² , Lucie Tosti ² , Bernard Previtali ² , Pierre Perreau ² , Thierry Poiroux ² , Marc Sanquer ² , Olivier Faynot ¹ ¹ <i>CEA-LETI-MINATEC, France</i> ; ² <i>CEA-LETI-MINATEC and CEA-INAC, France</i>	

Active Strain Modulation in Field Effect Devices	125
Tom van Hemert, Raymond Huetting <i>Universiteit Twente, Netherlands</i>	

Table of Contents

<hr/>	
A4L-G	Thin-Film Transistors
<hr/>	
Date:	Tuesday, September 18, 2012
Time:	15:10 - 16:10
Room:	Room F2
Chairs:	Peter Ashburn; <i>Southampton University</i> Ryoichi Ishihara; <i>TU Delft</i>
	Static and Low Frequency Noise Characterization of Densely Packed CNT-TFTs 129
	Min-Kyu Joo ¹ , Un Jeong Kim ⁴ , Dae-Young Jeon ¹ , So Jeong Park ¹ , Mireille Mouis ¹ , Gyu-Tae Kim ³ , Gérard Ghibaudo ² <i>¹IMEP-LAHC, France; ²IMEP-LAHC, MINATEC, INPG, France; ³Korea University, Korea, South; ⁴Samsung Advanced Institute of Technology, Korea, South</i>
	Mechanically Flexible Double Gate a-IGZO TFTs..... 133
	Niko Münzenrieder, Christoph Zysset, Thomas Kinkeldei, Luisa Petti, Giovanni A. Salvatore, Gerhard Tröster <i>ETH Zurich, Switzerland</i>
	Top-Down Fabricated ZnO Nanowire Transistors for Application in Biosensors 137
	Suhana Mohamed Sultan, Kai Sun, Maurits de Planque, Peter Ashburn, Harold Chong <i>University of Southampton, United Kingdom</i>
<hr/>	
B2L-E	Novel Thin Film Integration
<hr/>	
Date:	Wednesday, September 19, 2012
Time:	09:40 - 10:40
Room:	Room E2
Chairs:	Jurriaan Schmitz; <i>University of Twente</i> Simon Deleonibus; <i>CEA</i>
	Manufacturing Aspects of an Ultra-Thin Chip Technology 141
	Evangelos Angelopoulos, Muhammad Al-Shahed, Wolfgang Appel, Stefan Endler, Saleh Ferwana, Christine Harendt, Mahadi-UI Hassan, Horst Rempp, Martin Zimmermann, Joachim Burghartz <i>Institute for Microelectronics Stuttgart - IMS CHIPS, Germany</i>
	Epitaxial Growth of Large-Area p+n Diodes at 400 °C by Aluminum-Induced Crystallization 145
	Agata Sakic, Lin Qi, Tom Scholtes, Johan van der Cingel, Lis Nanver <i>Technische Universiteit Delft, Netherlands</i>
	Current-Voltage Characteristics of Vertical Diodes for Next Generation Memories 149
	Hokyun An ¹ , Kongsoo Lee ¹ , Yoongoo Kang ¹ , Seonghoon Jeong ¹ , Wonseok Yoo ¹ , Jaejong Han ¹ , Bonghyun Kim ¹ , Hanjin Lim ¹ , Seokwoo Nam ¹ , Gitae Jeong ¹ , Hokyung Kang ¹ , Chilhee Chung ² , Byoungdeog Choi ³ <i>¹Samsung Electronics, Semiconductor R&D Center, Korea, South; ²Semiconductor R&D Center, Samsung Electronics Co., Korea, South; ³Sungkyunkwan University, Korea, South</i>

Table of Contents

B2L-F Tunneling Devices	
Date:	Wednesday, September 19, 2012
Time:	09:40 - 10:40
Room:	Room F1
Chairs:	Francois Andrieu; <i>CEA-Leti</i> Jean-Pierre Colinge; <i>Tyndall</i>
	Si Tunneling Transistors with High on-Currents and Slopes of 50 mV/dec Using Segregation Doped NiSi₂ Tunnel Junctions 153
	Lars Knoll ¹ , Qing-Tai Zhao ¹ , Stefan Trelenkamp ¹ , Anna Schäfer ¹ , Konstantin Bourdelle ² , Siegfried Mantl ¹ ¹ <i>Forschungszentrum Jülich, Germany</i> ; ² <i>SOITEC, France</i>
	A Comparative Analysis of Tunneling FET Circuit Switching Characteristics and SRAM Stability and Performance 157
	Yin-Nien Chen, Ming-Long Fan, Vita Pi-Ho Hu, Ming-Fu Tsai, Chia-Hao Pao, Pin Su, Ching-Te Chuang <i>National Chiao Tung University, Taiwan</i>
	Tunnel FET with Non-Uniform Gate Capacitance for Improved Device and Circuit Level Performance..... 161
	Cem Alper, Luca De Michielis, Nilay Dagtekin, Livio Lattanzio, Adrian M. Ionescu <i>École Polytechnique Fédérale de Lausanne, Switzerland</i>
B2L-G MEMS / OTFT	
Date:	Wednesday, September 19, 2012
Time:	09:40 - 10:40
Room:	Room F2
Chairs:	Piotr Grabiec; <i>Inst. of Electron Technology</i> Fiodor Sizov; <i>National Academy of Sciences of Ukraine</i>
	From FinFET to Nanowire ISFET 165
	Michal Zaborowski, Daniel Tomaszewski, Piotr Dumania, Piotr Grabiec <i>Institute of Electron Technology, Poland</i>
	Micro- and Nano-Link Ultra-Low Power Heaters for Sensors 169
	Alfons Groenland, Elizaveta Vereshchagina, Alexey Kovalgin, Rob Wolters, Han Gardeniers, Jurriaan Schmitz <i>Universiteit Twente, Netherlands</i>
	High Performance Printed N and P-Type OTFTs for Complementary Circuits on Plastic Substrate..... 173
	Stephanie Jacob ¹ , Mohammed Benwadih ¹ , Jacqueline Bablet ¹ , Isabelle Chartier ¹ , Romain Gwoziecki ¹ , Sahel Abdinia ³ , Eugenio Cantatore ³ , Lidia Maddiona ⁴ , Francesca Tramontana ⁴ , Giorgio Maiellaro ⁵ , Luigi Mariucci ² , Giuseppe Palmisano ⁵ , Romain Coppard ¹ ¹ <i>CEA-LITEN, France</i> ; ² <i>CNR-IMM, Italy</i> ; ³ <i>Eindhoven University of Technology, Netherlands</i> ; ⁴ <i>STMicroelectronics, Italy</i> ; ⁵ <i>Università di Catania, Italy</i>

Table of Contents

B3L-F	High-frequency Transistors	
Date:	Wednesday, September 19, 2012	
Time:	11:00 - 12:20	
Room:	Room F1	
Chairs:	Nathalie Malbert; <i>IMS - Bordeaux</i> Gilles Dambrine; <i>IEMN</i>	
	A Gate-Last In0.53Ga0.47As Channel FinFET with Molybdenum Source/Drain Contacts	177
	Xingui Zhang, Hua Xin Guo, Xiao Gong, Yee-Chia Yeo <i>National University of Singapore, Singapore</i>	
	Complementary RF-LDMOS Transistors Realized with Standard CMOS Implantations	181
	Andreas Mai, Holger Rucker <i>IHP, Germany</i>	
	TCAD Degradation Modeling for LDMOS Transistors	185
	Susanna Reggiani ² , Gaetano Barone ² , Elena Gnani ² , Antonio Gnudi ² , Stefano Poli ¹ , Ming-Yeh Chuang ¹ , Weidong Tian ¹ , Rick Wise ¹ ¹ Texas Instruments Incorporated, United States; ² Università di Bologna, Italy	
	Pulsed I(V) - Pulsed RF Measurement System for Microwave Device Characterization with 80ns/45GHz	189
	Mario Weiß, Sébastien Fregonese, Marco Santorelli, Amit Kumar Sahoo, Cristell Maneux, Thomas Zimmer <i>Université de Bordeaux, France</i>	
B3L-G	DRAMs and SRAMs	
Date:	Wednesday, September 19, 2012	
Time:	11:00 - 12:20	
Room:	Room F2	
Chairs:	Andreas Schenk; <i>ETH Zurich</i> Isodiana Crupi; <i>CNR - IMM Catania (Italy)</i>	
	Novel Deep Trench Buried-Body-Contact (DBBC) of 4F2 Cell for Sub 30nm DRAM Technology	193
	Youngseung Cho ¹ , Yoosang Hwang ² , Huijung Kim ² , Eunok Lee ² , Soojin Hong ² , Hyunwoo Chung ² , Daeik Kim ² , Jiyoung Kim ² , Yongchul Oh ² , Hyeongsun Hong ² , Gyo-Young Jin ² , Chilhee Chung ² ¹ Samsung Electronics Co., LTD., Korea, South; ² Semiconductor R&D Center, <i>Samsung Electronics Co., Korea, South</i>	
	Z²-Fet Used as 1-Transistor High-Speed DRAM	197
	Jing Wan ³ , Cyrille Le Royer ² , Alex Zaslavsky ¹ , Sorin Cristoloveanu ³ ¹ Brown University, United States; ² CEA-LETI-MINATEC, France; ³ IMEP- <i>INPG/Minatec, France</i>	
	A 5.61 pJ, 16 Kb 9T SRAM with Single-Ended Equalized Bitlines and Fast Local Write-Back for Cell Stability Improvement	201
	Qi Li, Bo Wang, Tony Kim <i>Nanyang Technological University, Singapore</i>	
	An Advanced Statistical Compact Model Strategy for SRAM Simulation at Reduced VDD	205
	Plamen Asenov ² , Dave Reid ¹ , Scott Roy ² , Campbell Millar ³ , Asen Asenov ² ¹ Gold Standard Simulations Ltd., United Kingdom; ² University of Glasgow, United Kingdom; ³ University of Glasgow, Gold Standard Simulations Ltd., United Kingdom	

Table of Contents

B7L-E	Mobility Characterization and Parameter Extraction in Advanced MOSFETs
Date:	Wednesday, September 19, 2012
Time:	16:30 - 18:10
Room:	Room E2
Chairs:	Henryk Przewlocki; <i>Inst. of Electron Technology</i> Stefan Bengtsson; <i>Chalmers University of Technology</i>
	Multibranch Mobility Characterization: Evidence of Carrier Mobility Enhancement by Back-Gate Biasing in FD-SOI MOSFET209
	Carlos Navarro ⁶ , Noel Rodriguez ⁵ , Luca Donetti ⁵ , Akiko Ohata ⁴ , Francisco Gamiz ⁵ , François Andrieu ¹ , Olivier Faynot ¹ , Claire Fenouillet-Berangerand ² , Sorin Cristoloveanu ³ ¹ CEA-LETI-MINATEC, France; ² CEA-LETI-MINATEC / STMicroelectronics, France; ³ IMEP-INPG/Minatec, France; ⁴ Osaka City University, Japan; ⁵ Universidad de Granada - CITIC, Spain; ⁶ Universidad de Granada - CITIC / IMEP-Minatec, Spain
	The Role of the Temperature on the Scattering Mechanisms Limiting the Electron Mobility in Metal-Oxide-Semiconductor Field-Effect-Transistors Fabricated on (110) Silicon-Oriented Wafers213
	Philippe Gaubert, Akinobu Teramoto, Shigetoshi Sugawa, Tadahiro Ohmi <i>Tohoku University, Japan</i>
	New Parameter Extraction Method Based on Split C-V for FDSOI MOSFETs217
	Imed Ben Akkez ⁴ , Antoine Cros ⁵ , Claire Fenouillet-Beranger ¹ , Frederic Boeuf ⁵ , Quentin Rafhay ² , Francis Balestra ² , Gérard Ghibaudo ³ ¹ CEA-LETI/STMicroelectronics (Crolles), France; ² IMEP-LAHC, France; ³ IMEP-LAHC, MINATEC, INPG, France; ⁴ IMEP-LaHc/STMicroelectronics, France; ⁵ STMicroelectronics, France
	Methodology for Extracting the Characteristic Capacitances of a Power MOSFET Transistor, Using Conventional on-Wafer Testing Techniques.....221
	Christoph Kerner, Ivan Ciofi, Thomas Chiarella, Stefaan Van Huylbroeck <i>IMEC, Belgium</i>
B7L-F	Advanced Photodetectors
Date:	Wednesday, September 19, 2012
Time:	16:30 - 18:10
Room:	Room F1
Chairs:	Denis Flandre; <i>UC Lovain</i> Lorenzo Faraone; <i>Univ. Western Australia</i>
	A Gate Modulated Avalanche Bipolar Transistor in 130nm CMOS Technology.....226
	Robert Henderson, Eric A. G. Webster, Richard J. Walker <i>University of Edinburgh, United Kingdom</i>
	Low-Noise and Large-Area CMOS SPADs with Timing Response Free from Slow Tails.....230
	Danilo Bronzi ² , Federica Villa ² , Simone Bellisai ² , Bojan Markovic ² , Simone Tisa ² , Alberto Tosi ² , Franco Zappa ² , Sascha Weyers ¹ , Daniel Durini ¹ , Werner Brockherde ¹ , Uwe Paschen ¹ ¹ Fraunhofer IMS, Germany; ² Politecnico di Milano, Italy
	Extreme Temperature 4H-SiC Metal-Semiconductor-Metal Ultraviolet Photodetectors.....234
	Wei-Cheng Lien ³ , Albert P. Pisano ³ , Dung-Sheng Tsai ¹ , Jr-Hau He ¹ , Debbie G. Senesky ² ¹ National Taiwan University, Taiwan; ² Stanford University, United States; ³ University of California, Berkeley, United States

Table of Contents

A Silicon Photomultiplier with >30% Detection Efficiency from 450-750nm and 11.6µm Pitch NMOS-Only Pixel with 21.6% Fill Factor in 130nm CMOS.....238
 Eric A. G. Webster², Richard J. Walker², Robert Henderson², Lindsay A. Grant¹
¹STMicroelectronics, United Kingdom; ²University of Edinburgh, United Kingdom

B7L-G Analog/Low Power Devices

Date: Wednesday, September 19, 2012
 Time: 16:30 - 18:10
 Room: Room F2
 Chairs: Kazu Ishimaru; *Toshiba*
 Thomas Ernst; *CEA-LETI*

Addressing Healthcare Challenges Using Semiconductor Technology Tools and Approaches No paper
 Peter Peumans
IMEC, Belgium

Low-Power DRAM-Compatible Replacement Gate High-k/Metal Gate Stacks242
 Romain Ritzenthaler¹, Tom Schram¹, Erik Bury², Jerome Mitard¹, Lars-Ake Ragnarsson¹, Guido Groeseneken², Naoto Horiguchi¹, Aaron Thean¹, Alessio Spessot³, Christian Caillat³, Vidya Srividya³, Pierre Fazan³
¹IMEC, Belgium; ²IMEC - Katholieke Universiteit Leuven, Belgium; ³Micron Technology, Belgium

On the UTBB SOI MOSFET Performance Improvement in Quasi-Double-Gate Regime.....246
 Valeriya Kilchytska², Denis Flandre², François Andrieu¹
¹CEA-LETI-MINATEC, France; ²Université catholique de Louvain, Belgium

C2L-E Emerging Devices

Date: Thursday, September 20, 2012
 Time: 09:40 - 10:40
 Room: Room E2
 Chairs: Stephen Hall; *University of Liverpool*
 Anthony O'Neill; *Newcastle University*

An Integration Approach for Graphene Double-Gate Transistors.....250
 Sam Vaziri¹, Anderson Smith¹, Christoph Henkel¹, Mikael Östling¹, Max C. Lemme¹, Grzegorz Lupina², Gunther Lippert², Jaroslaw Dabrowski², Wolfgang Mehr²
¹KTH Royal Institute of Technology, Sweden; ²Leibniz-Institut für Innovative Mikroelektronik, IHP, Germany

MTJ-Based Implication Logic Gates and Circuit Architecture for Large-Scale Spintronic Stateful Logic Systems254
 Hiwa Mahmoudi, Viktor Sverdlov, Siegfried Selberherr
Technische Universität Wien - IUE, Austria

Resistive Switching Memory Using Titanium-Oxide Nanoparticle Films258
 Emanuele Verrelli², Dimitris Tsoukalas², Pascal Normand³, Nikos Boukos³, Alistair H. Kean¹
¹Mantis Deposition Ltd., United Kingdom; ²National Technical University of Athens, Greece; ³NCSR Demokritos, Greece

Table of Contents

C2L-F Characterization of Aging and Failure Mechanisms	
Date:	Thursday, September 20, 2012
Time:	09:40 - 10:40
Room:	Room F1
Chairs:	Montserrat Nafria; <i>UAB</i> Joachim Burghartz; <i>Institut für Mikroelektronik Stuttgart</i>
	An Array-Based Chip Lifetime Predictor Macro for Gate Dielectric Failures in Core and IO FETs.....262
	Pulkit Jain ² , John Keane ¹ , Chris Kim ² ¹ <i>Intel Corporation, United States</i> ; ² <i>University of Minnesota, United States</i>
	Unified Characterization of RTN and BTI for Circuit Performance and Variability Simulation266
	Nuria Ayala, Javier Martin-Martinez, Rosana Rodriguez, Montse Nafria, Xavier Aymerich <i>Universitat Autònoma de Barcelona, Spain</i>
	Kink Effect Characterization in AlGaN/GaN HEMTs by DC and Drain Current Transient Measurements.....270
	Laurent Brunel ² , Nathalie Malbert ² , Arnaud Curutchet ² , Nathalie Labat ² , Benoit Lambert ¹ ¹ <i>United Monolithic Semiconductors, France</i> ; ² <i>Université de Bordeaux, France</i>
C3L-F Resistive Memories	
Date:	Thursday, September 20, 2012
Time:	11:00 - 12:20
Room:	Room F1
Chairs:	Andrea Lacaita; <i>Politecnico di Milano</i> Fernanda Irrera; <i>Università Roma La Sapienza</i>
	Random Telegraph Signal Noise Properties of HfOx RRAM in High Resistive State.....274
	Francesco Maria Puglisi ² , Paolo Pavan ² , Andrea Padovani ² , Luca Larcher ² , Gennadi Bersuker ¹ ¹ <i>SEMATECH, United States</i> ; ² <i>Università degli Studi di Modena e Reggio Emilia, Italy</i>
	On the Impact of Ag Doping on Performance and Reliability of GeS₂-Based Conductive Bridge Memories278
	Elisa Vianello ² , Carlo Cagli ² , Gabriel Molas ² , Emeline Souchier ² , Philippe Blaise ² , Catherine Carabasse ² , Guillaume Rodriguez ² , V. Jousseume ² , Barbara De Salvo ³ , Florian Longnos ¹ , Faiz Dahmani ¹ , Pascal Verrier ¹ , Damien Bretegnier ¹ , Jacques Liebault ¹ ¹ <i>Altis Semiconductor, France</i> ; ² <i>CEA-LETI, France</i> ; ³ <i>CEA-LETI-MINATEC, France</i>
	Analysis of the Effect of Cell Parameters on the Maximum RRAM Array Size Considering Both Read and Write282
	Leqi Zhang ² , Stefan Cosemans ¹ , Dirk Wouters ² , Guido Groeseneken ² , Malgorzata Jurczak ¹ ¹ <i>IMEC, Belgium</i> ; ² <i>IMEC - Katholieke Universiteit Leuven, Belgium</i>

Table of Contents

Carbon-Doped Ge₂Sb₂Te₅ Phase-Change Memory Devices Featuring Reduced Reset Current and Power Consumption.....286
 Quentin Hubert¹, Carine Jahan¹, Alain Toffoli¹, Gabriele Navarro¹, Sandhya Chandrashekar¹, Pierre Noé¹, Véronique Sousa¹, Luca Perniola¹, Jean-François Nodin¹, Alain Persico¹, Sylvain Maitrejean¹, Anne Roule¹, Ewen Henaff¹, Magali Tessaire¹, Paola Zuliani³, Roberto Annunziata³, Gilles Reimbold¹, Georges Pananakakis², Barbara De Salvo¹
¹CEA-LETI-MINATEC, France; ²IMEP - LAHC, France; ³STMicroelectronics, Italy

C3L-G Quantum Transport

Date: Thursday, September 20, 2012

Time: 11:00 - 12:20

Room: Room F2

Chairs: Denis Rideau; *STMicroelectronics*
 David Esseni; *University of Udine*

Transport Properties of Strained Silicon Nanowires.....290
 Yann Michel Niquet³, Christophe Delerue², Viet Hung Nguyen³, Christophe Krzeminski², François Triozon¹
¹CEA-LETI-MINATEC, France; ²IEMN, France; ³SP2M, France

Tin Nanowire Field Effect Transistor294
 Lida Ansari³, Giorgos Fagas², James C. Greer¹
¹Tyndall National Institute, Ireland; ²Tyndall National Institute, University College Cork, Ireland; ³University College Cork, Tyndall National institute, Ireland

Effects of Disorder on Transport Properties of Extremely Scaled Graphene Nanoribbons298
 Mirko Poljak¹, Emil Song¹, Minsheng Wang¹, Tomislav Suligoj², Kang Wang¹
¹University of California, Los Angeles - DRL, United States; ²University of Zagreb - FER-ZEMRIS, Croatia

C6L-E GaN-based Power Switches

Date: Thursday, September 20, 2012

Time: 16:30 - 17:50

Room: Room E2

Chairs: Gaudenzio Meneghesso; *University of Padova*
 Tetsuya Suemitsu; *Tohoku University*

High Temperature Behaviour of GaN-on-Si High Power MISHEMT Devices302
 Dirk Wellekens, Rafael Venegas, Xuanwu Kang, Mohammed Zahid, Tian-Li Wu, Denis Marcon, Puneet Srivastava, Marleen Van Hove, Stefaan Decoutere
IMEC, Belgium

High Voltage Low Ron In-situ SiN/Al_{0.35}GaN_{0.65}/GaNon-Si Power HEMTs Operation Up to 300 °C306
 Abel Fontseré¹, Amador Pérez-Tomás¹, Phillippe Godignon¹, Jose Millán¹, John M. Parsey², Peter Moens²
¹IMB-CNM-CSIC, Spain; ²On-Semiconductors, Belgium

Critical Gate Module Process Enabling the Implementation of a 50A/600V AlGaIn/GaN MOS-HEMT310
 Sameh Khalil², Rongming Chu², Ray Li², Danny Wong², Scott Newell², Xu Chen², Mary Chen², Daniel Zehnder², Samuel Kim², Andrea Corrión², Brian Hughes², Karim Boutros², Chandra Namuduri¹
¹General Motors, United States; ²HRL Laboratories, LLC, United States

Table of Contents

Scaling of InAlN/GaN Power Transistors	314
Daniel Piedra ² , Hyung-Seok Lee ² , Tomas Palacios ² , Xiang Gao ¹ , Shiping Guo ¹ <i>¹IQE RF LLC, United States; ²Massachusetts Institute of Technology, United States</i>	

C6L-F Semi-classical Transport

Date: Thursday, September 20, 2012
 Time: 16:30 - 17:50
 Room: Room F1
 Chairs: Bernd Meinerzhagen; *TU Braunschweig*
 Tibor Grasser; *Vienna University of Technology*

Deterministic Simulation of 3D and Quasi-2D Electron and Hole Systems in SiGe Devices	318
Christoph Jungemann ¹ , Anh-Tuan Pham ³ , Sung-Min Hong ² , Bernd Meinerzhagen ⁴ <i>¹RWTH Aachen University, Germany; ²Samsung, United States; ³Synopsys Inc., United States; ⁴Technische Universität Braunschweig, Germany</i>	

A Multi-Subband Monte Carlo Study of Electron Transport in Strained SiGe N-Type FinFETs	322
Daniel Lizzit ¹ , Pierpaolo Palestri ¹ , David Esseni ¹ , Francesco Conzatti ² , Luca Selmi ¹ <i>¹Università degli studi di Udine, Italy; ²University of Udine, Italy</i>	

Electron Transport in Germanium Junctionless Nanowire Transistors	326
Pedram Razavi, Giorgos Fagas, Isabelle Ferain, Ran Yu, Samaresh Das <i>Tyndall National Institute, University College Cork, Ireland</i>	

C6L-G Low Frequency Noise in Next Generation FET Devices

Date: Thursday, September 20, 2012
 Time: 16:30 - 17:50
 Room: Room F2
 Chairs: Paolo Pavan; *Universita degli Studi di Modena e Reggio Emilia*
 Gunnar Malm; *KTH Royal Institute of Technology*

Low-Frequency Noise Assessment of the Transport Mechanisms in SiGe Channel Bulk FinFETs	330
Tommaso Romeo ¹ , Luigi Pantisano ¹ , Eddy Simoen ¹ , Raymond Krom ¹ , Mitsuhiro Togo ¹ , Naoto Horiguchi ¹ , Jerome Mitard ¹ , Aaron Thean ¹ , Guido Groeseneken ² , Cor Claeys ¹ , Felice Crupi ³ <i>¹IMEC, Belgium; ²IMEC - Katholieke Universiteit Leuven, Belgium; ³Università della Calabria, Italy</i>	

Impact of Front-Back Gate Coupling on Low Frequency Noise in 28 nm FDSOI MOSFETs	334
Christoforos Theodorou ¹ , Eleftherios Ioannidis ² , Sebastien Haendler ⁴ , Nicolas Planes ⁴ , Franck Arnaud ⁴ , Jalal Jomaah ² , Charalabos Dimitriadis ¹ , Gérard Ghibaudo ³ <i>¹Aristotle University of Thessaloniki, Greece; ²IMEP-LAHC, MINATEC, France; ³IMEP-LAHC, MINATEC, INPG, France; ⁴STMicroelectronics, France</i>	

On the Correlation Between the Retention Time of FBRAM and the Low-Frequency Noise of UTBOX SOI nMOSFETs	338
Eddy Simoen ¹ , Marc Aoulaiche ¹ , Anabela Veloso ¹ , Gosja Jurczak ¹ , Cor Claeys ¹ , Abraham Luque Rodríguez ³ , Juan Antonio Jiménez Tejada ³ , Luciano Mendes Almeida ⁴ , Maria Gloria C. Andrade ⁴ , Christian Caillat ² , Pierre Fazan ² <i>¹IMEC, Belgium; ²Micron Technology, Belgium; ³Universidad de Granada, Spain; ⁴Universidade de São Paulo, Brazil</i>	

Effect of Substrate Bias on Frequency Dependence of MOSFET Noise Intensity	342
Kenji Ohmori, Ranga Hettiarachchi, Keisaku Yamada <i>University of Tsukuba, Japan</i>	