

2012 25th Symposium on Integrated Circuits and Systems Design

(SBCCI 2012)

**Brasilia, Brazil
30 August – 2 September 2012**



**IEEE Catalog Number: CFP12237-PRT
ISBN: 978-1-4673-2606-3**

SBCCI 2012 List of Papers

Hybrid-on-Chip communication architecture for dynamic MP-SoC protection

Johanna Sepilveda, Guy Gogniat, Ricardo Pires, Wang J. Chau, and Marius Strum

FPGA design for real time flaw detection on edges using the LEDges technique

Ygo N. Batista, Cristiano C. de Araújo, and Abel G. S. Filho

Application-Specific Network-on-Chip Synthesis with Topology-Aware Floorplanning

Bo Huang, Song Chen, Wei Zhong, and Takeshi Yoshimura

Robust Modular Bulk Built-In Current Sensors for Detection of Transient Faults

Frank S. Torres and Rodrigo P. Bastos

Memory and communication driven spatio-temporal scheduling on MPSoCs

Zubair W. Bhatti, Narasinga R. Miniskar, Davy Preuveneers, Roel Wuyts, Yolande Berbers, and Francky Catthoor

Design-Oriented Delay Model for CMOS Inverter

Felipe S. Marranghelo, André I. Reis, and Renato P. Ribas

Extended use of Pseudo-Flash Reset Technique for an Active Pixel with Logarithmic Compressed Response

Carlos A. de M. Cruz, Israel L. Marinho, and Davies W. de L. Monteiro

Yield Optimization for Low Power Current Controlled Current Conveyor

Zia Abbas, Marat Yakupov, Mauro Olivieri, Andreas Ripp, and Gunter Strobe

FPGA-based Digital Direct-Conversion Transceiver for Nuclear Magnetic Resonance Systems

Cecil A. R. de A. Melo and Ricardo E. de Souza

A 50MHz-1GHz Wideband Low Noise Amplifier in 130nm CMOS Technology

Henrique L. A. Pimentel and Sergio Bampi

Power Consumption Reduction in MPSoCs through DFS

Thiago R. da Rosa, Vivian Larréa, Ney L. V. Calazans, and Fernando G. Moraes

FPGA Design Methodology for DSP Industrial Applications – A Case Study of a Three-Phase Positive-Sequence Detector

Paulo S. B. Nascimento, Helder E. P. Souza, Francisco A. S. Neves, and Marco A. O. Domingues

A Low Complexity Lossless Data Compressor IP-Core for Satellite Images

Yuri G. Costa, José A. G. de Lima, and Guilherme Navarro

DPA insensitive voltage regulator for contact smart cards

Hugo Hernandez, Jonathan Scott, and Wilhelmus van Noije

A Formally Verified Deadlock-Free Routing Function in a Fault-Tolerant NoC Architecture

Abdulaziz Alhussien, Nader Bagherzadeh, Freek Verbeek, Bernard van Gastel, and Julien Schmaltz

On-chip 4to20mA reconfigurable current loop trasnmitter for smart sensor applications

Jefferson D. B. Soldera, Julio C. Saldaña, César G. Penteado, Hugo D. Hernandez, Raul Acosta, Fernando C. Porras, Marcos A. Valério, Angélica dos Anjos, and Paulo H. Trevisan

Multi-Bit Flip-Flop Usage Impact on Physical Synthesis

Cristiano Santos, Ricardo Reis, Guilherme Godoi, Marcos Barros, and Fabio Duarte

Partitioning-based Wirelength Estimation Technique for Y-Routing

Tuhina Samanta, Hafizur Rahaman, and Parthasarathi Dasgupta

A Very Low Power Area Efficient CMOS Only Bandgap Reference

Edgar M. C. Galeano, Alfredo Olmos, and Andre L. V. Boas

Current-Mode Analog Integrated Circuit for Focal-Plane Image Compression

Fernanda D. V. R. Oliveira, Hugo L. Haas, José G. R. C. Gomes, and Antonio Petraglia

Topological Impact on Latency and Throughput: 2D versus 3D NoC Comparison

Yan Ghidini, Thais Webber, Edson Moreno, Ivan Quadros, Rubem Fagundes, and César Marcon

Differential Mixer with NMOS/PMOS Stack at Switching Stage

Everson Martins, Matheus A. Alejandro, and Thaís V. Fogaca

A PLL for clock generation with automatic frequency control under TID effects

Ricardo V. Dallasen, Gilson I. Wirth, and Thiago H. Both

A temperature compensated CMOS relaxation oscillator for low power applications

Jefferson D. B. Soldera, Michael T. Berens, and Alfredo Olmos

Hardware Pipelining of Runtime-Detected Loops

Joao Bispo, João M. P. Cardoso, and Jose Monteiro

Return-to-One Protocol for Reducing Static Power in C-elements of QDI Circuits Employing m-of-n Codes

Matheus T. Moreira, Ricardo A. Guazzelli, and Ney L. V. Calazans

A Pragma Based Approach for mapping MATLAB Applications on a Coarse Grained Reconfigurable Architecture

Omer Malik and Ahmed Hemani

High Throughput Hardware Design for the Adaptive Loop Filter of the Emerging HEVC Video Coding

Fabiane Rediess, Cássio Cristani, Pargles Dall'Oglio, Marcelo Porto, and Luciano Agostini

Hardware and Software Co-Design for the AAC Audio Decoder

Renato C. Sampaio, Pedro de A. Berger, and Ricardo P. Jacobi

Top-down Design for Low power Multi-bit Sigma-Delta Modulator

Heiner A. Cubas and João N. Soares Júnior

Communication software synthesis from UML-ESL models

Thiago Cardoso, Edna Barros, Bruno Prado, and Andre Aziz

Heterogeneous System-Level Modeling for Small and Medium Enterprises

Seyed H. A. Niaki, Gilmar S. Beserra, Nikolaj Andersen, Mathias Verdon, and Ingo Sander

A 65nm CMOS 60GHz Class F-E Power Amplifier for WPAN Applications

Sophie Dréan, Nathalie Deltimple, Eric Kerhervé, Baudouin Martineau, and Didier Belot

NSP Kernel Finder - A Methodology to Find and to Build Non-Series-Parallel Transistors Arrangements

Vinicius N. Possani, Felipe S. Marques, Leomar S. da Rosa Junior, Vinicius Callegaro, André I. Reis, and Renato P. Ribas

Kernel Analysis for Architecture Design Trade Off in Convolution-Based Image Filtering

Jones Y. Mori, Carlos H. Llanos, and Pedro A. Berger