

**2012 IEEE 23rd International
Conference on
Application-Specific Systems,
Architectures and Processors**

(ASAP 2012)

**Delft, Netherlands
9 – 11 July 2012**



**IEEE Catalog Number: CFP12063-PRT
ISBN: 978-1-4673-2243-0**

**2012 IEEE 23rd International
Conference
on Application-Specific Systems,
Architectures and Processors**

ASAP 2012

Table of Contents

Message from the Conference Chairs.....	ix
Program Committee.....	x
External Reviewers	xii
Keynotes.....	xiii

Reconfigurable Logic and Graphics Engines

Real Time Iris Segmentation on FPGA	1
<i>Hau Ngo, Jennifer Shafer, Robert Ives, Ryan Rakvic, and Randy Broussard</i>	
A Reconfigurable Computing Approach for Efficient and Scalable Parallel Graph Exploration	8
<i>Brahim Betkaoui, Yu Wang, David B. Thomas, and Wayne Luk</i>	
High Performance Parallel JPEG2000 Streaming Decoder Using GPGPU-CPU Heterogeneous System	16
<i>Roto Le, Joseph L. Mundy, and R. Iris Bahar</i>	
A Performance Model for Memory Bandwidth Constrained Applications on Graphics Engines	24
<i>Lin Ma and Roger D. Chamberlain</i>	

Special Session on Ongoing EU Projects

EU Collaborative Research on Application-Specific Systems	32
<i>Koen Bertels</i>	

Advances in Arithmetic

(M, p, k)-Friendly Points: A Table-Based Method for Trigonometric Function Evaluation	46
<i>Nicolas Brisebarre, Miloš D. Ercegovic, and Jean-Michel Muller</i>	
On-line Decimal Adder with RBCD Representation	53
<i>Carlos Garcia Vega, Sonia Gonzalez Navarro, Julio Villalba Moreno, and Emilio L. Zapata</i>	
Virtual Floating-Point Units for Low-Power Embedded Processors	61
<i>Syed Zohaib Gilani, Nam Sung Kim, and Michael Schulte</i>	
Simultaneous Floating-Point Sine and Cosine for VLIW Integer Processors	69
<i>Claude-Pierre Jeannerod and Jingyan Jourdan-Lu</i>	

Digital Signal Processing Applications

A High-Rate, Low-Power, ASIC Speech Decoder Using Finite State Transducers	77
<i>Jeffrey R. Johnston and Rob A. Rutenbar</i>	
Partial Expansion Graphs: Exposing Parallelism and Dynamic Scheduling Opportunities for DSP Applications	86
<i>George F. Zaki, William Plishker, Shuvra S. Bhattacharyya, and Frank Fruth</i>	
SIMD/MIMD Dynamically-Reconfigurable Architecture for High-Performance Embedded Vision Systems	94
<i>A. Nieto, D.L. Vilariño, and V.M. Brea</i>	

Cryptology and Security

A Speed Area Optimized Embedded Co-processor for McEliece Cryptosystem	102
<i>Santosh Ghosh, Jeroen Delvaux, Leif Uhsadel, and Ingrid Verbauwhede</i>	
Interface Design for Mapping a Variety of RSA Exponentiation Algorithms on a HW/SW Co-design Platform	109
<i>Leif Uhsadel, Markus Ullrich, Ingrid Verbauwhede, and Bart Preneel</i>	
Instruction Set Extensions for Cryptographic Hash Functions on a Microcontroller Architecture	117
<i>Jeremy H.-F. Constantin, Andreas P. Burg, and Frank K. Gürkaynak</i>	

Application-Specific Acceleration

Design Automation Framework for Application-Specific Logic-in-Memory Blocks	125
<i>Qiuling Zhu, Kaushik Vaidyanathan, Ofer Shacham, Mark Horowitz, Larry Pileggi, and Franz Franchetti</i>	
Viterbi Accelerator for Embedded Processor Datapaths	133
<i>Muhammad Waqar Azhar, Magnus Sjölander, Hasan Ali, Akshay Vijayashekar, Tung Thanh Hoang, Kashan Khurshid Ansari, and Per Larsson-Edefors</i>	
Accelerating NoC-Based MPI Primitives via Communication Architecture Customization	141
<i>Libo Huang, Zhiying Wang, and Nong Xiao</i>	

Posters

A Linear Algebra Core Design for Efficient Level-3 BLAS	149
<i>Ardavan Pedram, Syed Zohaib Gilani, Nam Sung Kim, Robert van de Geijn, Michael Schulte, and Andreas Gerstlauer</i>	
Reconfigurable Cluster-Based Networks-on-Chip for Application-Specific MPSoCs	153
<i>Mehdi Modarressi and Hamid Sarbazi-Azad</i>	
Automated Synthesis of FSM-D-Based Accelerators for Hardware Compilation	157
<i>Nikolaos Kavvadias and Kostas Masselos</i>	
Design Space Exploration for the Implementation of a Predictive Current Controller Based on FPGA	161
<i>Pedro Martín, Osmell Machado, Francisco J. Rodríguez, and Emilio J. Bueno</i>	
Design of Low Power On-chip Processor Arrays	165
<i>Vahid Lari, Shravan Muddasani, Srinivas Boppu, Frank Hannig, and Jürgen Teich</i>	
Novel Application of Genetic Sequencing Algorithms to Optimization of Hardware Resource Sharing for DSP	169
<i>S. McKeown and R. Woods</i>	
Enabling Automatic Pipeline Utilization Improvement in Polyhedral Process Network Implementations	173
<i>Sven van Haastregt and Bart Kienhuis</i>	
Long Residue Checking for Adders	177
<i>Michael B. Sullivan and Earl E. Swartzlander Jr.</i>	
FPGA Based Particle Identification in High Energy Physics Experiments	181
<i>H. Fatih Ugurdag, Ali Basaran, Taylan Akdogan, V. Ugur Güney, and Sezer Gören</i>	
Reconfigurable Design Automation by High-Level Exploration	185
<i>Tim Todman and Wayne Luk</i>	

Author Index189