

Proceedings of the 2012 Conference on Design and Architectures for Signal and Image Processing

(DASIP 2012)

**Karlsruhe, Germany
23 – 25 October 2012**



**IEEE Catalog Number: CFP12DAS-PRT
ISBN: 978-1-4673-2089-4**

Table of Contents

Welcome	8
General Chairs	9
Sponsors	9
Keynote Speakers.....	10
Program Chairs	11
Steering Committee	12
Program Committee.....	12
Session 1: Definition and Implementation of Image and Signal Processing Algorithms	13
<i>A Low Energy Adaptive Motion Estimation Hardware for H.264 Multiview Video Coding</i>	<i>14</i>
Yusuf Aksehir, Kamil Erdayandi, Tevfik Zafer Ozcan and Ilker Hamzaoglu (Sabanci University)	
<i>A High Performance and Low Energy Intra Prediction Hardware for HEVC Video Decoding.....</i>	<i>20</i>
Ercan Kalali, Yusuf Adibelli and Ilker Hamzaoglu (Sabanci University)	
<i>Design of Fixed-point Rounding Operators for the VHDL-2008 Standard.....</i>	<i>28</i>
Nikolaos Kavvadias and Kostas Masselos (University of Peloponnese)	
<i>Investigating Performance Variations of an Optimized GPU-ported Granulometry Algorithm.....</i>	<i>36</i>
Vincent Boulos, Vincent Fristot and Dominique Houzet (GIPSA-Lab), Luc Salvo and Pierre Lhuissier (SIMaP)	
Session 2 (SS): Reconfigurable and Adaptive Architectures for Image and Signal Processing.....	42
<i>Energy-efficient Heterogeneous Reconfigurable Sensor Node for Distributed Structural Health Monitoring.....</i>	<i>43</i>
Andreas Engel, Björn Liebig and Andreas Koch (TU Darmstadt)	
<i>Implementing Large-Kernel 2-D Filters using Impulse Codeveloper.....</i>	<i>51</i>
Carlos Colodro, Javier Toledo, Jose Javier Martinez, Javier Garrigos and Jose Manuel Ferrandez (Universidad Politecnica de Cartagena - UPCT)	
<i>Middleware Based Executive for Embedded Reconfigurable Platforms</i>	<i>59</i>
Amel Khiar, Nicolas Knecht, Laurent Gantel, Soufyane Lkad and Benoit Miramond (ETIS Lab)	
<i>Partitioning and Context Switching for a Reconfigurable FPGA-based DAB Receiver.....</i>	<i>65</i>
Michael Feilen, Andreas Iliopoulos, Matthias Ihmig and Walter Stechele (Technical University of Munich)	
Session 3: Application-specific Processor and Co-processors for Image and Signal Processing ..	73
<i>An Evaluation on Using GPU Coprocessing for Software Radios on a Low-cost Platform.....</i>	<i>74</i>
Lothar Stolz (BMW Research and Technology), Matthias Ihmig and Walter Stechele (Technical University of Munich)	
<i>Application-specific Instruction Processor for Extracting Local Binary Patterns</i>	<i>82</i>
Jani Boutellier, Ismo Lundbom, Janne Janhunen, Jari Ylimäinen and Jari Hannuksela (University of Oulu)	
<i>Consumption Analysis and Estimation in the Design of GStreamer Based Multimedia Applications.....</i>	<i>90</i>
Mickaël Lanoe and Eric Senn (Lab-STICC, University of South-Brittany)	
<i>Flexible Front-End Processing for Software Defined Radio Applications using Application Specific</i>	<i>97</i>
<i>Instruction-set Processors</i>	
Carina Schmidt-Knorreck and Raymond Knopp (Eurecom), Renaud Pacalet (Telecom ParisTech), Andreas Minwegen, Uwe Deidersen, Torsten Kempf and Gerd Ascheid (RWTH Aachen)	

Table of Contents

Session 4: Multi-processor Architectures for Image and Signal Processing	105
<i>Architectural Decomposition of Video Decoders for Many Core Architectures.....</i>	106
Henryk Richter and Volker Kühn (University of Rostock), and Benno Stabernack (Fraunhofer)	
<i>HLS-based Fast Design Space Exploration of ad hoc Hardware Accelerators: a Key Tool for MPSoC Synthesis on FPGA.....</i>	114
Youenn Corre, Hoang Van-Trinh, Jean-Philippe Diguët, Dominique Heller and Loïc Lagadec (Lab-STICC, University of South-Brittany)	
<i>On the Scalability of Image and Signal Processing Parallel Applications on Emerging cc-NUMA Many Cores</i>	122
Ghassan Almaless and Franck Wajsburt (LIP6 - UPMC Sorbonne Universités)	
<i>Programmable Routers for Efficient Mapping of Applications onto NoC-based MPSoCs</i>	130
Manel Djemal (INRIA), Francois Pecheux (UPMC/LIP6), Dumitru Potop Butucaru (INRIA Rocquencourt), Robert De Simone (INRIA Sophia Antipolis), Franck Wajsbürt and Zhen Zhang (LIP6)	
Session 5 (SS): Arithmetic for Image and Signal Processing.....	138
<i>Noise Probability Density Function in Fixed-point Systems Based on Smooth Operators</i>	139
Romuald Rocher and Pascal Scalart (IRISA)	
<i>Analytical Approach to Evaluate the Effect of the Spread of Quantization Noise through the Cascade of Decision Operators for Spherical Decoding.....</i>	147
Aymen Chakhari, Karthick Parashar, Romuald Rocher and Pascal Scalart (INRIA/IRISA)	
<i>Range Estimation of Floating-point Variables in Simulink Models</i>	152
Laurent-Stéphane Didier (LIP6), Alexandre Chapoutot (ENSTA ParisTech), and Fanny Villers (LPMA)	
<i>Sum-of-products Evaluation Schemes with Fixed-point arithmetic, and their Application to IIR Filter Implementation</i>	160
Benoit Lopez, Thibault Hilaire and Laurent-Stéphane Didier (Université Pierre et Marie Curie)	
Session 6 (SS): Architectures for Forward Error Correction Decoders	168
<i>Optimal Low Power and Scalable Memory Architecture for Turbo Encoder.....</i>	169
Venugopal Santhanam and Lokesh Kabra (Synopsys)	
<i>Multi-standard Trellis-based FEC Decoder.....</i>	177
Jean Dion, Marie-Hélène Hamon and Pierre Pénard (Orange Labs), Matthieu Arzel and Michel Jezequel (TELECOM Bretagne)	
<i>Layered Detection and Decoding in MIMO Wireless Systems.....</i>	184
Nicholas Preyss and Andreas Burg (EPFL), Christoph Studer (Rice University)	
<i>High-Throughput LDPC Decoding Using The RHS Algorithm</i>	192
François Leduc-Primeau, Alexandre Raymond, Pascal Giard, Warren Gross (McGill University), Claude Thibeault (Ecole de Technologie Supérieure)	
Session 7: Design Techniques and Methodologies	198
<i>Analysis Techniques for Static Dataflow Models with Access Patterns</i>	199
Kaushik Ravindran, Arkadeb Ghosal, Rhishikesh Limaye, Guoqiang Wang, Guang Yang, and Hugo Andrade (National Instruments Corporation)	
<i>Design Space Exploration Strategies for FPGA Implementation of Signal Processing Systems using CAL Dataflow Program.....</i>	207
Ab Al-Hadi Ab Rahman, Richard Thavot, Simone Casale Brunet, Endri Bezati and Marco Mattavelli (EPFL)	
<i>Design under Constraints of Availability and Energy for Sensor Node in Wireless Sensor Network</i>	215
Van-Trinh Hoang, Nathalie Julien and Pascal Berruet (Lab-STICC)	

Table of Contents

Session 8 (SS): Visual Surveillance.....	223
<i>FPGA Implementation of Camera Tamper Detection in Real-time</i>	224
Tomasz Kryjak, Mateusz Komorkiewicz and Marek Gorgon (AGH University of Science and Technology)	
<i>FPGA Implementation of Real-time Head-shoulder Detection using Local Binary Patterns, SVM and Foreground Object Detection</i>	232
Tomasz Kryjak, Mateusz Komorkiewicz and Marek Gorgoń (AGH University of Science and Technology)	
<i>Impact of High-level Transforms for High-level Synthesis for Motion Detection Algorithm</i>	240
Haixiong Ye and Olivier Florent (ST Microelectronics), Lionel Lacassagne, Daniel Etiemble, Joel Falcou and Andres Romero (University Paris Sud), Laurent Cabaret (Ecole Centrale Paris)	
<i>Video Surveillance Application Based on a Application Specific Vector Processors.....</i>	248
Roman Bartosinski, Martin Danek , Jaroslav Sykora and Lukas Kohout (UTIA AV CR,v.v.i.), and Petr Honzik (CIP plus,s.r.o.)	
Poster Session 1	256
<i>FPGA Implementation of Mono and Stereo Inverse Perspective Mapping for Obstacle Detection</i>	257
Diego Botero, Jonathan Piat, Pierre Chalimbaud, Michel Devy, and Jean Louis Boizard (LAAS-CNRS)	
<i>Performance Evaluation of Total Focusing Method on GPP and GPU</i>	265
Jason Lambert, Antoine Pedron and Ekaterina Iakovleva (CEA LIST), and Guillaume Gens, Franck Bimbard and Lionel Lacassagne (Institut d'Electronique Fondamentale, UMR 8622, Université Paris-Sud 11)	
<i>GPU-based Acceleration of Symbol Timing Recovery</i>	273
Scott Kim, William L. Plishker and Shuvra Bhattacharyya (University of Maryland), and Joseph Cavallaro (Rice University)	
<i>Gradient: an Adaptive Fault-tolerant Routing Algorithm for 2D Mesh Network-on-Chips</i>	281
Istas Pratomo and Sebastien Pillement (University of Rennes 1)	
Poster Session 2	289
<i>A Generic Video Adaptation FPGA Implementation Towards Content - and Context - Awareness in Future Networks.....</i>	290
Willy Aubry, Daniel Negru and Simon Desfarges (LaBRI), Bertrand Le Gal and Dominique Dallet (IMs Lab)	
<i>A Hierarchical Approach to the Out-of-Order Arrival of Frames in Video Streaming Applications on Clustered MPSoC.....</i>	297
Daniela Genius and Khoulood Zine El Abidine (LIP6)	
<i>Black-Box and White-Box Early Power Intent Simulation and Verification: Two Novel Approaches</i>	305
Ons Mbarek, Alain Pegatoquet and Michel Auguin (LEAT, University of Nice Sophia Antipolis)	
<i>Application of Temporal Decoupling to the Creation of Efficient Performance Models of Automotive Architectures.....</i>	313
Takieddine Majdoub, Sebastien Le Nours and Olivier Pasquier (University of Nantes), and Fabienne Nouvel (INSA Rennes)	
<i>A Nature-inspired Adaptive Floating-point Co-processing System</i>	321
Carlo Sau, Danilo Pani, Francesca Palumbo, and Luigi Raffo (University of Cagliari)	

Table of Contents

Poster Session 3	329
<i>Empirical Comparison of Chirp and Multitones on Experimental UWB Software Defined Radar Prototype</i>	330
Julien Le Kernec (University of Nottingham Ningbo), Olivier Romain (ETIS), Patrick Garda and Julien Denoulet (UPMC-LIP6)	
<i>Many-Core Parallelization of Fixed-Point Optimization of VLSI Circuits through GPU Devices</i>	338
Gabriel Caffarena (University of San Pablo CEU) and Daniel Menard (IRISA/INRIA)	
<i>Synthesis of Arithmetic Expressions for the Fixed-point Arithmetic: The Sardana Approach</i>	346
Arnault Ioualalen and Matthieu Martel (Université de Perpignan Via Domitia)	
<i>A Hierarchical Implementation of Hadamard Transform using RVC-CAL Dataflow Programming and Dynamic Partial Reconfiguration</i>	354
Manel Hentati (ENIS/CEA), Yassine Aoudni (ENIS/CEA), Jean François Nezan (INSA/IETR), Mohamed Abid (ENIS/CEA)	
Demo Night	361
<i>The COMPLEX Eclipse Framework for UML/MARTE Specification and Design Space Exploration of Embedded Systems</i>	363
Fernando Herrera, Héctor Posadas, Pablo Peñil, Eugenio Villar (University of Cantabria), Francisco Ferrero, Raúl Valencia (GMV), and Gianluca Palermo (Politecnico di Milano)	
<i>Design of Fixed-point Embedded Systems (DEFIS) French ANR Project</i>	365
Daniel Menard (IRISA/INRIA - University of Rennes I), Laurent Stéphane Didier (LIP6), Eric Goubault (CEA), Revy Guillaume (Univ. Perpignan Via Domitia), Laurent Fangain (InPixa), and Fabrice Lemonnier (Thales)	
<i>An Experimental Toolchain Based on High-level Dataflow Models of Computation for Heterogeneous MPSOC</i>	367
Julien Heulot, Karol Desnos, Jean-Francois Nezan, Maxime Pelcat, Mickael Raulet (INSA, IETR, UMR 6164, UEB), Hervé Yviquel (IRISA, University of Rennes 1) Jean-Christophe Le Lann and Pierre-Laurent Lagalaye (Modaë Technologies)	
<i>Is FPGA a Suitable Platform for Advanced Video Surveillance Systems?</i>	369
Tomasz Kryjak, Mateusz Komorkiewicz and Marek Gorgon (AGH University of Science and Technology)	
<i>FPGA Prototyping of an ASIP LDPC Decoder for the DVB-T2 Standard FPGA</i>	371
Bertrand Le Gal and Christophe Jegu (University of Bordeaux)	
<i>FPGA Based Demonstrator for Blocker Detection in LTE Systems</i>	373
Thomas Schlechter, Christoph Juritsch and Mario Huemer (Klagenfurt University)	
<i>Foreground Detection and Image Segmentation in a Flexible ASVP Platform for FPGAs</i>	375
Roman Bartosinski, Martin Danek, Jaroslav Sykora, Lukas Kohout (UTIA AV CR,v.v.i.), and Petr Honzik (CIP plus s.r.o.)	
<i>GAMPPIX: a New Generation of Gamma Camera</i>	377
Mathieu Thévenin, Frederick Carrel, Mehdi Gmar, Hermine Lemaire and Vincent Schoepff (CEA, LIST)	
<i>GRECO: GREEn Communicating Objects</i>	379
Olivier Berder, Olivier Sentieys, Samuel Mouget, Romain Fontaine (IRISA / University of Rennes 1), Trong Nhan Le, (IRISA / LEAT), Alain Pégatoquet, Cécile Belleudy, Michel Auguin, Gilles Jacquemod, William Tatinian (LEAT / University of Nice Sophia Antipolis), Oswaldo Ramos (LEAT / IM2NP), Florian Broekaert (Thales), Amine Didioui, Carolyn Bernier, Karim Ben Chehida (CEA-LETI), Sylvain Bourdel (IM2NP / University of Aix-Marseille), Hervé Barthélémy (IM2NP / University Sud Toulon - Var), Pascal Ciais and Christopher Barrat (Insight-SIP)	

Table of Contents

<i>HaLOEWEn: A Heterogeneous Reconfigurable Sensor Node for Distributed Structural Health Monitoring</i>	381
Andreas Engel, Björn Liebig and Andreas Koch (TU Darmstadt)	
<i>High-Speed Camera with Embedded FPGA Processing</i>	383
Uros Stevanovic, Michele Caselle, Suren Chilingaryan, Armin Herth, Andreas Kopmann, Matthias Vogelgesang, Matthias Balzer and Marc Weber (KIT, IPE)	
<i>MEMSCOPT: A Source-to-Source Compiler for Dynamic Code Analysis and Loop Transformations</i>	385
Grigoris Dimitroulakos, Christakis Lezos and Konstantinos Masselos (University of Peloponnese)	
<i>Open-People: an Open Platform for Estimation and Optimizations of Energy Consumption</i>	387
Eric Senn (University of South Britany), Daniel Chillet (University of Rennes 1, Inria/Irisa), Olivier Zendra (INRIA Nancy Grand Est), Cecile Belleudy (University of Nice Sophia Antipolis), Rabie Ben Atitallah (University of Valenciennes), Agnes Fritsch (Thales Communications), and Christian Samoyeau (InPixal)	
<i>Parallel Video-Based Traffic Sign Recognition on the Intel SCC Many-core Platform</i>	389
Jan Micha Borrmann, Alexander Viehl (Forschungszentrum Informatik Karlsruhe), Oliver Bringmann and Wolfgang Rosenstiel (Universität Tübingen)	
<i>A Portable Demonstration Device for an Integrated Optical Angle Measurement System</i>	391
Jürgen Oehm, Christian Koch, Ivan Stoychev and Andreas Gornik (Ruhr-Universität Bochum)	
<i>A Prototype of an Invasive Tightly-Coupled Processor Array</i>	393
Shravan Muddasani, Srinivas Boppu, Frank Hannig, Boris Kuzmin, Vahid Lari and Jürgen Teich (University of Erlangen-Nuremberg)	
<i>Prototype of a Radio-on-demand Broadcast Receiver with Real Time Musical Genre Classification</i>	395
Olivier Romain (ETIS), Brunel Happi Tietche and Bruce Denby (UPMC)	
<i>Sparsity-Based Real-Time Audio Restoration</i>	397
Patrick Maechler, David Bellasi, Norbert Felber, Hubert Kaeslin (ETH Zurich), Andreas Burg (EPFL), and Christoph Studer (Rice University)	
<i>Stereo Depth Map Computation on a Tiler TILEPro64 Embedded Multicore Processor</i>	399
Timo Schönwald, Alexander Koch, Benjamin Ranft, Alexander Viehl (FZI), Oliver Bringmann and Wolfgang Rosenstiel (Universität Tübingen)	
<i>Tools for Deploying Dataflow Models on FPGA Targets</i>	401
Kaushik Ravindran, Arkadeb Ghosal, Rhishikesh Limaye, Hugo Andrade, Alejandro Asenjo, Takao Inoue, Douglas Kim, Ankita Prasad, Trung N. Tran, Mike Trimborn, Gerald Wang, and Guang Yang (National Instruments)	
<i>Virtualization of Heterogeneous and Adaptive Multi-Core /Multi-Board Systems</i>	403
Oliver Oey, Stephan Werner, Diana Göhringer, Jürgen Becker (KIT), Andreas Stuckert (Fraunhofer IOSB), and Michael Hübner (Ruhr-University of Bochum)	
<i>XMSIM: A Tool for Early Memory Hierarchy Evaluation</i>	405
Grigoris Dimitroulakos, Theodoros Lioris, Christakis Lezos and Konstantinos Masselos (University of Peloponnese)	