

2012 IEEE/ACM International Conference on Computer-Aided Design

(ICCAD 2012)

**San Jose, California, USA
5 – 8 November 2012**



**IEEE Catalog Number: CFP12CAD-PRT
ISBN: 978-1-4503-1573-9**

TABLE OF CONTENTS

Session 1A Sensing and Harvesting for Energy-Efficient System Design

Moderator(s): Hidetoshi Onodera – Kyoto University

- 1A.1 Online Fault Detection and Tolerance for Photovoltaic Energy Harvesting Systems** 1
*Xue Lin, University of Southern California; Yanzhi Wang, University of Southern California;
Di Zhu, University of Southern California; Naehyuck Chang, Seoul National University;
Massoud Pedram, University of Southern California*
- 1A.2 Tunable Sensors for Process-Aware Voltage Scaling** 7
*Tuck-Boon Chan, University of California at San Diego; Andrew B. Kahng, University of
California at San Diego*
- 1A.3 Collaborative Calibration of On-Chip Thermal Sensors using Performance Counters** 15
*Shiting (Justin) Lu, University of Massachusetts, Amherst; Russell Tessier, University of
Massachusetts, Amherst; Wayne Burlison, University of Massachusetts, Amherst*

Session 1B Test Cost and Security

Moderator(s): Prashant Goteti – Intel Corporation

- 1B.1 Spatial Correlation Modeling for Probe Test Cost Reduction in RF Devices** 23
*Nathan Kupp, Yale University; Ke Huang, University of Texas at Dallas; John M. Carulli Jr.,
Texas Instruments, Inc.; Yiorgos Makris, University of Texas at Dallas*
- 1B.2 Small-Delay-Fault ATPG with Waveform Accuracy** 30
*Matthias Sauer, University Freiburg; Alexander Czutro, University Freiburg; Ilia Polian,
University of Passau; Bernd Becker, University Freiburg*
- 1B.3 Experimental Analysis of a Ring Oscillator Network for
Hardware Trojan Detection in a 90nm ASIC** 37
*Andrew Ferraiuolo, University of Connecticut; Xuehui Zhang, University of Connecticut;
Mohammad Tehranipoor, University of Connecticut*

Session 1C DFM for EUV and Multiple Patterning Lithography

Moderator(s): Duo Ding – Oracle Corporation

- 1C.1 Layout Small-Angle Rotation and Shift for EUV Defect Mitigation** 43
*Hongbo Zhang, Synopsys, Inc.; Yuelin Du, University of Illinois at Urbana-Champaign; Martin
D.F. Wong, University of Illinois at Urbana-Champaign; Yunfei Deng, GLOBALFOUNDRIES;
Pawitter Mangat, GLOBALFOUNDRIES*
- 1C.2 A Methodology for the Early Exploration of Design Rules for
Multiple-Patterning Technologies** 50
*Rani S. Ghaida, University of California, Los Angeles; Tanaya Sahu, University of California, Los
Angeles; Parag Kulkarni, Qualcomm, Inc.; Puneet Gupta, University of California, Los Angeles*

1C.3	A Polynomial Time Triple Patterning Algorithm for Cell based Row-Structure Layout	57
	<i>Haitong Tian, University of Illinois at Urbana-Champaign; Hongbo Zhang, Synopsys, Inc.; Qiang Ma, Synopsys, Inc.; Zigang Xiao, University of Illinois at Urbana-Champaign; Martin D.F. Wong, University of Illinois at Urbana-Champaign</i>	
Session 1D	EMBEDDED TUTORIAL: Algorithms for Analysis and Optimization of Future Cyber Physical Systems	
Session 2A	Hardware and Software Techniques for for Memory Hierarchy Optimization	
	<i>Moderator(s): Sri Parameswaran – University of New South Wales</i>	
2A.1	Improving Last Level Cache Locality by Integrating Loop and Data Transformations	65
	<i>Wei Ding, Pennsylvania State University; Mahmut Kandemir, Pennsylvania State University</i>	
2A.2	Asymmetric DRAM Synthesis for Heterogeneous Chip Multiprocessors in 3D-Stacked Architecture	73
	<i>Minje Jun, Yonsei University; Myoung-Jin Kim, Yonsei University; Eui-Young Chung, Yonsei University</i>	
2A.3	Optimizing Bandwidth and Power of Graphics Memory with Hybrid Memory Technologies and Adaptive Data Migration	81
	<i>Jishen Zhao, Pennsylvania State University; Yuan Xie, Pennsylvania State University, Advanced Micro Devices, Inc.</i>	
2A.4	Probabilistic Design Methodology to Improve Run-Time Stability and Performance of STT-RAM Caches	88
	<i>Xiuyuan Bi, Polytechnic Institute of New York University; Zhenyu Sun, Polytechnic Institute of New York University; Hai Li, Polytechnic Institute of New York University; Wenqing Wu, Qualcomm, Inc.</i>	
Session 2B	Simulation-Based Verification	
	<i>Moderator(s): Bryan Brady – IBM Corporation</i>	
2B.1	Bridging Pre- and Post-Silicon Debugging with BiPeD	95
	<i>Andrew DeOrio, University of Michigan; Jialin Li, University of Michigan; Valeria Bertacco, University of Michigan</i>	
2B.2	Novel Test Detection to Improve Simulation Efficiency – A Commercial Experiment	101
	<i>Wen Chen, University of California, Santa Barbara; Nik Sumikawa, University of California, Santa Barbara; Li-C. Wang, University of California, Santa Barbara; Jayanta Bhadra, Freescale Semiconductor, Inc.; Xiushan Feng, Freescale Semiconductor, Inc.; Magdy S. Abadir, Freescale Semiconductor, Inc.</i>	
2B.3	A Robust General Constrained Random Pattern Generator for Constraints with Variable Ordering	109
	<i>Bo-Han Wu, National Taiwan University; Chung-Yang (Ric) Huang, National Taiwan University</i>	
2B.4	Fast and Scalable Hybrid Functional Verification and Debug with Dynamically Reconfigurable Co-Simulation	115
	<i>Somnath Banerjee, Mentor Graphics Pvt. Ltd., India; Tushar Gupta, Mentor Graphics Pvt. Ltd., India</i>	

Session 2C Advanced Topics in Routing

Moderator(s): *Aiqun Cao – Synopsys, Inc.*
Inki Hong – Cadence Design Systems, Inc.

- 2C.1 TRIAD: A Triple Patterning Lithography Aware Detailed Router** 123
Yen-Hung Lin, National Chiao Tung University; Bei Yu, University of Texas at Austin;
David Z. Pan, University of Texas at Austin; Yih-Lang Li, National Chiao Tung University
- 2C.2 Maze Routing Algorithms with Exact Matching Constraints for Analog and Mixed Signal Designs** 130
Muhammet Mustafa Ozdal, Intel Corporation; Renato Fernandes Hentschke, Intel Corporation
- 2C.3 Reclaiming Over-the-IP-Block Routing Resources with Buffering-Aware Rectilinear Steiner Minimum Tree Construction** 137
Yilin Zhang, University of Texas at Austin; Ashutosh Chakraborty, Oracle Corporation;
Salim Chowdhury, Oracle Corporation; David Z. Pan, University of Texas at Austin
- 2C.4 Construction of Rectilinear Steiner Minimum Trees with Slew Constraints over Obstacles** 144
Tao Huang, The Chinese University of Hong Kong;
Evangeline F.Y. Young, The Chinese University of Hong Kong

Session 2D Computing in the Random Noise: The Bad, the Good, and the Amazing Grace

Moderator(s): *Amit Singhee – IBM T.J. Watson Research Center*

- 2D.1 Noise based Logic: Why Noise?** 152
He Wen, Texas A&M University, Hunan University; Laszlo B. Kish, Texas A&M University
- 2D.2 An Efficient Implementation of Numerical Integration using Logical Computation on Stochastic Bit Streams** 156
Weikang Qian, Shanghai Jiao Tong University; Chen Wang, Shanghai Jiao Tong University;
Peng Li, University of Minnesota; David J. Lilja, University of Minnesota;
Kia Bazargan, University of Minnesota; Marc D. Riedel, University of Minnesota
- 2D.3 Utilizing Random Noise in Cryptography: Where is the Tofu?** 163
Hui Geng, Missouri University of Science and Technology; Jun Wu, Missouri University of
Science and Technology; Jianming Liu, Missouri University of Science and Technology;
Minsu Choi, Missouri University of Science and Technology; Yiyu Shi, Missouri University of
Science and Technology
- 2D.4 Learning from Biological Neurons to Compute with Electronic Noise** 168
Hsin Chen, National Tsing Hua University; Chih-Chen Lu, National Tsing Hua University;
Yi-Da Wu, National Tsing Hua University; Tang-Jung Chiu, Taiwan Semiconductor
Manufacturing Co., Ltd.

Session 3A Timing and Behavioral Modeling

Moderator(s): *Chenjie Gu – Intel Corporation*
Igor Keller – Cadence Design Systems, Inc.

- 3A.1 On the Computation of Criticality in Statistical Timing Analysis** 172
S. Ramprasath, Indian Institute of Technology, Madras;
V. Vasudevan, Indian Institute of Technology, Madras

3A.2	A Dynamic Method for Efficient Random Mismatch Characterization of Standard Cells	180
	<i>Wangyang Zhang, IBM Systems and Technology Group; Amith Singhee, IBM T.J. Watson Research Center; Jinjun Xiong, IBM T.J. Watson Research Center; Peter Habitz, IBM Systems and Technology Group; Amol Joshi, IBM Systems and Technology Group; Chandu Visweswariah, IBM Systems and Technology Group; James Sundquist, IBM Systems and Technology Group</i>	
3A.3	Classifying Circuit Performance using Active-Learning Guided Support Vector Machines	187
	<i>Honghuang Lin, Texas A&M University; Peng Li, Texas A&M University</i>	
Session 3B Formal Approaches to Verification		
Moderator(s): Pankaj Chauhan – Calypto Design Systems, Inc.		
3B.1	Scalable Sampling Methodology for Logic Simulation: Reduced-Ordered Monte Carlo	195
	<i>Chien-Chih Yu, University of Michigan; Armin Alaghi, University of Michigan; John P. Hayes, University of Michigan</i>	
3B.2	Trajectory-Directed Discrete State Space Modeling for Formal Verification of Nonlinear Analog Circuits	202
	<i>Sebastian Steinhorst, TUM CREATE Ltd.; Lars Hedrich, University of Frankfurt</i>	
3B.3	Word Level Feature Discovery to Enhance Quality of Assertion Mining	210
	<i>Lingyi Liu, University of Illinois at Urbana-Champaign; Chen-Hsuan Lin, University of Illinois at Urbana-Champaign; Shobha Vasudevan, University of Illinois at Urbana-Champaign</i>	
Session 3C Leakage and Technology-Aware Gate Sizing		
Moderator(s): Cheng Zhuo – Intel Corporation		
Jianchao Lu – Synopsys, Inc.		
3C.1	Impact of Range and Precision in Technology on Cell-Based Design	218
	<i>John Lee, University of California, Los Angeles; Puneet Gupta, University of California, Los Angeles</i>	
3C.2	An Efficient Algorithm for Library-Based Cell-Type Selection in High-Performance Low-Power Designs	226
	<i>Li Li, Northwestern University; Peng Kang, Northwestern University; Yinghai Lu, Synopsys, Inc.; Hai Zhou, Northwestern University</i>	
3C.3	Sensitivity-Guided Metaheuristics for Accurate Discrete Gate Sizing	233
	<i>Jin Hu, University of Michigan; Andrew B. Kahng, University of California at San Diego; SeokHyeong Kang, University of California at San Diego; Myung-Chul Kim, University of Michigan; Igor L. Markov, University of Michigan</i>	
Session 3D Dealing with Manufacturing and Reliability in Extremely Scaled CMOS and Beyond		
Moderator(s): David Z. Pan – University of Texas at Austin		
Sachin Sapatnekar – University of Minnesota		
3D.1	Dealing with IC Manufacturability in Extreme Scaling	240
	<i>Bei Yu, University of Texas at Austin; Jih-Rong Gao, University of Texas at Austin; Duo Ding, University of Texas at Austin; Yongchan Ban, University of Texas at Austin; Jae-seok Yang, University of Texas at Austin; Kun Yuan, University of Texas at Austin; Minsik Cho, University of Texas at Austin; David Z. Pan, University of Texas at Austin</i>	

3D.2	Circuit Reliability: From Physics to Architectures	243
	<i>Jianxin Fang, University of Minnesota; Saket Gupta, University of Minnesota; Sanjay V. Kumar, University of Minnesota; Sravan K. Marella, University of Minnesota; Vivek Mishra, University of Minnesota; Pingqiang Zhou, University of Minnesota; Sachin S. Sapatnekar, University of Minnesota</i>	
Session 4A	System-Level Modeling and Optimization of Power Ground Networks	
	Moderator(s): Yiyu Shi – Missouri University of Science and Technology Don MacMillen – Nimbic, Inc.	
4A.1	Stability Assurance and Design Optimization of Large Power Delivery Networks with Multiple On-Chip Voltage Regulators	247
	<i>Suming Lai, Texas A&M University; Boyuan Yan, Texas A&M University; Peng Li, Texas A&M University</i>	
4A.2	A Silicon-Validated Methodology for Power Delivery Modeling and Simulation	255
	<i>Cheng Zhuo, Intel Corporation; Gustavo Wilke, Intel Corporation; Ritochit Chakraborty, Intel Corporation; Alaeddin Aydiner, Intel Corporation; Sourav Chakravarty, Intel Corporation; Wei-Kai Shih, Intel Corporation</i>	
4A.3	Optimization of On-Chip Switched-Capacitor DC-DC Converters for High-Performance Applications	263
	<i>Pingqiang Zhou, University of Minnesota; Won Ho Choi, University of Minnesota; Bongjin Kim, University of Minnesota; Chris H. Kim, University of Minnesota; Sachin S. Sapatnekar, University of Minnesota</i>	
Session 4B	Challenges in 3D IC Technologies and Integration	
	Moderator(s): David Z. Pan – University of Texas at Austin	
4B.1	Scaling the “Memory Wall”	271
	<i>Shih-Lien Lu, Intel Corporation; Tanay Karnik, Intel Corporation; Ganapati Srinivasa, Intel Corporation; Kai-Yuan Chao, Intel Corporation; Doug Carmean, Intel Corporation; Jim Held, Intel Corporation</i>	
4B.2	Test Challenges in Designing Complex 3D Chips: What is on the Horizon for the EDA Industry?	273
	<i>Sandeep Kumar Goel, Taiwan Semiconductor Manufacturing Co., Ltd.</i>	
4B.3	3D Integrated Circuits: Designing in a New Dimension	274
	<i>Robert Patti, Tezzaron Semiconductor</i>	
Session 4C	Placement for the Next Decade	
	Moderator(s): Patrick Groeneveld – Synopsys, Inc.	
4C.1	Progress and Challenges in VLSI Placement Research	275
	<i>Igor L. Markov, University of Michigan; Jin Hu, University of Michigan; Myung-Chul Kim, University of Michigan</i>	
4C.2	The Upcoming Golden Age of Placement Research	n/a
	<i>Shankar Krishnamoorthy, Mentor Graphics Corporation</i>	

4C.3	Placement: Hot or Not?	283
	<i>Charles Alpert, IBM Corporation; Zhuo Li, IBM Corporation; Gi-Joon Nam, IBM Corporation; C.N. Sze, IBM Corporation; Natarajan Viswanathan, IBM Corporation; Samuel I. Ward, IBM Corporation</i>	
Session 4D Automation of Biological System Modeling and Analysis		
Moderator(s): Subarna Sinha – Stanford University		
4D.1	Modeling and Design Automation of Biological Circuits and Systems	291
	<i>Natasa Miskov-Zivanov, University of Pittsburgh; James R. Faeder, University of Pittsburgh; Chris J. Myers, University of Utah; Herbert M. Sauro, University of Washington</i>	
Session 5A Power-Aware Architecture and System Design		
Moderator(s): Youngsoo Shin – KAIST		
5A.1	CACTI-IO: CACTI with Off-Chip Power-Area-Timing Models	294
	<i>Norman P. Jouppi, Hewlett-Packard Co.; Andrew B. Kahng, University of California at San Diego; Naveen Muralimanohar, Hewlett-Packard Co.; Vaishnav Srinivas, University of California at San Diego</i>	
5A.2	AFReP: Application-Guided Function-Level Registerfile Power-Gating for Embedded Processors	302
	<i>Hamed Tabkhi, Northeastern University; Gunar Schirner, Northeastern University</i>	
5A.3	Efficient Multiple-Bit Retention Register Assignment for Power Gated Design: Concept and Algorithms	309
	<i>Yu-Guang Chen, National Tsing-Hua University; Yiyu Shi, Missouri University of Science and Technology; Kuan-Yu Lai, National Tsing-Hua University; Geng Hui, Missouri University of Science and Technology; Shih-Chieh Chang, National Tsing-Hua University</i>	
Session 5B Reliability and Thermal Issues in 3-D ICs		
Moderator(s): Miroslav Velez – Aries Design Automation, LLC		
5B.1	A Holistic Analysis of Circuit Timing Variations in 3D-ICs with Thermal and TSV-Induced Stress Considerations	317
	<i>Sravan K. Marella, University of Minnesota; Sanjay V. Kumar, University of Minnesota; Sachin S. Sapatnekar, University of Minnesota</i>	
5B.2	Electromigration-Aware Routing for 3-D ICs with Stress-Aware EM Modeling	325
	<i>Jiwoo Pak, University of Texas at Austin; Sung Kyu Lim, Georgia Institute of Technology; David Z. Pan, University of Texas at Austin</i>	
5B.3	3D Transient Thermal Solver using Non-Conformal Domain Decomposition Approach	333
	<i>Jianyong Xie, Georgia Institute of Technology; Madhavan Swaminathan, Georgia Institute of Technology</i>	

Session 5C CAD Contests

Moderator(s): *Zhuo Li – IBM Research, Austin*

Iris Hui-Ru Jiang – National Chiao Tung University

- 5C.1 Opening: Introduction to CAD Contest at ICCAD 2012** 341
*Iris Hui-Ru Jiang, National Chiao Tung University; Zhuo Li, IBM Corporation;
Yih-Lang Li, National Chiao Tung University*
- 5C.2 ICCAD-2012 CAD Contest in Finding the Minimal Logic Difference for Functional ECO and Benchmark Suite** 342
*WoeiTzy Jong, Cadence Taiwan, Inc.; Hwei-Tseng Wang, Cadence Taiwan, Inc.;
Chengta Hsieh, Cadence Design Systems, Inc.; Kei-Yong Khoo, Cadence Design Systems, Inc.*
- 5C.3 ICCAD-2012 CAD Contest in Design Hierarchy Aware Routability-Driven Placement and Benchmark Suite** 345
Natarajan Viswanathan, IBM Corporation; Charles Alpert, IBM Corporation; Cliff Sze, IBM Corporation; Zhuo Li, IBM Corporation; Yaoguang Wei, IBM Corporation
- 5C.4 ICCAD-2012 CAD Contest in Fuzzy Pattern Matching for Physical Verification and Benchmark Suite** 349
J. Andres Torres, Mentor Graphics Corporation

Session 5D Power Characterization and Optimization in Smartphones

Moderator(s): *Massoud Pedram – University of Southern California*

- 5D.1 System Energy Consumption is a Multi-Player Game** 351
*Mian Dong, Rice University; Tian Lan, George Washington University;
Lin Zhong, Rice University*
- 5D.2 Power Estimation and Modeling Challenges for Mobile Devices** n/a
Mohamed Allam, Qualcomm, Inc.
- 5D.3 Thermal Management on Smart-Phones: A Case Study** n/a
*Ajat Hukkoo, Broadcom Corporation; Hwisung Jung, Broadcom Corporation;
John Redmond, Broadcom Corporation*

Session 6A Computational Approaches for Biological Systems

Moderator(s): *Phillip Brisk – University of California, Riverside*

Saurabh Srivastava – University of California, Berkeley

- 6A.1 Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips** 353
*Sheng-Han Yeh, National Cheng Kung University; Jia-Wen Chang, National Cheng Kung University; Tsung-Wei Huang, National Cheng Kung University;
Tsung-Yi Ho, National Cheng Kung University*
- 6A.2 Compiling Program Control Flows into Biochemical Reactions** 361
*De-An Huang, National Taiwan University; Jie-Hong R. Jiang, National Taiwan University;
Ruei-Yang Huang, National Taiwan University; Chi-Yun Cheng, National Taiwan University*
- 6A.3 Dictionary-Based Error Recovery in Cyberphysical Digital-Microfluidic Biochips** 369
*Yan Luo, Duke University; Krishnendu Chakrabarty, Duke University;
Tsung-Yi Ho, National Cheng Kung University*

6A.4	Reactant Minimization during Sample Preparation on Digital Microfluidic Biochips using Skewed Mixing Trees	377
	<i>Juinn-Dar Huang, National Chiao Tung University; Chia-Hung Liu, National Chiao Tung University; Ting-Wei Chiang, National Chiao Tung University</i>	
Session 6B Fast Parallel Power Ground Network Simulation Methods		
Moderator(s): Wil Schilders – Technische University Eindhoven		
Amitava Bhaduri – Intel Corporation		
6B.1	Fast Transform-Based Preconditioners for Large-Scale Power Grid Analysis on Massively Parallel Architectures	384
	<i>Konstantis Daloukas, University of Thessaly; Nestor Evmorfopoulos, University of Thessaly; George Drasidis, University of Thessaly; Michalis Tsiampas, University of Thessaly; Panagiota Tsompanopoulou, University of Thessaly; George I. Stamoulis, University of Thessaly</i>	
6B.2	Deterministic Random Walk Preconditioning for Power Grid Analysis	392
	<i>Jia Wang, Illinois Institute of Technology</i>	
6B.3	Efficient Parallel Power Grid Analysis via Additive Schwarz Method	399
	<i>Ting Yu, University of Illinois at Urbana-Champaign; Zigang Xiao, University of Illinois at Urbana-Champaign; Martin D.F. Wong, University of Illinois at Urbana-Champaign</i>	
6B.4	Circuit Simulation via Matrix Exponential Method for Stiffness Handling and Parallel Processing	407
	<i>Shih-Hung Weng, University of California at San Diego; Quan Chen, University of Hong Kong; Ngai Wong, University of Hong Kong; Chung-Kuan Cheng, University of California at San Diego</i>	
Session 6C Efficient Verification and Yield Estimation for Analog Circuits		
Moderator(s): Ibrahim Elfadel – Masdar Institute of Science and Technology		
Eric Keiter – Sandia National Laboratories		
6C.1	An Efficient Control Variates Method for Yield Estimation of Analog Circuits based on a Local Model	415
	<i>Pierre-Francois Desrumaux, Cambridge Silicon Radio; Yoan Dupret, Cambridge Silicon Radio; Jens Tingleff, Cambridge Silicon Radio; Sean Minehane, Cambridge Silicon Radio; Mark Redford, Cambridge Silicon Radio; Laurent Latorre, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier; Pascal Nouet, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier</i>	
6C.2	A Fast Time-Domain EM-TCAD Coupled Simulation Framework via Matrix Exponential	422
	<i>Quan Chen, University of Hong Kong; Wim Schoenmaker, Magwel; Shih-Hung Weng, University of California at San Diego; Chung-Kuan Cheng, University of California at San Diego; Guan-Hua Chen, University of Hong Kong; Li-Jun Jiang, University of Hong Kong; Ngai Wong, University of Hong Kong</i>	
6C.3	GPSCP: A General-Purpose Support-Circuit Preconditioning Approach to Large-Scale SPICE-Accurate Nonlinear Circuit Simulations	429
	<i>Xueqian Zhao, Michigan Technological University; Zhuo Feng, Michigan Technological University</i>	
6C.4	Verifying Dynamic Properties of Nonlinear Mixed-Signal Circuits via Efficient SMT-Based Techniques	436
	<i>Leyi Yin, Texas A&M University; Yue Deng, Texas A&M University; Peng Li, Texas A&M University</i>	

Session 6D Toward Co-Design in High-Performance Computing Systems

Moderator(s): X. Sharon Hu – University of Notre Dame

- 6D.1 Toward Codesign in High Performance Computing Systems** 443
Richard F. Barrett, Sandia National Laboratories; Sudip S. Dosanjh, Sandia National Laboratories; Michael A. Heroux, Sandia National Laboratories; X.S. Hu, University of Notre Dame; S. Parker, NVIDIA Corporation; J. Shalf, Lawrence Berkeley National Lab

Session 7A System-Level Modeling and Optimization

Moderator(s): Sri Parameswaran – University of New South Wales

- 7A.1 Accurate On-Chip Router Area Modeling with Kriging Methodology** 450
Florentine Dubois, STMicroelectronics; Valerio Catalano, STMicroelectronics; Marcello Coppola, STMicroelectronics; Frederic Petrot, TIMA Laboratory, CNRS/Grenoble INP/UJF
- 7A.2 Distributed Memory Interface Synthesis for Network-on-Chips with 3D-Stacked DRAMs** 458
Yi-Jung Chen, National Chi Nan University; Chia-Lin Yang, National Taiwan University; Jian-Jia Chen, Karlsruhe Institute of Technology
- 7A.3 Efficient Design Space Exploration for Component-Based System Design** 466
Yinghai Lu, Synopsys, Inc.; Hai Zhou, Northwestern University

Session 7B High-Level Design Methods

Moderator(s): Mohammad A. Al Faruque – University of California, Irvine

- 7B.1 Multiple Tunable Constant Multiplications: Algorithms and Applications** 473
Levent Aksoy, INESC-ID; Eduardo Costa, Catholic University of Pelotas; Paulo Flores, INESC-ID/IST - TU Lisbon; José Monteiro, INESC-ID/IST - TU Lisbon
- 7B.2 The Synthesis of Complex Arithmetic Computation on Stochastic Bit Streams using Sequential Logic** 480
Peng Li, University of Minnesota; David J. Lilja, University of Minnesota; Weikang Qian, University of Michigan-Shanghai Jiao Tong University Joint Institute; Kia Bazargan, University of Minnesota; Marc Riedel, University of Minnesota
- 7B.3 Memory Partitioning and Scheduling Co-Optimization in Behavioral Synthesis** 488
Peng Li, Peking University; Yuxin Wang, Peking University; Peng Zhang, University of California, Los Angeles; Guojie Luo, Peking University; Tao Wang, Peking University; Jason Cong, University of California, Los Angeles

Session 7C The Next Wave: Top Challenges in Electromagnetic-Based Design Automation

Moderator(s): Vikram Jandhyala – University of Washington

- 7C.1 Confronting and Exploiting Operating Environment Uncertainty in Predictive Analysis of Signal Integrity** 496
Andreas C. Cangellaris, University of Illinois at Urbana-Champaign
- 7C.2 Multi-Scale, Multi-Physics Analysis for Device, Chip, Package, and Board Level** 497
Weng C. Chew, University of Illinois at Urbana-Champaign
- 7C.3 Design Strategies for High-Dimensional Electromagnetic Systems** 498
Vikram Jandhyala, University of Washington; Arun V. Sathanur, University of Washington

7C.4	Co-Simulations of Electromagnetic and Thermal Effects in Electronic Circuits using Non-Conformal Numerical Methods	499
	<i>Jin-Fa Lee, Ohio State University; Yang Shao, Ohio State University; Zhen Peng, Ohio State University</i>	
Session 7D EMBEDDED TUTORIAL: Printable Electronics		
Moderator(s): Mehdi Tahoori – Karlsruhe Institute of Technology		
Session 8A Runtime Adaptation for Performance and Reliability		
Moderator(s): Jian-Jia Chen – Karlsruhe Institute of Technology		
Naehyuck Chang – Seoul National University		
8A.1	ISBA: An Independent Set-Based Algorithm for Automated Partial Reconfiguration Module Generation	500
	<i>Ruining He, Tsinghua University; Yuchun Ma, Tsinghua University; Kang Zhao, Tsinghua University; Jinian Bian, Tsinghua University</i>	
8A.2	Fine-Grained Hardware/Software Methodology for Process Migration in MPSoCs	508
	<i>Tuo Li, University of New South Wales; Jude Angelo Ambrose, University of New South Wales; Sri Parameswaran, University of New South Wales</i>	
8A.3	Active Compensation Technique for the Thin-Film Transistor Variations and OLED Aging of Mobile Device Displays	516
	<i>Xiang Chen, University of Pittsburgh; Beiye Liu, University of Pittsburgh; Yiran Chen, University of Pittsburgh; Mengying Zhao, City University of Hong Kong; Chun Jason Xue, City University of Hong Kong; Xiaojun Guo, Shanghai Jiao Tong University</i>	
Session 8B Challenges in Embedded CPU/GPU Core Design		
Moderator(s): Sheng Li – Hewlett-Packard Labs.		
8B.1	Challenges in Validating Next-Generation GPU Compute Capable GPUs	n/a
	<i>Paul Martin, ARM, Inc.</i>	
8B.2	Implementing High-Performance, Low-Power Embedded Processors: Challenges and Solutions	523
	<i>Koen Lampaert, Broadcom Corporation</i>	
8B.3	Latency Tolerance for Throughput Computing	524
	<i>Chien-Ping Lu, MediaTek, Inc.; Brian Ko, MediaTek, Inc.</i>	
Session 8C Emerging Technologies for More-Moore and More-than-Moore Eras		
Moderator(s): Chun Jason Xue – City University of Hong Kong		
8C.1	Multi-Level Cell STT-RAM: Is it Realistic or Just a Dream?	526
	<i>Yaojun Zhang, University of Pittsburgh; Lu Zhang, University of Pittsburgh; Wujie Wen, University of Pittsburgh; Guangyu Sun, Peking University; Yiran Chen, University of Pittsburgh</i>	
8C.2	Ultra-Low Power NEMS FPGA	533
	<i>Sijing Han, Case Western Reserve University; Vijay Sirigiri, Case Western Reserve University; Daniel G. Saab, Case Western Reserve University; Massood Tabib-Azar, University of Utah</i>	

8C.3	Ultra High Density Logic Designs using Transistor-Level Monolithic 3-D Integration	539
	<i>Young-Joon Lee, Georgia Institute of Technology; Patrick Morrow, Intel Corporation; Sung Kyu Lim, Georgia Institute of Technology</i>	
Session 8D The Secret Art of Analog/Mixed-Signal Post-Silicon Validation		
Moderator(s): Eli Chiprout – Intel Corporation		
8D.1	Challenges in Post-Silicon Validation of High-Speed I/O Links	547
	<i>Chenjie Gu, Intel Corporation</i>	
8D.2	Post-Silicon Modeling and Tuning of Analog/Mixed-Signal Circuits via Bayesian Model Fusion	551
	<i>Xin Li, Carnegie Mellon University</i>	
8D.3	Validation Signature Testing: A Methodology for Post-Silicon Validation of Analog/Mixed-Signal Circuits	553
	<i>A. Chatterjee, Georgia Institute of Technology; S. Deyati, Georgia Institute of Technology; B. Muldrey, Georgia Institute of Technology; S. Devarakond, Georgia Institute of Technology; A. Banerjee, Georgia Institute of Technology</i>	
Session 9A Novel Techniques for Network on Chips and Hardware Security		
Moderator(s): John Bainbridge – Sonics, Inc. Grant Martin – Tensilica, Inc.		
9A.1	Functional Post-Silicon Diagnosis and Debug for Networks-on-Chip	557
	<i>Rawan Abdel-Khalek, University of Michigan; Valeria Bertacco, University of Michigan</i>	
9A.2	TRACKER: A Low Overhead Adaptive NoC Router with Load Balancing Selection Strategy	564
	<i>John Jose, Indian Institute of Technology, Madras; K.V. Mahathi, Indian Institute of Technology, Madras; J. Shiva Shankar, Indian Institute of Technology, Madras; Madhu Mutyam, Indian Institute of Technology, Madras</i>	
9A.3	Provably Complete Hardware Trojan Detection using Test Point Insertion	569
	<i>Sheng Wei, University of California, Los Angeles; Kai Li, Rice University; Farinaz Koushanfar, Rice University; Miodrag Potkonjak, University of California, Los Angeles</i>	
9A.4	Using Standardized Quantization for Multi-Party PPUF Matching: Foundations and Applications	577
	<i>Saro Meguerdichian, University of California, Los Angeles; Miodrag Potkonjak, University of California, Los Angeles</i>	
Session 9B Advances in Logic Synthesis		
Moderator(s): Iris Hui-Ru Jiang – National Chiao Tung University		
9B.1	Simultaneous Information Flow Security and Circuit Redundancy in Boolean Gates	585
	<i>Wei Hu, Northwestern Polytechnical University; Jason Oberg, University of California at San Diego; Dejun Mu, Northwestern Polytechnical University; Ryan Kastner, University of California at San Diego</i>	
9B.2	On Logic Synthesis for Timing Speculation	591
	<i>Yuxi Liu, The Chinese University of Hong Kong; Rong Ye, The Chinese University of Hong Kong; Feng Yuan, The Chinese University of Hong Kong; Rakesh Kumar, University of Illinois at Urbana-Champaign; Qiang Xu, The Chinese University of Hong Kong</i>	

9B.3	Lazy Man’s Logic Synthesis	597
	<i>Wenlong Yang, Fudan University; Lingli Wang, Fudan University; Alan Mishchenko, University of California, Berkeley</i>	

9B.4	Minimizing Area and Power of Sequential CMOS Circuits using Threshold Decomposition	605
	<i>Niranjana Kulkarni, Arizona State University; Nishant Nukala, Arizona State University; Sarma Vrudhula, Arizona State University</i>	

Session 9C New Approaches in Physical Synthesis of Nano-Scale Analog Circuits

Moderator(s): Sheldon Tan – University of California, Riverside

9C.1	Performance-Driven Analog Placement Considering Monotonic Current Paths	613
	<i>Po-Hsun Wu, National Cheng Kung University; Mark Po-Hung Lin, National Chung Cheng University; Yang-Ru Chen, National Cheng Kung University; Bing-Shiun Chou, National Cheng Kung University; Tung-Chieh Chen, SpringSoft, Inc.; Tsung-Yi Ho, National Cheng Kung University; Bin-Da Liu, National Cheng Kung University</i>	

9C.2	Configurable Analog Routing Methodology via Technology and Design Constraint Unification	620
	<i>Po-Cheng Pan, National Chiao Tung University; Hung-Ming Chen, National Chiao Tung University; Yi-Kan Cheng, Taiwan Semiconductor Manufacturing Co., Ltd.; Jill Liu, Taiwan Semiconductor Manufacturing Co., Ltd.; Wei-Yi Hu, Taiwan Semiconductor Manufacturing Co., Ltd.</i>	

9C.3	Efficient Parametric Yield Estimation of Analog/Mixed-Signal Circuits via Bayesian Model Fusion	627
	<i>Xin Li, Carnegie Mellon University; Wangyang Zhang, Carnegie Mellon University; Fa Wang, Carnegie Mellon University; Shupeng Sun, Carnegie Mellon University; Chenjie Gu, Intel Corporation</i>	

9C.4	Analytical-Based Approach for Capacitor Placement with Gradient Error Compensation and Device Correlation Enhancement in Analog Integrated Circuits	635
	<i>Cheng-Wu Lin, National Cheng Kung University; Chung-Lin Lee, National Cheng Kung University; Jai-Ming Lin, National Cheng Kung University; Soon-Jyh Chang, National Cheng Kung University</i>	

Session 9D Power Grid Simulation and Verification for Billion-Transistor VLSI Designs

Moderator(s): Claude Moughanni – Lattice Semiconductor Corp.

9D.1	2012 TAU Power Grid Simulation Contest: Benchmark Suite and Results	643
	<i>Zhuo Li, IBM Corporation; Raju Balasubramanian, IBM Corporation; Frank Liu, IBM Corporation; Sani Nassif, IBM Corporation</i>	

9D.2	PGT_SOLVER: An Efficient Solver for Power Grid Transient Analysis	647
	<i>Ting Yu, University of Illinois at Urbana-Champaign; Martin D.F. Wong, University of Illinois at Urbana-Champaign</i>	

9D.3	PowerRush: Efficient Transient Simulation for Power Grid Analysis	653
	<i>Jianlei Yang, Tsinghua University; Zuowei Li, Tsinghua University; Yici Cai, Tsinghua University; Qiang Zhuo, Tsinghua University</i>	

9D.4	Parallel Forward and Back Substitution for Efficient Power Grid Simulation	660
	<i>Xuanxing Xiong, Illinois Institute of Technology; Jia Wang, Illinois Institute of Technology</i>	

9D.5	Design Analysis of IC Power Delivery	664
	<i>Peng Li, Texas A&M University</i>	

9D.6 **Power Grid Effects and Their Impact On-Die** 667
Eli Chiprout, Intel Corporation

9D.7 **Overview of Vectorless/Early Power Grid Verification** 670
Farid N. Najm, University of Toronto

Session 10A Power-Efficient Design and Management of OLED Displays

Moderator(s): Jason Xue – City University of Hong Kong

10A.1 **High-Performance Metal-Oxide TFT and its Application for High-Power Efficiency AMOLED Displays** n/a
Gang Yu, CBRITE, Inc.; Chan-Long Shieh, CBRITE, Inc.

10A.2 **Transistor Technologies and Pixel Circuit Design for Efficient Active-Matrix Organic Light-Emitting Diode Displays** 678
Xiaojun Guo, Shanghai Jiao Tong University; Guangyu Yao, Shanghai Jiao Tong University; Xiaoli Xu, Shanghai Jiao Tong University; Wenjiang Liu, Shanghai Jiao Tong University; Tao Liu, Shanghai Jiao Tong University

10A.3 **Battery Cell Configuration for Organic Light Emitting Diode Display in Modern Smartphones and Tablets-PCs** 679
Donghwa Shin, Seoul National University; Kitae Kim, Seoul National University; Naehyuck Chang, Seoul National University; Massoud Pedram, University of Southern California

10A.4 **Mobile Devices User – The Subscriber and also the Publisher of Real-Time OLED Display Power Management Plan** 687
Yiran Chen, University of Pittsburgh; Xiang Chen, University of Pittsburgh; Mengying Zhao, City University of Hong Kong; Chun Jason Xue, City University of Hong Kong

Session 10B 2-D and 3-D Physical Design Optimization

Moderator(s): Thorlindur Thorolfsson – North Carolina State University

10B.1 **Clock Mesh Synthesis with Gated Local Trees and Activity Driven Register Clustering** 691
Jianchao Lu, Synopsys, Inc.; Xiaomi Mao, Oracle Corporation; Baris Taskin, Drexel University

10B.2 **Fast Approximation for Peak Power Driven Voltage Partitioning in Almost Linear Time** 698
Jia Wang, Michigan Technological University; Xiaodao Chen, Michigan Technological University; Lin Liu, Michigan Technological University; Shiyuan Hu, Michigan Technological University

10B.3 **Multiobjective Optimization of Deadspace, a Critical Resource for 3-D-IC Integration** 705
Johann Knechtel, Dresden University of Technology; Igor L. Markov, University of Michigan; Jens Lienig, Dresden University of Technology; Matthias Thiele, Dresden University of Technology

10B.4 **A Fast Maze-Free Routing Congestion Estimator with Hybrid Unilateral Monotonic Routing** 713
Wen-Hao Liu, National Chiao Tung University; Yih-Lang Li, National Chiao Tung University; Cheng-Kok Koh, Purdue University

Session 10C Enabling Design for Resilience

Moderator(s): Sung Kyu Lim – Georgia Institute of Technology

10C.1	A Thermal and Process Variation Aware MTJ Switching Model and Its Applications in Soft Error Analysis	720
	<i>Peiyuan Wang, University of Pittsburgh; Wei Zhang, Nanyang Technological University; Rajiv Joshi, IBM T.J. Watson Research Center; Rouwaida Kanj, American University of Beirut; Yiran Chen, University of Pittsburgh</i>	
10C.2	Modeling and Synthesis of Quality-Energy Optimal Approximate Adders	728
	<i>Jin Miao, University of Texas at Austin; Ku He, University of Texas at Austin; Andreas Gerstlauer, University of Texas at Austin; Michael Orshansky, University of Texas at Austin</i>	
10C.3	Representative Critical Reliability Paths for Low-Cost and Accurate On-Chip Aging Evaluation	736
	<i>Shuo Wang, University of Connecticut; Jifeng Chen, University of Connecticut; Mohammad Tehranipoor, University of Connecticut</i>	

Session 10D High-Performance, Low-Power Resonant Clocking

Moderator(s): Matthew R. Guthaus – University of California, Santa Cruz

10D.1	High-Performance, Low-Power Resonant Clocking	742
	<i>Matthew R. Guthaus, University of California, Santa Cruz; Baris Taskin, Drexel University</i>	