2012 IEEE International Test Conference

(ITC 2012)

Anaheim, California, USA
5 – 8 November 2012

IEEE Catalog Number: CFP12ITC-PRT
ISBN: 978-1-4673-1594-4

Table of Contents

INTRODUCTORY SECTION

Welcome Message
Steering Committee
Paper Awards
Technical Program Committee
ITC Technical Paper Evaluation and Selection Process
2013 Call-for-Papers
Test Technology Technical Council (TTTC)
Technical Paper Reviewers

ADDRESSES

Keynote

The State of the Future
Krisztián Flautner

Invited

DFT and Testing vs. Inflection Points and Paradigm Shift
Jeff Rearick

Invited

K Computer, the First Supercomputer Which Broke the 10-Petaflops Barrier and Beyond
Kenichi Miura

SESSION 1 MICROPROCESSOR AND SOC TEST

Session Chair: D. Josephson

1.1 *Cell-aware Production Test Results from a 32-nm Notebook Processor*
M. Reese, F. Hapke, J. Rivers, A. Over, V. Ravikumar, W. Redemund, A. Glowatz, J. Schloeffel, J. Rajski

1.2 *The DFT Challenges and Solutions for the ARM Cortex-A15 Microprocessor*
F. Frederick, T. McLaurin, R. Slobodnik

1.3 *A Dynamic Programming Solution for Optimizing Test Delivery in Multicore SOCs*
M. Agrawal, M. Richter K. Chakrabarty

SESSION 2 JITTER AND PHASE NOISE

Session Chair: M. Margala

2.1 *On-Die Instrumentation to Solve Challenges for 28-nm, 28-Gbps Timing Variability and Stressing*
W. Ding, M. Pan, W. Wong, D. Chow, M. Li, S. Shumarayev

2.2 *A Digital Method for Phase Noise Measurement*
A. Ecker, K. Blakkan, M. Soma

2.3 *Higher-Than-Nyquist Test Waveform Synthesis and Digital Phase Noise Injection Using Time-Interleaved Mixed-Mode Data Converters*
X. Wang, N. Tzou, T. Moon, A. Chatterjee, H. Choi

Table of Contents

PH.D. THESIS COMPETITION FORUM: FINAL ROUND
Session Chair: Y. Zorian

PTF 1 *Integrated Optimization of Semiconductor Manufacturing: A Machine Learning Approach*
N. Kupp, Y. Makris

PTF 2 *Low-Power Test Application with Selective Compaction in VLSI Designs*
D. Czysz, J. Tyszer, J. Rajski

SESSION 3 DEBUG AND VALIDATION
Session Chair: P. Varma

3.1 *On Efficient Silicon Debug with Flexible and X-tolerant Trace Interconnection Fabric*
X. Liu, Q. Xu

3.2 *Adaptive Test Selection for Post-Silicon Timing Validation: A Data Mining Approach*
M. Gao, P. Lisherness, K. Cheng

3.3 *In-System Constrained-Random Stimuli Generation for Post-Silicon Validation*
A. Kinsman, H-F. Ko, N. Nicolici

SESSION 4 NEW GENERATION ATE FOR NEW GENERATION CHALLENGES
Session Chair: A. Evans

4.1 *Driver Sharing Challenges for DDR4 High-Volume Testing with ATE*
J. Moreira, M. Moessinger, K. Sasaki, T. Nakamura

4.2 *8-Gbps CMOS Pin Electronics Hardware Macro with Simultaneous Bidirectional Capability*
S. Kojima, Y. Arai, T. Fujibe, T. Ataka, A. Ono, K. Sawada, D. Watanabe

4.3 *Multi-GHz Arbitrary Timing Generator with Data Pattern Serializing and Formatting*
D. Keezer, T. Chen, C. Gray, H. Choi, S. Kim, S. Lee

SESSION 5 UNDERSTANDING STATISTICS OF DEFECTS AND VARIATION
Session Chair: K. Butler

5.1 *Spatial Estimation of Wafer Measurement Parameters Using Gaussian Process Models*
N. Kupp, K. Huang, J. Carulli, Y. Makris

5.2 *Systematic Defect Screening in Controlled Experiments Using Volume Diagnosis*
B. Seshadri, P. Gupta, Y-T. Lin, B. Cory

5.3 *Screening Customer Returns with Multivariate Test Analysis*
N. Sumikawa, L. Wang, L. Winemberg

Table of Contents

SESSION 6 ADVANCES IN ATPG

Session Chair: J. Li

6.1 *On Pinpoint Capture Power Management in At-Speed Scan Test GenerationÌÌÈFHÏ*
X. Wen, K. Miyase, S. Kajihara, Y. Nishida, P. Girard, M. Tehranipoor, L-T. Wang

6.2 *A Fast and Accurate Per-Cell Dynamic IR-Drop Estimation Method for At-Speed Scan Test Pattern ValidationÌÌÈI Ï*
Y. Yamato, T. Yoneda, K. Hatayama, M. Inoue

6.3 *Functional Test of Small-Delay Faults Using SAT and Craig InterpolationÌÌÈÍ Í*
M. Sauer, S. Kupferschmid, A. Czutro, I. Polian, S. Reddy, B. Becker

SESSION 7 BETTER YIELD AT LESS COST

Session Chair: W. Fritzsche

7.1 *An ATE Architecture for Implementing Very-High-Efficiency Concurrent TestingÌÌÈÎ H*
T. Nakajima, T. Yaguchi, H. Sugimura

7.2 *Low-Cost and Robust Wideband Periodic Signal Reconstruction by Incoherent Undersampling Using Total Variation As Cost FunctionÌÌÈÏ H*
N. Tzou, D. Bhatta, S. Hsiao, H. Choi, A. Chatterjee

7.3 *Power Integrity Control of ATE for Emulating Power Supply Fluctuations on Customer EnvironmentÌÌÈÌ H*
M. Ishida, T. Nakura, T. Kikkawa, T. Kusaka, S. Komatsu, K. Asada

SESSION 8 ADVANCES IN VERIFICATION AND VALIDATION

Session Chair: D. Belete

8.1 *Event-driven Framework for Configurable Runtime System Observability for SOC DesignsÌÌÈJH*
J. Lee, F. Kouteib, R. Lysecky

8.2 *Modeling, Verification and Pattern Generation for Reconfigurable Scan NetworksÌÌG€H*
R. Baranowski, M. Kochte, H-J. Wunderlich

8.3 *Design Validation of RTL Circuits Using Evolutionary Swarm IntelligenceÌÌGFG*
M. Li, K. Gent, M. Hsiao

SESSION 9 SCAN COMPRESSION

Session Chair: A. Cron

9.1 *Improving Test Compression by Retaining Non-Pivot Free Variables in Sequential Linear DecompressorsÌÌGG€*
S. Muthyala, N. Touba

9.2 *Hybrid Selector for High-X Scan CompressionÌÌGGÏ*
P. Wohl, J. Waicukauski, F. Neuveux, J. Colburn

9.3 *Low-Power Programmable PRPG with Enhanced Fault Coverage GradientÌÌGHÏ*
J. Tyszer, J. Solecki, N. Mukherjee, G. Mrugalski, J. Rajski

Table of Contents

SESSION 10 RF/ANALOG TEST OPTIMIZATION AND CALIBRATION

Session Chair: S. Tilden

10.1 *Making Predictive Analog/RF Alternate Test Strategy Independent of Training Set Size*
H. Ayari, F. Azais, S. Bernard, M. Comte, V. Kerzerho, O. Potin, M. Renovell

10.2 *Algorithm for Dramatically Improved Efficiency in ADC Linearity Test*
D. Chen, Z. Yu

10.3 *Calibration of a Flexible High- Precision Power-On Reset During Production Test*
G. Hilber, D. Gruber, M. Sams, T. Ostermann

SESSION 11 FINDING/DIAGNOSING NEW AND HARD-TO-DETECT DEFECTS

Session Chair: S. Jayaraman

11.1 *Root-Cause Identification of an Hard-to-Find On-Chip Power Supply Coupling Fail*
F. Stellari, T. Cowell, P. Song, Z. Toprak Deniz, J. Bulzacchelli, N. Mitra

11.2 *Improved Volume Diagnosis Throughput Using Dynamic Design Partitioning*
X. Fan, H. Tang, Y. Huang, W. Cheng, S. Reddy, B. Benware

11.3 *On Modeling Faults in FinFET Logic Circuits*
Y. Liu, Q. Xu

SESSION 12 3D/TSV

Session Chair: B. Cory

12.1 *A Unified Method for Parametric Fault Characterization of Post-Bond TSVs*
S-Y. Huang, Y-H. Lin, K-H. Tsai, W-T. Cheng, S. Sunter

12.2 *Impact of Radial Defect Clustering on 3-D Stacked IC Yield from Wafer to Wafer Stacking*
E. Singh

12.3 *Scan Test of Die Logic in 3-D ICs Using TSV*
B. Noia, Duke University; S. Panth, K. Chakrabarty, S. Lim

12.4 *DFT Architecture and ATPG for Interconnect Test of JEDEC Wide-IO Memory-on-Logic Die Stacks*
S. Deutsch, Duke University; B. Keller, V. Chickermane, S. Mukherjee, N. Sood, S. Goel, J. Chen, A. Mehta, F. Lee, E. Marinissen

SESSION 13 BOARD AND SYSTEM-LEVEL TEST

Session Chair: W. Eklow

13.1 *Capacitive Sensing Testability in Complex Memory Devices*
K. Parker

13.2 *FPGA-based Synthetic Instrumentation for Board Test*
A. Jutman, I . Aleksejev, S. Devadze, S. Odintsov, T. Wenzel

13.3 *Board-assisted BIST: Long- and Short-Term Solutions for Testpoint Erosion—Reaching into the DFx Toolbox*
Z. Conroy, J. Grealish, H. Miles, A. Crouch, A. Suto, S. Myers

13.4 *Packet-based JTAG for Remote Testing*
M. Portolan

Table of Contents

SESSION 14 TEST STRATEGIES FOR DIFFERENT MEMORY TYPES

Session Chair: S. Hamdioui

14.1 *A Memory Yield Improvement Scheme Combining Built-in Self-Repair and Error Correction Codes*ÌÌÌÎ Í
P. Chen, ITRI; T. Wu, M. Lee, B. Lin, C. Wu, C. Tien, H. Lin, H. Chen, C. Peng, M. Wang

14.2 *Testing Strategies for a 9T Sub-threshold SRAM*ÌÌÌÏ I
H. Yang, C. Lin, H. Chen, M. Chao, M. Tu, S. Jou, C. Chuang

14.3 *Low-Power SRAMs Power Mode Control Logic: Failure Analysis and Test Solutions*ÌÌÌÌ I
L. Zordan, A. Bosio, L. Dilillo, P. Girard, A. Todri, A. Virazel, N. Badereddine

14.4 *A Built-in Self-Test Scheme for 3-D RAMs*ÌÌÌUI
Y-C. Yu, J-F. Li, C-W. Chou, C-Y. Lo, D-M. Kwai, Y-F. Chou, C-W. Wu

SESSION 15 AGING DIAGNOSTICS AND REDUNDANCY APPLICATIONS

Session Chair: I. Harris

15.1 *On-Chip Diagnosis for Early-Life and Wear-Out Failures*ÌÌÌ €H
M. Beckler, R. Blanton

15.2 *DART: Dependable VLSI Test Architecture and Its Implementation*ÌÌÌ FH
Y. Sato, S. Kajihara, T. Yoneda, K. Hatayama, M. Inoue, Y. Miura, S. Ohtake, T. Hasegawa, M. Sato, K. Shimamura, H. Yang, C. Lin, H. Chen, M. Chao, M. Tu, S. Jou, C. Chuang

15.3 *A Design Flow to Maximize Yield/Area of Physical Devices Via Redundancy*ÌÌÌ GH
M. Mirza-Aghatabar, M. Breuer, S. Gupta

15.4 *BS 1149.1 Extensions for an Online Interconnect Fault Detection and Recovery*ÌÌÌ HH
S. Sadeghi-Kohan, M. Namaki-Shoushtari, F. Javaheri, Z. Navabi

SESSION 16 COVERAGE ANALYSIS AND TEST OPTIMIZATION

Session Chair: J. Potter

16.1 *FALCON: Rapid Statistical Fault Coverage Estimation for Complex Designs*ÌÌÌ I G
S. Mirkhani, J. Abraham, T. Vo, H. Jun, W. Eklow

16.2 *Methodology for Fault Grading High-Speed I/O Interfaces Used in Complex Graphics Processing Unit*ÌÌÌ Í G
A. Khare, P . Kishore, S. Reddy, A. Sanghani, K. Rajan

16.3 *Functional Test Content Optimization for Peak-Power Validation—An Experimental Study*ÌÌÌ Î €
V. Kamath, W. Chen, N. Sumikawa, L-C. Wang

Table of Contents

SESSION 17 RF BIST LOOKS WITHOUT TOUCHING
Session Chair: F. Taenzler

17.1 *Experiences With Nonintrusive Sensors for RF Built-in Testÿÿÿ Ï €*
L. Abdallah, H. Stratigopolulos, S. Mir C. Kelma

17.2 *A Frequency Measurement BIST Implementation Targeting Gigahertz Applicationÿÿÿ Ï Ì*
M. Dubois, E. De Foucauld, C. Mounet, S. Dia, C. Mayor

17.3 *DC Temperature Measurements for Power Gain Monitoring in RF Power Amplifiersÿÿÿ Ì Î*
J. Altet, D. Mateo, D. Gómez, X. Perpinyà, M. Vallvehi, X. Jordà

SESSION 18 ELEVATING SOFTWARE TO A HIGHER LEVEL
Session Chair: C. Gavin

18.1 *Automated System-level Functional Test Program Generation on ATEÿÿÿ JI*
M. Ueda, S. Ishikawa, M. Goishi, S. Kitagawa, H. Araki, S. Inage

18.2 *Low-Cost High-Speed Test Data Acquisition: Accurate Period-Estimation- driven Signal Reconstruction Using Incoherent Subsamplingÿÿÿ €F*
T. Moon, H. Choi, A. Chatterjee

18.3 *RNA: Advanced Phase Tracking Method for Digital Waveform Reconstructionÿÿÿ F€*
H. Okawara, T. Ito, J. Liu

SESSION 19 RELIABILITY
Session Chair: A. Crouch

19.1 *Radic: A Standard-Cell-based Sensor for On-Chip Aging and Flip-Flop Metastability Measurementsÿÿÿ FJ*
X. Wang, D. Tran, S. George, L. Winemberg, N. Ahmed, S. Palosh, A . Dobin, M. Tehranipoor

19.2 *Vulnerability-based Interleaving for Multi-Bit Upset Protection in Modern Microprocessorsÿÿÿ GÌ*
M. Maniatakos, Y. Makris, M. Michail

19.3 *An Experiment of Burn-in Time Reduction Based on Parametric Test Analysisÿÿÿ HÎ*
N. Sumikawa, L. Wang, M. Abadir

LECTURE 1 ANALOG DFT*
Session Chair: J. Carulli

L 1.1 *Analog Verification and Test from Circuit Designer's Perspective*
J. Kim

L 1.2 *Analog DFT from a Test Perspective*
R. Geiger

L 1.3 *Analog DFT from an Industrial Perspective*
E. Silva

*Presented at ITC, but not included in proceedings.

Table of Contents

LECTURE 2 ELEVATOR TALKS*
Session Chair: S. Mitra

V. Agrawal, R. Daasch, J. Dworak, M. Fujita, S. Hamidioui,
M. Hashimoto, Y. Hu, C-M. Li, G. Roberts, O. Sinanoglu, D. Walker

LECTURE 3 ADVANCES IN SECURITY, TEST AND VALIDATION*
Session Chair: Y. Makris

L 3.1 *Hardware-based Security: The Most Challenging Testing Task*
M. Potkonjak

L 3.2 *Memory Scan Write-Thru (MSWT): A Method for Efficient Testing of Memory Interface Logic*
B. Nadeau-Dostie, D.Buck, J-F. Côté

L 3.3 *Best-Known Methods in Post-Silicon Validation Platform Thermal Management and Margining*
R. Mohammed, A. Kabadi

ADVANCED INDUSTRIAL PRACTICES

AIP 1 BUILDING RELIABLE SYSTEMS*
Session Chair: J. Dworak

A 1.1 *Challenges in Power-constrained System Resilience*
P. Bose, C. Cher, M. Gupta, P. Kudva, J. Rivers

A 1.2 *Aging Effects and Workload Dependencies in Embedded Processors*
V. Chandra

A 1.3 *Resilient Circuit Design for Mitigation of Droop, Temperature and Aging Effects*
J. Tschanz

AIP 2 YIELD EXPERIENCES FROM THE FRONT LINES*
Session Chair: B. Benware

A 2.1 *The Changing Face of Defects—New and Nefarious?*
S. Venkataraman

A 2.2 *New Test-based Yield Learning Methodologies Providing ROI*
T. Herrmann, S. Malik

A 2.3 *Practical Considerations When Using Scan Data for Yield Enhancement*
S. Palosh, D. Carder

AIP 3 POST-SILICON VALIDATION*
Session Chair: Q. Xu

A 3.1 Silicon Validation: Today and Tomorrow
E. Rentschler

A 3.2 K Computer: A Highly Reliable 10-Petaflops Supercomputer
T. Yoshikawa, T. Nakada, K. Takayama, D. Maruyama, M. Yanagida, S. Kameyama

A 3.3 Post-Silicon Electrical Validation Challenges and Methodologies
N. Hakim

*Presented at ITC, but not included in proceedings.

Table of Contents

AIP 4 JITTER/HIGH-SPEED IO TESTING*
Session Chair: D. Hong

A 4.1 *The Whole Shebang: Jitter Implementations Speak Louder Than Jitter Words*
T. Schumacher

A 4.2 *Capture 25-Gbps Serdes Eye Diagram in ATE Production Environment*
M. Lin

A 4.3 *Millimeter-Wave Testing: The Struggle Between Feasibility and Manufacturing Dream*
M. Slamani, H.Ding, A. Valdes-Garcia, Y. Ding, J. Ferrario

PANEL 1 TEST/ATE VISION 2020—ENTREPRENEURSHIP IN TEST CEO PANEL
Moderator: E. Volkerink, Organizer: K. Lanier

Panelists: B. Bottoms, G. Erickson, D. Glotter, B. Madsen, M. Roos

P 1 *Test/ATE Vision 2020—Entrepreneurship in Test CEO Panel*[illegible] I Î
K. Lanier

PANEL 2 ARE INDUSTRIAL TEST PROBLEMS REAL PROBLEMS? I THOUGHT RESEARCH HAS SOLVED THEM ALL!
Moderator: X. Gu, Organizers: X. GU and K. Lanier

Panelists: R. Aitken, K. Butler, K. Chakrabarty, M. Fujita, N. Kanekawa, E. Marinissen

P 2 *Are Industrial Test Problems Real Problems? I Thought Research Has Solved Them All!*[illegible] I Ï
X. Gu

Panel 2 Posters*

Board- and System-level NTF Challenges on Test and Diagnosis
Z. Zhang, Y. Sun, Z. Wang

Introducing Logic Programmability for Pre- and Post-Silicon Verification and Debugging
T. Hoshino

Test Challenges and Collaboration Opportunities at Huawei Hisilicon
C. Liu

In-Field Testing Techniques for NAND Flash Memories
H. Yu, K. Huang, L. Zhang, X. Gu

WhiteDiag: A White-Box Diagnostic Framework for Board-level Faults
Z. Sun, L. Jiang, Q. Xu, Z, Wang, X. Gu

Trace and Debug Techniques for Many-Core Platforms
C-T. Huang

Patchable Hardware for FPGA-based Systems
M. Fujita

Circuit and System Mechanism for High Field Reliability
S. Kajihara

How to Promote Industry/Academia Research Collaboration
K. Chakrabarty

Low-Cost High-Quality Signal Generation for ADC Testing
H. Kobayashi

*Presented at ITC, but not included in proceedings.

Table of Contents

PANEL 3 MANAGING PROCESS VARIANCE IN ANALOG DESIGNS
Moderator: D. Floyd, Organizer: E. Atwood

Panelists: A. Frisch, D. O'Riordan, G. Roberts, S. Sunter, M. Tirupattur

P 3 *Managing Process Variance in Analog Designs𝄜 I Ì*
E. Atwood

PANEL 4 HOW ARE FAILURE MODES, DEFECT TYPES AND TEST METHODS CHANGING FOR 32 NM/28 NM AND BEYOND?
Moderator and Organizer: P. Nigh

Panelists: D.Appello, S.K. Goel, M. Laisne, R. Madge, S. Venkataraman

P 4 *How Are Failure Modes, Defect Types and Test Methods Changing for 32 nm/28 nm and Beyond?𝄜 I J*
P. Nigh

PANEL 5 TESTING HIGH-FREQUENCY AND LOW-POWER DESIGNS: DO THE STANDARD RULES AND TOOLS APPLY
Moderator and Organizer: S. Davidson

Panelists: S. Chakravarty, J. Doege, B. Keller, H. Konuk, R. Press

P 5 *Testing High-Frequency and Low-Power Designs: Do the Standard Rules and Tools Apply?𝄜 Í €*
S. Davidson

PANEL 6 ARE THE CHIPS GUYS HELPING OR HINDERING BOARD TEST?
Moderator and Organizer: Z. Conroy

Panelists: B. Bottoms, G. Erickson, D. Glotter, B. Madsen, M. Roos

P 6 *Are the IC Guys Helping or Hindering Board Test?𝄜 Í F*
Z. Conroy

PH.D THESIS COMPETITION FORUM: FINAL ROUND
Y. Zorian, Synopsys (Chair)

PTF1 Integrated Optimization of Semiconductor Manufacturing: A Machine Learning Approach"")) &
N. Kupp, Y. Makris

PTF2 Low-Power Test Application with Selective Compaction in VLSI Designs"") * &
D. Czysz, J. Tyszer, J. Rajski

Table of Contents

POSTER SESSION*

Session Chair: W. Eklow

PO 1 *Electrical Interconnect Testing of Open Defects in Assembled PCBs Utilizing IEEE 1149.1 Test Mechanism*
M. Hashizume, T. Konishi, H. Yotsuyanagi

PO 2 *Testing Resistive Connections on Boards and 3-D Stacked ICs*
K. Parker

PO 3 *Low-Distortion Sinusoidal Signal Generation Using Novel Harmonic Cancellation Techniques*
B. K. Vasan, S. Sudani, R.Geiger, D. Chen

PO 4 *GPU-Based Massively Parallel N-Detect Transition Delay Fault ATPG*
K. Liao, S. Hsu, J. Li

PO 5 *Transient IR-Drop Analysis for At-Speed Testing Using Representative Random Walk*
M. Tsai, W. Ding, P. Chen, J. Li

PO 6 *Dynamic Partitioning-based Scan-Chain Diagnosis to Improve Volume Diagnosis Throughput*
Y. Huang, H. Tang, M. Sharma, W. Cheng, B. Benware X. Fan, S. Reddy

PO 7 *Nearest Neighborhood Exclusion (NNE) Applications for Test Productivity and Quality Improvement*
G. Ponnuvel, K. Duffus, L. Nassar, P. Cannon

PO 8 *The Ohmic Contact RF MEMS Switch with Thru-Glass-Via for High-Frequency Up to 30 GHz*
T. Masuda, Y. Horimoto, D. Morihara, T. Seki, F. Sato, M. Oba

PO 9 *Post-Silicon Characterization Methodology for the Qualcomm Hexagon DSP Using Random Test Generation*
R. McAuliffe, P. McWithey

PO 10 *A New Methodology for Post-Silicon Speed-Path Analysis Using Logic Structural Content*
C. Tsai, K. Wee, R. Sharma, S. Shah

PO 11 *On RT-level DFT Insertion for Reducing Power Level*
M. Namaki-Shoushtari, Z. Navabi

PO 12 *Practical Approaches to ASIC Embedded Macro Test in an IEEE 1687 Environment*
K. Chakravadhanula, V. Chickermane, R. Khurana, C.P. Garg, C. Zoellin, B. Cowan

PO 13 *Reducing ATE Time for Power-constrained Scan Test by Asynchronous Clocking*
P. Venkataramani, V. Agrawal

PO 14 *Novel Approach to Detect and Diagnose Load Board Problems Early in the Production Flow*
M. Maroon, G. Cozacov

PO 15 *Standalone Multicell Probe Card for At-Speed Functional Testing*
M. Chung, H. Lai, M. Liu

PO 16 *Use XML to Enhance Embedded Test and a Case Study*
W. Wang

PO 17 *New Test Instrument Solves DDR Controller Test Challenges*
A. Sivaram

PO 18 *Multimode ATPG for DVFS Designs*
B. Bai, J. Li, J. Rau

*Presented at ITC, but not included in proceedings

Table of Contents

POSTER SESSION*

PO 19 *A Low-Cost Spectral Testing Method for Analog-to-Digital Converters with Amplitude Clipping and Noncoherent Sampling*
S. Sudani, L. Xu, D. Chen

PO 20 *Does Increased Compression Decrease Diagnosis Resolution?*
D. Carder

PO 21 *Automatic Design Error Diagnosis and Correction of Complex Processors Using Formal Methods*
A. Gharehbaghi, M. Fujita

PO 22 *Flow Optimization for ATPG/Diagnosis of AMD High- Performance APU*
R. Shukla, A. Margulis, A. Normatov

PO 23 *Experiments and Analysis Towards Understanding Logic State Retention in 28-nm Process Node*
S. Dasnurkar, N. Kulkarni, L. Ranganathan, R. Thirumala, A. Datta, M. Abu-Rahma,P. Seeram, P. Bhadri

PO 24 *Fault Coverage Analysis on Analog/Mixed-Signal Circuits Based on Statistical Dissimilarity*
K. Kim, J. Kim

PO 25 *On Pre-Bond Probing of TSVs in 3-D Stacked ICs Using Adhesive Silicon Interposer*
L. Jiang, Q. Xu

PO 26 *Scalable DFT Architecture for Multicore Design*
T. Vo, R. Vishwanath, Y. Lee

PO 27 *Resolutation Improvement Using TestLab Diagnosis*
R. Blanton

PO 28 *An Efficient Test Data Compression Scheme Using Selection Expansion*
J. Rau, P. Wu, K. Chen

PO 29 *Parallel Parametric Test in Semiconductor Production*
Y. Miyake, L. Levy

PO 30 *ADAGE: An Automated Synthesis Tool for Adaptive BCH-based ECC IP-Cores*
S. Di Carlo, M. Fabiano, M.Indaco, P. Prinetto

PO 31 *Accelerate Test Hole Reduction Through a Novel SOC Functional Test Architecture*
L. Rao, R. Jayabharathi

PO 32 *Timing Error Minimization Methods to DLT2Dr Scheme for Channel Bandwidth Enhancement of Low-Speed ATE*
G. Kim, W. Nah S. Kang

PO 33 *Using Scan Chain Diagnosis to Characterize DFM Rule Performance*
S. Palosh, A. Kochhar

PO 34 *Emerging Test Standards*
IEEE Standards Working Group Representative

ITC 2011 Best Paper

Real-Time Testing Method for 16-Gbps 4-PAM Signal InterfaceÈĚ Ï G
M. Ishida, K. Ichiyama, D. Watanabe, M. Kawabata, T. Okayasu

*Presented at ITC, but not included in proceedings