

2012 International Conference on Embedded Computer Systems

(SAMOS 2012)

**Samos, Greece
16-19 July 2012**



**IEEE Catalog Number: CFP1252A-PRT
ISBN: 978-1-4673-2295-9**

Table of Contents

Keynotes	i
<hr/>	
The Homogeneity of Architecture in a Heterogeneous world	i
<i>John Goodacre</i>	
It's About Time	ii
<i>Edward A. Lee</i>	
Maximum Performance Computing for Exascale Applications	iii
<i>Oskar Mencer</i>	
Design Space Exploration	1
<hr/>	
Just-in-Time Verification in ADL-based Processor Design	1
<i>Dominik Auras, Andreas Minwegen, Uwe Deidersen, Stefan Scürmans, Gerd Ascheid, and Rainer Leupers</i>	
Interleaving Methods for Hybrid System-level MPSoC Design Space Exploration	7
<i>Roberta Piscitelli and Andy D. Pimentel</i>	
A Template-based Methodology for Efficient Microprocessor and FPGA Accelerator Co-Design	15
<i>Angeliki Kritikakou, Francky Catthoor, George S. Athanasiou, Vasilios Kelefouras, and Costas Goutis</i>	
Using OpenMP Superscalar for Parallelization of Embedded and Consumer Applications	23
<i>Michael Andersch, Chi Ching Chi, and Ben Juurlink</i>	
Embedded Simulation	33
<hr/>	
Virtual Prototyping for Efficient Multi-Core ECU Development of Driver Assistance Systems	33
<i>Rainer Kiesel, Martin Streubühr, Christian Haubelt, Anestis Terzis, and Jürgen Teich</i>	
System Modeling and Multicore Simulation Using Transactions	41
<i>Amine Anane, El Mostapha Aboulhamid, and Yvon Savaria</i>	
HNOCS: Modular Open-Source Simulator for Heterogeneous NoCs	51
<i>Yaniv Ben-Itzhak, Eitan Zahavi, Israel Cidon, and Avinoam Kolodny</i>	
BADCO : Behavioral Application-Dependent Superscalar Core Model	58
<i>Ricardo A. Velásquez, Pierre Michaud, and André Seznec</i>	

Memory and Comms. Strategies	68
<hr/>	
An Application-Specific Network-on-Chip for Control Architectures in RF Transceivers	68
<i>Siegfried Brandstätter and Mario Huemer</i>	
A Framework for Efficient Cache Resizing	76
<i>Georgios Keramidas, Chrysovalantis Datsios, and Stefanos Kaziras</i>	
OSR-Lite: Fast and Deadlock-Free NoC Reconfiguration Framework	86
<i>Alessandro Strano, Davide Bertozzi, Francisco Triviño, José L. Sánchez, Francisco J. Alfaro, and José Flich</i>	
A Tightly-Coupled Multi-Core Cluster with Shared-Memory HW Accelerators	96
<i>Masoud Dehyadegari, Andrea Marongiu, Mohammad Reza Kakoe, Luca Benini, Siamak Mohammadi, and Naser Yazdani</i>	
Domain-Specific Architectures	104
<hr/>	
Architecture-Level Fault-Tolerance for Biomedical Implants	104
<i>Robert M. Seepers, Christos Strydis, and Georgi N. Gaydadjiev</i>	
Reconfigurable Miniature Sensor Nodes for Condition Monitoring	113
<i>Teemu Nyländén, Jani Boutellier, Karri Nikunen, Jari Hannuksela, and Olli Silvén</i>	
Counting Stream Registers: An Efficient and Effective Snoop Filter Architecture	120
<i>Aanjhan Ranganathan, Ali Galip Bayrak, Theo Kluter, Philip Brisk, Edoardo Charbon, and Paolo lenne</i>	
Dataflow Application Synthesis	128
<hr/>	
Design Space Exploration in Application-Specific Hardware Synthesis for Multiple Communicating Nested Loops	128
<i>Rosilde Corvino, Abdoulaye Gamatié, Marc Geilen, and Lech Józwiak</i>	
Automatic FPGA Synthesis of Memory Intensive C-based Kernels	136
<i>Matthew Milford and John McAllister</i>	
Throughput Driven Transformations of Synchronous Data Flows for Mapping to Heterogeneous MPSoCs	144
<i>Anastasia Stulova, Rainer Leupers, and Gerd Ascheid</i>	
Dataflow Analysis	152
<hr/>	
K-Periodic Schedules for Evaluating the Maximum Throughput of a Synchronous Dataflow Graph	152
<i>Bruno Bodin, Alix Munier-Kordon, and Benoît Dupont de Dinechin</i>	
Memory Bounds for the Distributed Execution of a Hierarchical Synchronous Data-Flow Graph	160
<i>Karol Desnos, Maxime Pelcat, Jean-Francois Nezan, and Slaheddine Aridhi</i>	
Out-Of-Order Execution of Synchronous Data-Flow Networks	168
<i>Daniel Baudisch, Jens Brandt, and Klaus Schneider</i>	

Embedded Processor Design	176
<hr/>	
An Efficient Asymmetric Distributed Lock for Embedded Multiprocessor Systems	176
<i>Jochem H. Rutgers, Marco J.G. Bekooij, and Gerard J.M. Smit</i>	
Simultaneous Reconfiguration of Issue-width and Instruction Cache for a VLIW Processor	183
<i>Fakhar Anjam, Stephan Wong, Luigi Carro, Gabriel L. Nazar, and Mateus B. Rutzig</i>	
Energy Efficient Stream-based Configurable Architecture for Embedded Platforms	193
<i>Frederico Pratas, Pedro Tomás, Pedro Trancoso, and Leonel Sousa</i>	
ESL Tools and Methods	201
<hr/>	
TaBit: a Framework for Task Graph to Bitstream Generation	201
<i>Alessandra Bonetto, Andrea Cazzaniga, Gianluca C. Durelli, Christian Pilato, Donatella Sciuto, and Marco D. Santambrogio</i>	
System-on-Chip deployment with MCAPI abstraction and IP-XACT metadata	209
<i>Lauri Matilainen, Lasse Lehtonen, Joni-Matti Määttä, Erno Salminen, and Timo D. Hämäläinen</i>	
Efficient System Design using the Statistical Analysis of Architectural Bottlenecks Methodology	217
<i>Manish Arora, Feng Wang, Bob Rychlik, and Dean M. Tullsen</i>	
SPECIAL SESSION 1: Programming Paradigms for Reconfigurable Multi-Core Embedded Systems	227
<hr/>	
Introduction to the Special Session on: Programming Paradigms for Reconfigurable Multi-Core Embedded Systems	227
<i>Diana Göhringer and Pedro Diniz</i>	
Towards Future Adaptive Multiprocessor Systems-On-Chip: an Innovative Approach for Flexible Architectures	228
<i>Fabrice Lemonnier, Philippe Millet, Gabriel Marchesan Almeida, Michael Hübner, Jürgen Becker, Sébastien Pillement, Olivier Sentieys, Martijn Koedam, Shubhendu Sinha, Kees Goossens, Christian Piquet, Marc-Nicolas Morgan, and Romain Lemaire</i>	
Adaptive Reinforcement Learning Method for Networks-on-Chip	236
<i>Fahimeh Farahnakian, Masoumeh Ebrahimi, Masoud Danesh Talab, Juha Plosila, and Pasi Liljeberg</i>	
Adaptive Processor Architecture	244
<i>Michael Huebner, Diana Göhringer, Carsten Tradowky, Joerg Henkel, and Jürgen Becker</i>	
Adaptive dynamic memory allocators by estimating application workloads	252
<i>Ioannis Koutras, Alexandros Bartzas, and Dimitrios Soudris</i>	
Hardware/Software Specialization Through Aspects: The LARA Approach	260
<i>João M. P. Cardoso, Tiago Carvalho, João Teixeira, Pedro Diniz, Fernando Gonçalves, and Zlatko Petrov</i>	
From Scilab to Multicore Embedded Systems: Algorithms and Methodologies	268
<i>George Goulas, Panayiotis Alefragis, Nikolaos S. Voros, Christos Valouzis, Christos Gogos, Nikolaos Kavvadias, Grigoris Dimitroulakis, Kostas Masselos, Diana Göhringer, Steven Derrien, Daniel Ménard, Olivier Sentieys, Michael Huebner, Timo Stripf, Oliver Oey, Jürgen Becker, Gerard Rauwerda, Kim Sunesen, Dimitrios Kritharidis, and Nikolaos Mitas</i>	

SPECIAL SESSION 2: FPGA-based Emulation of Hardware Architectures 276

Introduction to the Special Session on: FPGA-based Emulation of Hardware Architectures 276
Holger Blume

BEE technology overview 277
Joseph Rothman and Chen Chang

An FPGA-Accelerated Testbed for Hardware Component Development in MIMO Wireless
Communication Systems 278
*Filippo Borlenghi, Dominik Auras, Ernst Martin Witte, Torsten Kempf, Gerd Ascheid, Rainer
Leupers, and Heinrich Meyr*

An FPGA-based Prototyping Method for Verification, Characterization and Optimization of LDPC
Error Correction Systems 286
*Panagiotis Sakellariou, Ioannis Tsatsaragkos, Nikolaos Kanistras, Ahmed Mahdi, and Vassilis
Paliouras*

A Quantitative Analysis of Fixed-Point LDPC-Decoder Implementations using Hardware-Accelerated
HDL Emulations 294
Matthias Korb and Tobias G. Noll

An FPGA-based Probability-aware Fault Simulator 302
David May and Walter Stechele

Combining on-hardware prototyping and high-level simulation for DSE of multi-ASIP systems 310
Paolo Meloni, Sebastiano Pomata, Luigi Raffo, Roberta Piscitelli, and Andy D. Pimentel

SPECIAL SESSION 3: Aspects Of Cyber-Physical Systems 318

Introduction to the Special Session on: Aspects Of Cyber-Physical Systems 318
Ed Depretere

Rigorous Design of Cyber-physical Systems 319
Joseph Sifakis

Predictable Dynamic Embedded Data Processing 320
Marc Geilen, Sander Stuijk, and Twan Basten

Efficient Computing in Cyber-Physical Systems 328
Peter Marwedel and Michael Engel

Is Time Predictability Quantifiable? 333
Martin Schoeberl

Model-Driven Robot-Software Design using integrated Models and Co-Simulation 339
Jan F. Broenink and Yunyun Ni

Multicore Enablement for Cyber Physical Systems 345
Andreas Herkersdorf

Challenges in Automotive Cyber-physical Systems Design 346
*Dip Goswami, Reinhard Schneider, Alejandro Masrur, Martin Lukasiewicz, Samarjit Chakraborty,
Harald Voit, and Anuradha Annaswamy*

A Co-simulation Approach for System-Level Analysis of Embedded Control Systems 355
Michael Glaß, Jürgen Teich, and Liyuan Zhang

Instrumentation Techniques for CyberPhysical Systems Using the Targeted Dataflow Interchange Format	363
<i>Shuvra S. Bhattacharyya</i>	
Efficient Hardware Implementation of Data-Flow Parallel Embedded Systems.....	364
<i>Patrice Quinton, Anne-Marie Chana, and Steven Derrien</i>	



Author Index	372
---------------------------	-----