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Keynote Speeches

Title	**The DARPA Diverse Accessible Heterogeneous Integration (DAHI) Program: Convergence of Compound Semiconductor Devices and Silicon-Enabled Architectures**	**1**
Date/Time	Thursday, 22 November 2012 / 08:50 – 09:30	
Room	Leo 3 & Leo 4	
Speaker	Dr. Sanjay Raman, *Microsystems Technology Office (MTO), DARPA*	

Abstract

The DARPA Diverse Accessible Heterogeneous Integration (DAHI) program is developing transistor-scale heterogeneous integration processes to intimately combine advanced compound semiconductor (CS) devices, as well as other emerging materials and devices, with high-density silicon CMOS technology. DAHI incorporates thrusts in high performance electronics, electronic-photonic integration, and the establishment of a high-yield heterogeneous integration foundry capability. A key aspect of this technology is the potential to bring to bear complex, silicon-enabled architectures for in situ calibration, linearization and signal processing, well beyond what is possible in the native CS technologies alone. This talk will discuss recent accomplishments under the DAHI program and the future outlook.

Biography

Sanjay Raman is currently serving as a Program Manager in the Microsystems Technology Office (MTO) at DARPA. He is on assignment to DARPA from Virginia Tech where he is a Professor of Electrical and Computer Engineering. His programmatic interests include: silicon-based RF/microwave mm-wave circuits; adaptive, self-correcting RF/mixed-signal circuits; high-speed compound semiconductor devices and circuits; heterogeneous integration; and communications and sensor microsystems. He received his Ph.D in Electrical Engineering from the University of Michigan in Electrical Engineering in 1998, and his Bachelor's degree in EE from Georgia Tech in 1987. From 1987-1992 he served as a Nuclear trained submarine officer in the U.S. Navy.

Title	**Past, Current, and Future Trend in Reconfigurable Transceiver Research and Development**	7
Date/Time	Thursday, 22 November 2012 / 09:30 – 10:10	
Room	Leo 3 & Leo 4	
Speaker	Prof. Kiyomichi Araki, *Tokyo Institute of Technology, Japan*	

Abstract

In 1990's a concept of software-defined radio has been proposed by Mitola. A reconfigurability of the operating parameters; center frequency, bandwidth and power level in transceivers only altered by software is one of the most important features in the software-defined radio to realize a versatile transceiver.

Here we will review research and development works in the field of reconfigurable transceiver, and discuss its future trend of this technology. In addition our work on a design of direct sampling receivers will be introduced on the topics of the reconfigurability of several these frequency characteristics; image rejection, passband widening, etc. with an enhancement of digital assist technology.

Biography

Kiyomichi Araki was born in 1949. He received the Ph.D. degrees in physical electronics from Tokyo Institute of Technology, Japan, in 1978. In 1973-1975, and 1978-1985, he was a Research Associate at Tokyo Institute of Technology, and in 1985-1995, he was an Associate Professor at Saitama University. In 1979-1980 and 1993-1994, he was a visiting research scholar at University of Texas, Austin and University of Illinois, Urbana, respectively. Since 1995 he has been a Professor at Tokyo Institute of Technology. He has numerous journals and peer review publications in RF ferrite devices, RF circuit theory, electromagnetic field analysis, software defined radio, array signal processing, UWB technologies, wireless channel modeling, MIMO communication theory, digital RF circuit design, information security, and coding theory. He received a best paper award and a Fellow from IEICE in 2007 and 2004. He is a senior member of IEEE, and a president of electronics society of IEICE of Japan and a member of IEE and Information Processing Society of Japan. He served as a steering committee chair of APMC2010, and a chair of MTT-S Japan chapter.

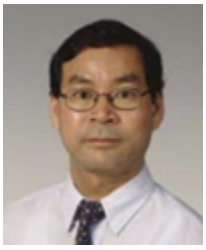
Tutorials

Title	**Power Management IC Design: DC-DC Converters and Charge Pumps** N/A
Date/Time	Wednesday, 21 November 2012 / 09:00 – 10:30 & 11:00 – 12:30
Room	Leo 3
Speakers	Prof. Wing-Hung Ki, *Hong Kong University of Science and Technology, Hong Kong*

Abstract

This tutorial covers the IC design of two major power management components: DC-DC converters and charge pumps. For DC-DC converters, second-order converters and their control schemes will be discussed. The focus is on building blocks of (i) the control loop such as RTCT oscillator, PWM compensator, hysteretic comparators, current sensing and compensation ramp; and (ii) the power stage such as power transistor design, gate drive techniques, synchronous rectification and active diodes. For charge pumps, charge balance law will be introduced, and step-up, step-down, inversion and reconfigurable charge pumps will be covered. There will also be discussion on maximizing efficiency in the presence of top- and bottom-plate parasitic capacitors, gate drive techniques, and 2-phase and multi-phase charge pumps.

Biography



Ki received his BSc degree (1984) from the University of California, San Diego, the MSc degree (1985) from the California Institute of Technology, Pasadena, and the PhD degree (1995) from the University of California, Los Angeles, all in electrical engineering.

He first joined Micro Linear Corporation, San Jose, from 1992 to 1995, working on the design of power converter controllers; and then joined the Hong Kong University of Science and Technology in 1995. He is now a professor of the Department of Electronic and Computer Engineering.

His research interests are integrated circuit techniques for power management circuits such as switching converters, charge pumps, low dropout regulators, power transponders for RFID and energy harvesting applications, and fundamental research in circuit analysis and design.

Title	THz and Millimeter-Wave Frequency Synthesis in Silicon N/A
Date/Time	Wednesday, 21 November 2012 / 09:00 – 10:30 & 11:00 – 12:30
Room	Leo 4
Speakers	Prof. Payam Heydari, *University of California, Irvine, USA*

Abstract

THz and millimeter-wave (mm-wave) imaging and sensing is considered to be one of the emerging and disruptive technologies over the next decade. THz (including the W-band) waves pass through non-conducting materials such as clothes, paper, wood and brick and so cameras sensitive to them can peer inside envelopes, into living rooms and "frisk" people at distance. THz/mm-wave imaging and sensing systems, therefore, will be key enabling components in applications such as security surveillance (to find concealed weapons and explosives), non-destructive testing, biology, radio astronomy, multi-gigabit wireless connectivity, and medical imaging. One of the most critical and daunting tasks in a THz/mm-wave system is signal generation and frequency synthesis. This tutorial presents an overview and comparative study of recent research efforts which have explored several circuit techniques and architectures leading to highly efficient frequency synthesis and signal generation in silicon.

Biography

Payam Heydari (S'98–M'00–SM'07) received the B.S. and M.S. degrees (with highest honors) in electrical engineering from the Sharif University of Technology in 1992 and 1995, respectively. He received the Ph.D. degree in electrical engineering from the University of Southern California in 2001.

Dr. Heydari is currently a Full Professor of Electrical Engineering and also School of Engineering Faculty Vice Chair. His research interests include the design of high-speed analog, radio-frequency (RF), and mixed-signal integrated circuits. He is the (co)-author of one book and 100 journal and conference papers.

The Office of Technology Alliances at UCI has named Dr. Heydari one of 10 outstanding innovators at the university. Dr. Heydari is the co-recipient of the 2009 Business Plan Competition First Place Prize Award and Best Concept Paper Award both from Paul Merage School of Business at UC-Irvine. He is the recipient of the 2010 Faculty of the Year Award from UC-Irvine's Engineering Student Council (ECS), the 2009 School of Engineering Fariborz Maseeh Best Faculty Research Award, the 2007 IEEE Circuits and Systems Society Guillemin-Cauer Award, the 2005 NSF CAREER Award, the 2005 IEEE Circuits and Systems Society Darlington Award, the 2005 UCI's School of Engineering Teaching Excellence Award, the Best Paper Award at the 2000 IEEE International Conference on Computer Design (ICCD), the 2000 Honorable Award from the Department of EE-Systems at the University of Southern California, and the 2001 Technical Excellence Award in the area of Electrical Engineering from the Association of Professors and Scholars of Iranian Heritage (APSIH). He was recognized as the 2004 Outstanding Faculty at the UCI's EECS Department. Dr. Heydari's paper entitled: Design of Ultra High-Speed Low-Voltage CMOS CML buffers and Latches, published in October 2004 issue of the IEEE TRANS. ON VLSI SYSTEMS, was ranked first among top downloaded articles in 2007. His research on novel low-power multi-purpose multi-antenna RF front-ends received the Low-Power Design Contest Award at the 2008 IEEE Int'l Symposium on Low-Power Electronics and Design (ISLPED). He is the co-founder of ZeroWatt Technologies, Inc., a fabless semiconductor startup in low power mixed signal integrated circuits design.

Dr. Heydari is a Guest Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS. He currently serves on the Technical Program Committees of Compound Semiconductor IC Symposium (CSICS) and International Symposium on Low-Power Electronics and Design (ISLPED). He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS – part I from 2006 to 2008. He was a Technical Program Committee member of the IEEE Custom Integrated Circuits Conference (CICC), and International Symposium on Quality Electronic Design (ISQED).

Title	**Analog and Digital Frequency Synthesizers N/A**
Date/Time	Wednesday, 21 November 2012 / 13:30 – 15:00 & 15:30 – 17:00
Room	Leo 3
Speakers	Prof. Michael H. Perrott, *Masdar Institute of Science and Technology, United Arab Emirates*

Abstract

Phase-locked loop (PLL) circuits are a key component of most modern communication circuits, and are also used in a variety of digital processor applications in order to generate high frequency, low jitter clock sources. This tutorial-level presentation will present an overview of analog and digital frequency synthesizers, including basic concepts and recent innovation.

Classical analog integer-N synthesizers will first be examined in order to provide background on basic PLL components, modeling, and system level tradeoffs. Analog fractional-N synthesizers will then be presented along with key concepts in Sigma-Delta modulation. Finally, digital frequency synthesizers will be examined with high performance time-to-digital conversion being a particular focus point. High level design and simulation techniques are presented, as well as recent implementation techniques of quantization noise cancellation and low jitter frequency divider structures.

Biography

Dr. Michael Perrott received a BS degree in Electrical Engineering from New Mexico State University, Las Cruces, NM in 1988, and MS and PhD degrees in Electrical Engineering and Computer Science from Massachusetts Institute of Technology in 1992 and 1997 respectively.

From 1997 to 1998, he worked at Hewlett-Packard Laboratories in Palo Alto, CA, on high speed circuit techniques for Sigma-Della synthesizers. In 1999, he was a visiting Assistant Professor at the Hong Kong University of Science and Technology, and taught a course on the theory and implementation of frequency synthesizers. From 1999 to 2001 he worked at Silicon Laboratories in Austin, TX, and developed circuit and signal processing techniques to achieve high performance clock and data recovery circuits. Dr Perrott was an Assistant and then Associate Professor in Electrical Engineering and Computer Science at the Massachusetts Institute of Technology from 2001 to 2008. From 2008 to 2010, he was Chief Circuit Architect at SiTime Corporation, a Silicon Valley startup developing clock generation and timing solutions which incorporate Micro-Electro Mechanical Systems (MEMS) resonator devices inside standard silicon electronic chips.

Title	**Millimeter-wave and TeraHertz CMOS Design N/A**
Date/Time	Wednesday, 21 November 2012 / 13:30 – 15:00 & 15:30 – 17:00
Room	Leo 4
Speakers	Prof. Minoru Fujishima, *Hiroshima University, Japan*

Abstract

Millimeter-wave and its h igher-frequency part "terahertz" have attracted many attentions to open up new applications such as ultr ahigh-speed wireless communication and noninva sive transparent image. Utilizing recent transistor performance in CMOS technology, those new applications are being realized by commercial CMOS process. Since base-band signal processors are indispensable in a system level, CMOS circuits for millimeter-wave and terahertz have advantage against compound-semiconductor circuits from viewpoint of high-volume production and low-power consumption. In this talk, we will discuss millimeter-wave and terahertz CMOS design by clarifying difference from conventional microwave design. Design examples from system level to building block for mobile high-speed communication are also discussed.

Biography

Minoru Fujishima received the B.E., M.E. and Ph.D degrees in Electronics Engineering from the University of Tokyo, Japan in 1988, 1990 and 1993, respectively. He joined faculty of the University of Tokyo in 1988 as a research associate, and was an associate professor of the School of Frontier Sciences, University of Tokyo since 1999. He was a visiting professor at the ESAT-MICAS laboratory, Katholieke, Universiteit Leuven, Belgium, from 1998 to 2000. Since 2009, he has been a professor of the Graduate School of Advanced Sciences of Matter, Hiroshima University.

He studied design and modeling of CMOS and BiCMOS circuits, nonlinear circuits, single-electron circuits, and quantum-computing circuits. His current research interests are in the designs of low-power millimeter- and short-millimeter-wave wireless CMOS circuits. He coauthored more than 40 journal papers and 100 conference papers, and a book entitled "Design and Modeling of Millimeter-Wave CMOS Circuits for Wireless Transceivers: Era of Sub-100nm Technology," published by Springer, 2008.

He is a member of IEICE, IEEE, and JSAP. He is currently serving as a technical committee member of several international conferences.

Technical Program

Session	Session TH-IF: Interactive Forum I
Date/Time	Thursday, 22 November 2012 / 10:10 – 11:10
Room	Foyer
Chair	Wang-Ling Goh, *Nanyang Technological University, Singapore*

Session	TH1A: mmWave IC
Date/Time	Thursday, 22 November 2012 / 11:10 – 12:10
Room	Leo 3
Chair	Fujiang Lin, *University of Science and Technology of China, China*
Co-Chair	Georg Boeck, *Technische Universtaet Berlin, Germany*

Session	TH1B: Filter and Delay
Date/Time	Thursday, 22 November 2012 / 11:10 – 12:10
Room	Leo 4
Chair	Kaixue Ma, *Nanyang Technological University, Singapore*
Co-Chair	Liguo Sun, *University of Science and Technology of China, China*

Session	TH2A: Dividers and VCO
Date/Time	Thursday, 22 November 2012 / 13:30 – 15:10
Room	Leo 3
Chair	Piew Yoong Chee, *I^2R, A*STAR, Singapore*
Co-Chair	Howard Luong, *The Hong Kong U. of Science and Technology*

Session	TH2B: Data Converter
Date/Time	Thursday, 22 November 2012 / 13:30 – 15:10
Room	Leo 4
Chair	Yong Ping Xu, *National University of Singapore, Singapore*
Co-Chair	Pingfen Lin, *Beijing University of Technology, China*

Session	TH3A: Special Session – SiP
Date/Time	Thursday, 22 November 2012 / 15:30 – 17:35
Room	Leo 3
Chair	Ken Sun, *Sychip Inc. USA*
Co-Chair	Xiaowu Zhang, *IME, A*STAR, Singapore*

Session	TH3B: Analog IC
Date/Time	Thursday, 22 November 2012 / 15:30 – 17:10
Room	Leo 4
Chair	Pak-Kwong Chan, *Nanyang Technological University, Singapore*
Co-Chair	Hyung-Joun Yoo, *KAIST Electrical Engineering, Korea*

Session	FR1A: Wireless Power Transfer and RFID
Date/Time	Friday, 23 November 2012 / 08:30 – 09:50
Room	Leo 3
Chair	Yuanjin Zheng, *Nanyang Technological University, Singapore*
Co-Chair	Sheng Sun, *The University of Hong Kong*

Session	FR1B: Characterization and Modeling
Date/Time	Friday, 23 November 2012 / 08:30 – 09:55
Room	Leo 4
Chair	Sivanand Krishnan, *I^2R, A*STAR, Singapore*
Co-Chair	Patrick Yue, *The Hong Kong University of Science and Technology*

Session	FR2A: Wireless Bio IC and UWB
Date/Time	Friday, 23 November 2012 / 10:15 – 12:05
Room	Leo 3
Chair	Yuan Gao, *IME, A*STAR, Singapore*
Co-Chair	Zhiliang Hong, *Fudan University, China*

Session	FR2B: Special Session – GaN
Date/Time	Friday, 23 November 2012 / 10:15 – 12:20
Room	Leo 4
Chair	Yongxin Guo, *National University of Singapore, Singapore*
Co-Chair	Arulkumaran Subramaniam, *Nanyang Technological University*

Session	FR3A: Automotive Radar and High Frequency IC
Date/Time	Friday, 23 November 2012 / 13:30 – 14:50
Room	Leo 3
Chair	Koen Mouthaan, *National University of Singapore, Singapore*
Co-Chair	Stan Skafidas, *University of Melbourne, Australia*

Session	FR3B: RF Devices
Date/Time	Friday, 23 November 2012 / 13:30 – 14:50
Room	Leo 4
Chair	Johnny Chew, *Global Foundries, Singapore*
Co-Chair	Xiao-Peng Yu, *Zhejiang University, China*

Session	FR-IF: Interactive Forum II
Date/Time	Friday, 23 November 2012 / 14:50 – 15:50
Room	Foyer
Chair	Liter Siek, *Nanyang Technological University, Singapore*

Session	FR4A: Synthesizers
Date/Time	Friday, 23 November 2012 / 15:50 – 17:15
Room	Leo 3
Chair	Chirn Chye Boon, *Nanyang Technological University*
Chair	Zhiqun Li, *Southeast University*

Session	FR4B: Power Amplifiers
Date/Time	Friday, 23 November 2012 / 15:50 – 17:15
Room	Leo 4
Chair	Bo Shi, *I^2R, A*STAR, Singapore*
Chair	Haruichi Kanaya, *Kyushu University, Japan*