

# **NORCHIP 2012**

**Copenhagen, Denmark  
12-13 November 2012**



**IEEE Catalog Number: CFP12828-PRT**  
**ISBN: 978-1-4673-2221-8**

# TABLE OF CONTENTS

<b>Design of Power Efficient FPGA based Hardware Accelerators for Financial Applications</b> .....	1
<i>Jonas Stenbæk Hegner, Joakim Sindholt, Alberto Nannarelli</i>	
<b>Architectural Trends in GHz Speed DACs</b> .....	5
<i>S. Balasubramanian, W. Khalil</i>	
<b>A Continuous-Time IR-UWB RAKE Receiver for Coherent Symbol Detection</b> .....	9
<i>Shanthi Sudalaiyandi, Tor Sverre Lande</i>	
<b>A Power Scalable and High Pulse Swing UWB Transmitter for Wirelessly-Powered RFID Applications</b> .....	13
<i>Jia Mao, Zhuo Zou, David Sarmiento, Fredrik Jonsson, Li-Rong Zheng</i>	
<b>A 26 GHz UWB CMOS IR-UWB Transmitter with On-chip Balun</b> .....	17
<i>Kristian Gjertsen Kjeldgaard, Tor Sverre Lande</i>	
<b>H.264/AVC Motion Estimation on FPGAs and GPUs: A Comparative Study</b> .....	21
<i>Iracu O. Santos, Alba S. B. Lopes, Bruno M. Carvalho, Edgard Correa, Marcio Kreutz</i>	
<b>FPGA Implementation of Elementary Generalized Unitary Rotation with CORDIC Based Architecture - Preliminary Results</b> .....	25
<i>Peteris Misans, Uldis Derums, Vents Kandars</i>	
<b>Energy Efficient MIMO Channel Pre-processor Using a Low Complexity On-Line Update Scheme</b> .....	31
<i>Chenxin Zhang, Hemanth Prabhu, Liang Liu, Ove Edfors, Viktor Owall</i>	
<b>Modeling and Design of a Dual-Residue Pipelined ADC in 130nm CMOS</b> .....	35
<i>Eirik Steen-Hansen, Trond Ytterdal</i>	
<b>A 9-bit 50MS/s Asynchronous SAR ADC in 28nm CMOS</b> .....	39
<i>Tuan-Vu Cao, Snorre Aunet, Trond Ytterdal</i>	
<b>KL-Cut Based Digital Circuit Remapping</b> .....	45
<i>Lucas Machado, Mayler Martins, Vinicius Callegaro, Renato P. Ribas, Andre I. Reis</i>	
<b>Optimal Register Allocation by Augmented Left-Edge Algorithm on Arbitrary Control-Flow Structures</b> .....	49
<i>Mark Ruvald Pedersen, Jan Madsen</i>	
<b>A Novel On-Chip Ultra-low Power Temperature Sensing Scheme</b> .....	55
<i>Shailesh Singh Chouhan, Kari Halonen</i>	
<b>Variability-aware Design of 55 nA Current Reference with 1.4% Standard Deviation and 290 nW Power Consumption</b> .....	59
<i>Francesca Cucchi, Stefano Di Pascoli, Giuseppe Iannaccone</i>	
<b>Low Power Real Time Clock With High Accuracy Over Large Supply Voltage Range</b> .....	63
<i>Wolfgang Gut, Gerald Hilber, Dominik Gruber, Manuel Kaufmann, Andreas Rauchenecker, Timm Ostermann</i>	
<b>Memory-Aware System Scenario Approach Energy Impact</b> .....	67
<i>Iason Filippopoulos, Francky Cathoor, Per Gunnar Kjeldsberg, Elena Hammari, Jos Huisken</i>	
<b>Configurable RTL Model for Level-1 Caches</b> .....	73
<i>Vahid Saljooghi, Alen Bardizbanyan, Magnus Sjalander, Per Larsson-Edefors</i>	
<b>Novel SRAM Bias Control Circuits for a Low Power L1 Data Cache</b> .....	77
<i>Azam Seyedi, Adria Armejach</i>	
<b>An Operational Amplifier for High Performance Pipelined ADCs in 65nm CMOS</b> .....	83
<i>Sima Payami, Amin Ojani</i>	
<b>Analyses of Single-Stage Complementary Self-Biased CMOS Differential Amplifiers</b> .....	87
<i>Vladimir Milovanovic, Horst Zimmermann</i>	
<b>Heart and Respiratory Detection and Simulations for Tracking Humans based on Respiration by using Pulse-Based Radar</b> .....	91
<i>Mehran Baboli, Olga Boric-Lubecke, Victor Lubecke</i>	
<b>Implementation of FPGA Based DSP Module for CW Doppler Radar: Preliminary Results</b> .....	95
<i>Maris Terauds</i>	
<b>A 2.1 <math>\mu</math>W 76 dB SNDR DT-<math>\Delta\Sigma</math> Modulator for Medical Implant Devices</b> .....	101
<i>Ali Fazli Yeknami, Atila Alvandpour</i>	
<b>Power Efficient Arrangement of Oversampling Sigma-Delta DAC</b> .....	105
<i>Nadeem Afzal, J. Jacob Wikner</i>	
<b>A 90nm CMOS Gated-Ring-Oscillator-Based 2-Dimension Vernier Time-to-Digital Converter</b> .....	109
<i>Ping Lu, Pietro Andreani, Antonio Liscidini</i>	
<b>Study and Simulation of an Example Redundant FIR Filter</b> .....	113
<i>Joakim Alvrant, J. Jacob Wikner</i>	

<b>Artificial Neural Network Emulation on NOC based Multi-Core FPGA Platform</b> .....	117
<i>Nowshad Painsa Mand, Francesco Robino, Johnny Oberg</i>	
<b>Performability of Error Control Schemes for NOC Interconnects</b> .....	121
<i>Deena M. Zamzam, A. Mohamed, Abd El Ghany, Klaus Hofmann</i>	
<b>Linearization of RF Power Amplifiers Using an Enhanced Memory Polynomial Predistorter</b> .....	126
<i>Felice Francesco Tafuri, Cataldo Guaragnella, Marco Fiore, Torben Larsen</i>	
<b>Deembedding Static Nonlinearities of Power Amplifiers Using Least Square Error Algorithm</b> .....	130
<i>Wei Wei, Jan H. Mikkelsen, Ole Kiel Jensen</i>	
<b>Wideband Reconfigurable Capacitive Shunt-Feedback LNA in 65nm CMOS</b> .....	134
<i>Imad Ud Din, Johan Wernehag, Stefan Andersson, Sven Mattisson</i>	
<b>A 2.5 GHz Self-Compensated, Bandwidth Tracking PLL with 0.8 ps Jitter</b> .....	138
<i>Mitesh Yogesh, Puneet Sareen, Markus Dietl, Ketan Dewan</i>	
<b>Testing of an off-chip NoC protocol using a BIST/Synthesizable Testbench approach</b> .....	142
<i>Saif Uddin, Johnny Oberg</i>	
<b>A Light-Weight Statically Scheduled Network-on-Chip</b> .....	147
<i>Rasmus Bo Sorensen, Martin Schoeberl, Jens Sparso</i>	
<b>Intermediate Nodes Selection Schemes for Network Coding in Network-on-Chips</b> .....	153
<i>Ahmed Shalaby, M. El-Sayed Ragab, Victor Goulart</i>	
<b>A Genetic Algorithm based Optimization Method for Low Vertical Link Density 3-Dimensional Networks-on-Chip Many Core Systems</b> .....	158
<i>Haoyuan Ying, Kris Heid, Thomas Hollstein, Klaus Hofmann</i>	
<b>Nanoscale CMOS Impulse Radar - From Research to Product</b> .....	162
<i>Dag T. Wisland</i>	
<b>Challenges in IC Design for Hearing Aids</b> .....	163
<i>Ivan Jorgensen</i>	
<b>Electrical and Human Feedback</b> .....	164
<i>Hanspeter Schmid</i>	
<b>Biochips: The Integrated Circuit of Biology</b> .....	174
<i>Jan Madsen</i>	
<b>Behavioral Modeling of Nonlinear Settling for Multiple Cascaded SC Stages</b> .....	175
<i>Jia Sun, Timo Rahkonen, Marko Neitola</i>	
<b>An Analog Receiver Front-End for Capacitive Body-Coupled Communication</b> .....	181
<i>Prakash Harikumar, Muhammad Irfan Kazim, J. Jacob Wikner</i>	
<b>A Readout Circuit for an Uncooled IR Camera With Mismatch and Self-Heating Compensation</b> .....	185
<i>Daniel Svard, Christer Jansson, Atila Alvandpour</i>	
<b>Embedded Low Power Clock Generator for Sensor Nodes</b> .....	189
<i>Oliver Schrape, Frank Vater</i>	
<b>Wideband RF Detector Design for High Performance On-Chip Test</b> .....	193
<i>Quoc-Tai Duong, Jerzy J. Dabrowski</i>	
<b>Effect of Process Variations in CMOS Chips for Radar Beamforming</b> .....	197
<i>Elias Bakken, Tor Sverre Lande, Sverre Holm</i>	
<b>SynZEN: A Hybrid TTA/VLIW Architecture with a Distributed Register File</b> .....	201
<i>Stefan Hauser, Nico Moser, Ben Juurlink</i>	
<b>A Fault-Aware Low-Energy Spare Core Allocation in Networks-on-Chip</b> .....	205
<i>Fatemeh Khalili, Hamid R. Zarandi</i>	
<b>An Accurate Fault Location Method Based on Configuration Bitstream Analysis</b> .....	209
<i>Zhou Jing, Liu Zengrong, Chen Lei, Wang Shuo, Wen Zhiping, Chen Xun, Qi Chang</i>	
<b>Lithography Analysis of Via-configurable Transistor Array Fabrics</b> .....	214
<i>Vinicius Dal Bem, Andre I. Reis, Renato P. Ribas</i>	
<b>Evaluation of Su8 Photo Polymer for Microwave Packaging Applications</b> .....	218
<i>Srinivasa Reddy Kuppireddi, Sayanu Pamidighantam, V. Janardhana, Oddvar Sorasen, J. S. Roy</i>	
<b>A Measurement Technique for the Vibrating Wire Sensors</b> .....	222
<i>Andrea Simonetti</i>	
<b>Functional Built-In Self-Test for Processor Cores in SoC</b> .....	228
<i>Raimund Ubar, Viljar Indus, Oliver Kalmend, Teet Evartson, Elmet Orasson</i>	
<b>PathAware: A Contention-aware Selection Function for Application-specific Network-on-Chips</b> .....	232
<i>Behrad Niazmand, Midia Reshadi, Akram Reza</i>	
<b>A Survey on Mixed Operating Mode/Self Synchronization</b> .....	238
<i>Dipak S. Marathe</i>	
<b>Integration of TTA Processor tools to Kactus2 IP-XACT Design Flow</b> .....	241
<i>Lauri Matilainen, Sakari Lahti, Otto Esko, Erno Salminen, Timo D. Hamalainen</i>	
<b>Author Index</b>	