

2012 International Conference on Field-Programmable Technology

(FPT 2012)

**Seoul, South Korea
10-12 December 2012**



**IEEE Catalog Number: CFP12528-PRT
ISBN: 978-1-4673-2846-3**

Table of Contents

Session 1.2 Design Methods and Techniques for FPGAs

1.2.1	Rapid RTL-based Signal Ranking for FPGA Prototyping1 <i>Steven J.E Wilton^{1,2}, Bradley R. Quinton¹, Eddie Hung²</i> ¹ Tektronix, ² University of British Columbia
1.2.2	K-Way Partitioning Based Packing for FPGA Logic Blocks without Input Bandwidth Constraint8 <i>Wenyi Feng</i> Microsemi Corporation
1.2.3	Neural Network Based Pre-placement Wirelength Estimation16 <i>Qiang Liu, Jianguo Ma, Qijun Zhang</i> Tianjin University
1.2.4	Heterogeneous Configuration Memory Scrubbing for Soft Error Mitigation in FPGAs23 <i>Ju-Yueh Lee¹, Cheng-Ru Chang¹, Naifeng Jing², Juexiao Su¹, Shijie Wen³, Rich Wong³, Lei He¹</i> ¹ University of California, Los Angeles, ² Shanghai Jiao Tong University, ³ Cisco System Inc.

Session 1.3 Posters

1.3.1	FPGA based Memory Efficient High Resolution Stereo Vision System for Video Tolling29 <i>Yi Shan¹, Zilong Wang¹, Wenqiang Wang¹, Yuchen Hao¹, Yu Wang¹, Kuenhung Tsof², Wayne Luk², Huazhong Yang¹</i> ¹ Tsinghua University, ² Imperial College London
1.3.2	A Task-level OOO Framework for Heterogeneous Systems33 <i>Junneng Zhang, Chao Wang, Xi Li, Peng Chen, Xiaojing Feng, Xuehai Zhou</i> University of Science and Technology of China
1.3.3	FPGA-GPU-CPU Heterogenous Architecture for Real-time Cardiac Physiological Optical Mapping37 <i>Pingfan Meng, Matthew Jacobsen, Ryan Kastner</i> University of California, San Diego
1.3.4	Managing Mutex Variables in a Cache-Coherent Shared-Memory System for FPGAs ...43 <i>Vincent Mirian, Paul Chow</i> University of Toronto
1.3.5	FPGA Optimized Packet-Switched NoC Using Split and Merge Primitives47 <i>Yutian Huan, André DeHon</i> University of Pennsylvania
1.3.6	Parallel Dataflow Execution for Sequential Programs on Reconfigurable Hybrid MPSoCs53 <i>Chao Wang¹, Xi Li¹, Xuehai Zhou¹, Yajun Ha²</i> ¹ University of Science and Technology of China, ² National University of Singapore
1.3.7	Guppy: A GPU-like Soft-Core Processor57 <i>Abdullah Al-Dujaili¹, Florian Deragisch², Andrei Hagiescu³, Weng-Fai Wong³</i> ¹ Nanyang Technological University, ² ETH Zürich, ³ National University of Singapore
1.3.8	A High Speed Open Source Controller for FPGA Partial Reconfiguration61 <i>Kizheppatt Vipin, Suhaib A. Fahmy</i> Nanyang Technological University
1.3.9	Design Space Exploration and Implementation of a High Performance and Low Area Coarse Grained Reconfigurable Processor67 <i>Dongkwan Suh, Kiseok Kwon, Sukjin Kim, Soojung Ryu, Jeongwook Kim</i> Samsung Electronics

Session 1.4 FPGA Architectures and Networks

1.4.1	Small Virtual Channel Routers on FPGAs Through Block RAM Sharing71 <i>Jimmy Kwa, Tor M. Aamodt</i> University of British Columbia
1.4.2	uBRAM-Based Run-Time Reconfigurable FPGA and Corresponding Reconfiguration Methodology80 <i>Yi-Chung Chen¹, Wenhua Wang¹, Wei Zhang², Hai Li¹</i> ¹ Polytechnic Institute of NYU, ² Nanyang Technological University
1.4.3	An FPGA with Power-Gated Switch Blocks87 <i>Assem A. M. Bsoul, Steven J. E. Wilton</i> University of British Columbia
1.4.4	Design Tradeoffs for Hard and Soft FPGA-Based Networks-on-Chip95 <i>Mohamed S. Abdelfattah, Vaughn Betz</i> University of Toronto

Session 1.5 Posters

1.5.1	Rule-Based Data Communication Optimization Using Quantitative Communication Profiling104 <i>Cuong Pham-Quoc, Zaid Al-Ars, Koen Bertels</i> Delft University of Technology
1.5.2	Parametric Reconfigurable Designs with Machine Learning Optimizer109 <i>Maciej Kurek, Wayne Luk</i> Imperial College London
1.5.3	Option Space Exploration Using Distributed Computing for Efficient Benchmarking of FPGA Cryptographic Modules113 <i>Benjamin Brewster, Ekawat Homsirikamol, Rajesh Velegali, Kris Gaj</i> George Mason University
1.5.4	A Study of Adaptable Co-Processors for Cyclic Redundancy Check on an FPGA119 <i>Amila Akagic, Hideharu Amano</i> Keio University
1.5.5	Side-Channel Resistant AES Architecture Utilizing Randomized Composite Field Representations125 <i>Bernhard Jung^{1,2}, Marc Stöttinger³, Jan Gampe¹, Steffen Reith¹, Sorin A. Huss³</i> ¹ Hochschule Rhein-Main, ² easycore GmbH, ³ Technische Universität Darmstadt,
1.5.6	Resiliency-Aware Scheduling: Resource Allocation for Hardened Computation on Configurable Devices129 <i>Jeremy Abramson, Pedro C. Diniz</i> University of Southern California
1.5.7	FPGA-Based Design and Implementation of an Approximate Polynomial Matrix EVD Algorithm135 <i>Server Kasap, Soydan Redif</i> European University of Lefke
1.5.8	Automatic Rectification of Design Errors in Complex Processors with Programmable Hardware141 <i>Amir Masoud Gharehbaghi, Masahiro Fujita</i> University of Tokyo
1.5.9	Verification of Streaming Hardware and Software Codesigns147 <i>Tim Todman, Peter Boehm, Wayne Luk</i> Imperial College London

Session 1.6 Soft Processors and Object Detectors

1.6.1	iDEA: A DSP Block Based FPGA Soft Processor151 <i>Hui Yan Cheah, Suhaib A. Fahmy, Douglas L. Maskell</i> Nanyang Technological University
1.6.2	A Memory-Efficient Parallel Single Pass Architecture for Connected Component Labeling of Streamed Images159 <i>Michael Klaiber, Lars Rockstroh, Zhe Wang, Yousef Baroud, Sven Simon</i> University of Stuttgart
1.6.3	An Energy-Efficient, Fast FPGA Hardware Architecture for OpenCV-Compatible Object Detection166 <i>Braiden Brousseau, Jonathan Rose</i> University of Toronto
1.6.4	A High-Performance Architecture for Training Viola-Jones Object Detectors174 <i>Charles Lo, Paul Chow</i> University of Toronto

Session 2.2 Efficient Implementation of Applications on FPGAs

2.2.1	A Fully-Pipelined Expectation-Maximization Engine for Gaussian Mixture Models182 <i>Ce Guo^{1,2}, Haohuan Fu², Wayne Luk¹</i> ¹ Imperial College London, ² Tsinghua University
2.2.2	Software/Hardware Framework for Generating Parallel Gaussian Random Numbers Based on the Monty Python Method190 <i>Yuan Li¹, Paul Chow², Jiang Jiang³, Minxuan Zhang¹, Shaojun Wei⁴</i> ¹ National University of Defense Technology, ² University of Toronto, ³ Shanghai Jiao Tong University, ⁴ Tsinghua University
2.2.3	Design Considerations of Real-Time Adaptive Beamformer for Medical Ultrasound Research Using FPGA and GPU198 <i>Junyong Chen, Alfred C.H. Yu, Hayden K.-H. So</i> University of Hong Kong
2.2.4	Designing a Hardware in the Loop Wireless Digital Channel Emulator for Software Defined Radio206 <i>Janarбек Matai¹, Pingfan Meng¹, Lingjuan Wu¹, Brad Weals², Ryan Kastner¹</i> ¹ University of California, San Diego, ² Toyon Research Corporation

Session 2.3 Posters

- 2.3.1 Investigation of Aging Effects in Different Implementations and Structures of Programmable Routing Resources of FPGAs215**
Abdulazim Amouri, Saman Kiamehr, Mehdi Tahoori
Karlsruhe Institute of Technology
- 2.3.2 Accelerated Evaluation of SEU Failure-in-Time Using Frame-Based Partial Reconfiguration220**
Yoshihiro Ichinomiya, Kohei Takano, Motoki Amagasaki, Morihiro Kuga, Masahiro Iida, Toshinori Sueyoshi
Kumamoto University
- 2.3.3 Introducing Irregularity to Routing Architecture of Structured ASIC for Better Routability224**
Insup Shin, Donkyu Baek, Youngsoo Shin
Korea Advanced Institute of Science and Technology
- 2.3.4 VersaPower: Power Estimation for Diverse FPGA Architectures229**
Jeffrey B. Goeders, Steven J.E. Wilton
University of British Columbia
- 2.3.5 Pipeline Frequency Boosting: Hiding Dual-Ported Block RAM Latency Using Intentional Clock Skew235**
Alexander Brant, Ameer Abdelhadi, Aaron Severance, Guy G.F. Lemieux
University of British Columbia
- 2.3.6 Acceleration of Fault Attack Emulation by Consideration of Fault Propagation239**
Armin Krieg¹, Johannes Grinschgl¹, Christian Steger¹, Reinhold Weiss¹, Holger Bock², Josef Haid²
¹Graz University of Technology, ²Infineon Technologies Austria AG
- 2.3.7 Implementation of a Volume Rendering on Coarse-Grained Reconfigurable Multiprocessor243**
Seunghun Jin, Sangheon Lee, Moo-Kyoung Chung, Yeongon Cho, Soojung Ryu
Samsung Advanced Institute of Technology
- 2.3.8 Area Constraint Propagation in High Level Synthesis247**
Razvan Nane, Vlad-Mihai Sima, Koen Bertels
Delft University of Technology
- 2.3.9 A Hardware Security Module for Quadrotor Communication253**
Abdulhadi Shoufan
Khalifa University of Science, Technology and Research
- 2.3.10 A New Hardware Coprocessor for Accelerating Notification-Oriented Applications257**
Eduardo Peters, Ricardo P. Jasinski, Volnei A. Pedroni, Jean M. Simão
Federal University of Technology – Paraná (UTFPR)

Session 2.4 Reconfigurable Architectures for Parallel Computing

- 2.4.1 VENICE: A Compact Vector Processor for FPGA Applications261**
Aaron Severance, Guy Lemieux
University of British Columbia
- 2.4.2 A Partially Reconfigurable Architecture Supporting Hardware Threads269**
*Ying Wang¹, Jian Yan¹, Xuegong Zhou¹, Lingli Wang¹,
Wayne Luk², Chenglian Peng³, Jiarong Tong¹*
¹Fudan University, ²Imperial College London, ³Fudan University
- 2.4.3 Software-Managed Automatic Data Sharing for Coarse-Grained
Reconfigurable Coprocessors277**
Toan X. Mai, Jongeun Lee
Ulsan National Institute of Science and Technology
- 2.4.4 Graph Minor Approach for Application Mapping on CGRAs285**
Liang Chen, Tulika Mitra
National University of Singapore

Session 2.5 Demonstrations

- 2.5.1 Dynamic Power Control with a Heterogeneous Multi-Core System Using a 3-D Wireless Inductive Coupling Interconnect293**
Yusuke Koizumi¹, Hideharu Amano¹, Hiroki Matsutani¹, Noriyuki Miura¹, Tadahiro Kuroda¹, Ryuichi Sakamoto², Mitaro Namik², Kimiyoshi Usami³, Masaaki Kondo⁴, Hiroshi Nakamura⁵
¹Keio University, ²Tokyo University of Agriculture and Technology, ³Shibaura Institute of Technology, ⁴University of Electro-Communications, ⁵University of Tokyo
- 2.5.2 Area-Time Estimation of C-Based Functions for Design Space Exploration297**
Yan Lin Aung, Siew-Kei Lam, Thambipillai Srikanthan
Nanyang Technological University
- 2.5.3 An Island-Style-Routing Compatible Fault-Tolerant FPGA Architecture with Self-Repairing Capabilities301**
Hasan Baig, Jeong-A Lee
Chosun University
- 2.5.4 Streamed High Dynamic Range Imaging305**
Donald G Bailey
Massey University
- 2.5.5 SimXMD: Integrated Debugging of C Code and Hardware Components309**
Ruediger Willenberg, Paul Chow
University of Toronto

Session 2.6 Special Session: Architectures and Compilers for Future Coarse-Grained Reconfigurable Processors

- 2.6.1 Design Evaluation of OpenCL Compiler Framework for Coarse-Grained Reconfigurable Arrays313**
Hee-Seok Kim¹, Minwook Ahn², John A. Stratton¹, Wen-mei W. Hwu¹
¹University of Illinois at Urbana-Champaign, ²Samsung Advanced Institute of Technology
- 2.6.2 SCC Based Modulo Scheduling for Coarse-Grained Reconfigurable Processors321**
Wonsub Kim, Donghoon Yoo, Haewoo Park, Minwook Ahn
Samsung Advanced Institute of Technology
- 2.6.3 ULP-SRP: Ultra Low Power Samsung Reconfigurable Processor for Biomedical Applications329**
Changmoo Kim¹, Mookyoung Chung¹, Yeongon Cho¹, Mario Konijnenburg², Soojung Ryu¹, Jeongwook Kim¹
¹Samsung Advanced Institute of Technology, ²Holst Centre / imec
- 2.6.4 Efficient Performance Scaling of Future CGRAs for Mobile Applications335**
Yongjun Park, Jason Jong Kyu Park, Scott Mahlke
University of Michigan

Session 3.2 Acceleration of Specific Functions Using FPGAs

- 3.2.1 ZIP-IO: Architecture for Application-Specific Compression of Big Data343**
Sang Woo Jun¹, Kermin E. Fleming¹, Michael Adler², Joel Emer^{1,2}
¹Massachusetts Institute of Technology, ²Intel Corporation
- 3.2.2 Parallelizing Sparse LU Decomposition on FPGAs352**
Guiming Wu¹, Xianghui Xie¹, Yong Dou², Junqing Sun³, Dong Wu¹, Yuan Li²
¹State Key Laboratory of Mathematical Engineering and Advanced Computing,
²National University of Defense Technology, ³Marvell Semiconductor
- 3.2.3 Minimizing the Error: A Study of the Implementation of an Integer Split-Radix FFT on an FPGA for Medical Imaging360**
Mohammad Reza Mohammadnia, Lesley Shannon
Simon Fraser University
- 3.2.4 Low Complexity and Hardware-Friendly Spectral Modular Multiplication368**
Donald Donglong Chen¹, Gavin Xiaoxu Yao¹, Çetin Kaya Koç², Ray C.C. Cheung¹
¹City University of Hong Kong, ²University of California, Santa Barbara