

# **2012 IEEE 21st Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS 2012)**

**Tempe, Arizona, USA  
21 – 24 October 2012**



**IEEE Catalog Number: CFP12EPP-PRT  
ISBN: 978-1-4673-2539-4**

# TABLE OF CONTENTS

## Novel Signaling Techniques

Ultra-High Speed Memory Bus Using Microwave Interconnects .....	3
Design and Analysis of a High-Speed Channel for Coded Differential Signaling.....	7
S-Parameter Based Multimode Signaling.....	11
Ultra-Low Power On-Chip Differential Interconnects Using High-Resolution Comparator.....	15

## Systems

Framework for Co-Simulation of Signal and Power Integrity in Server Systems.....	21
Thermal Analysis and Optimization of 2.5-D Integrated Voltage Regulator.....	25
Minimizing Simultaneous Switching Noise at Reduced Power with Power Transmission Lines for High-Speed Signaling .....	29
System-Level Performance Optimization and Benchmarking for On-Chip Graphene Interconnect.....	33

## Channels and Memory Interfaces

Challenges in Extending Single-Ended Graphics Memory Data Rates.....	39
Modeling and Measurement of Supply Noise Induced Jitter in a 12.8Gbps Single-Ended Memory Interface.....	43
Simultaneous Switching Noise Analysis of Reference Voltage Rails for Pseudo Differential Interfaces .....	47
Frequency Domain Analysis of Jitter Amplification in Clock Channels .....	51
Electrical Interconnect Design for Testing of High-Speed IC Transceivers .....	55

## Statistical Modeling

A Statistical Assessment of Opto-Electronic Links.....	61
Frequency- and Time-Domain Stochastic Analysis of Lossy and Dispersive Interconnects in a SPICE-Like Environment .....	65
Fast Assessment of the Impact of Surrounding Wiring on the Transmission Properties of High-Speed Interconnect Channels .....	69

## Special Session: TSV and 3D Packaging

Mitigating TSV-Induced Substrate Noise Coupling in 3-D IC Using Buried Interface Contacts .....	75
Power-Bandwidth Trade-off on TSV Array in 3D IC and TSV-RDL Junction Design Challenges .....	79
Comparison of TSV-Based PDN-Design Effects Using Various Stacking Topology Methods.....	83

New Power Delivery Scheme for 3D ICs to Minimize Simultaneous Switching Noise for High Speed I/Os .....	87
Measurement of SSO Noise and PDN Impedance of 3D SiP with 4k-IO Widebus Structure .....	91
A Compact On-Interposer Passive Equalizer for Chip-to-Chip High-Speed Data Transmission .....	95

## **Passive Component Modeling and Design**

Electrical Performance of Via Transitions in the Presence of Overlapping Anti-Pads .....	101
Circuit Modeling of Nonlinear Lossy Frequency Dependent Thin-Film Magnetic Inductors .....	105
Optimization of the Stub-Alternated and Serpentine Microstrip Structures to Minimize Far-End Crosstalk .....	109
A Discussion of an Analytical Per-Unit-Length Impedance Matrix Model .....	113

## **Fast Circuit Simulation and Performance Estimation**

An Efficient Method for Transient Simulation of High-Speed Interconnects with Nonlinear Terminations .....	119
I/O Supply Current Synthesis for Power Integrity Analysis of Single-Ended Signaling Scheme.....	123
An Enhanced Current Mirror for SSO Simulation .....	127
Eye Prediction of Digital Driver with Power Distribution Network Noise .....	131
Enhanced Eye-Height Estimation of Mismatched Lossy Transmission Lines.....	135

## **Electromagnetic Fields and Waves**

Fundamental Components of the IC Packaging Electromagnetic Interference (EMI) Analysis.....	141
Graphene-Based EMI Shielding for Vertical Noise Coupling Reduction in 3D Mixed-Signal System.....	145
Bandwidth and Gain Enhancement of Antenna in Package .....	149
Embedded Toroidal Magnetic Coupling Probe in Multi-Layer PCBs for Current Measurement.....	153

## **Electromagnetic Simulation**

An Unconditionally Stable Finite-Element Time-Domain Layered Domain-Decomposition Algorithm for Simulating 3D High-Speed Circuits .....	159
A New Efficient Method for Modeling Dense Via Arrays with 1D Discretization in 2D Method of Moment and Group T Matrix .....	163
Accurate and Efficient Computation of Power Plane Pair Inductance .....	167
Coupled 2D Telegrapher's Equations for PDN Analysis .....	171

## CAD I

A Partial Homomorphic Encryption Scheme for Secure Design Automation on Public Clouds .....	177
Hybrid Aggregated-Vector Algorithm for Efficient Parallelization of Fast Multipole Method .....	181
Loewner-Matrix Based Efficient Algorithm for Frequency Sweep of High-Speed Modules .....	185

## CAD II

Improved Procedure to Test Causality of Tabulated S-Parameters .....	191
Convex Passivity Enforcement of Linear Macromodels via Alternate Subgradient Iterations .....	195
Simulation-Based Design of High Dimensional Electromagnetic Systems .....	199

## Poster Session

Coupling Through Finite Ground Plane .....	205
Minimizing Displacement Return Currents in Multilayer Via Structures .....	208
Unconventional Applications of Conventional IBIS Models .....	P IC
Validation of Reduced-Terminal Models in Fast SSN Analysis .....	216
Chip Oriented Target Impedance for Digital Power Distribution Network Design .....	220
A Mixed-Domain Behavioral Model's Extraction for Digital I/O Buffers .....	224
Wafer-Level TSV Connectivity Test Using Ring Oscillator Scheme .....	228
Novel Crosstalk Modeling for Multiple Through-Silicon-Vias (TSV) on 3-D IC: Experimental Validation and Application to Faraday Cage Design .....	232
Skin Effect Modeling of Interconnects Using the Laguerre-FDTD Scheme .....	236
Transient Analysis of High-Speed Channels via Newton-GMRES Waveform Relaxation .....	240
Novel Technology for Power and Signal Integrity Using a Metal Particle Conductive Layer .....	244
Effect of Adjacent Power Distribution Grids on the Quality Factor of On-Chip Spiral Inductors .....	P IC
Waveform Relaxation with Overlapping based Partitioning for Fast Transient Simulation of Package/Board Power Distribution Networks .....	252
The Odd Couple: Antiresonance Control by Two Capacitors of Unequal Series Resistances .....	256
Characterizing the Impact of Conductor Surface Roughness on CB-CPW Behavior via Reduced Computational Complexity .....	260
Interposers for Power Supply Voltage Noise Reduction .....	264
Modeling and Analysis of SSN in Silicon and Glass Interposers for 3D Systems .....	268
Simulation and Measurement Correlation of Random Rough Surface Effects in Interconnects .....	272
Modeling differential Through-Silicon-Vias (TSVs) with large signal, non-linear capacitance .....	276
Using the Latency Insertion Method (LIM) to Generate X Parameters .....	280

Nonlinear Block-Type Leapfrog Scheme for the Fast Simulation of Multiconductor Transmission Lines with Nonlinear Drivers and Terminations .....	284
Hybrid Modeling Method for Transient Simulation of Multilayered Power/Ground Planes .....	288
On Aperture Coupling based Compact System of Lens Enhanced Phased Array .....	292
A Novel Miniaturized Bandstop Filter Using Defected Ground on System in Package (SiP)....	296
An Implementation of Interleaved Microstrip Motherboard Routing in Multi-Gbps I/O Channel Margin Improvement.....	299
Electrical Design and Performance of a Multichip Module on a Silicon Interposer .....	303
Current Distribution and Internal Impedance of Interconnect.....	307
On Analytic Model of Multiple Vias for High-Speed Printed Circuit Board and Electric Band-Gap Structures .....	311
Fast Analysis of the Impact of Interconnect Routing Variability on Signal Degradation .....	315
Common-Mode Noise Mitigation with the CM Choke in High-Speed LVDS Design .....	P 1C
Findings and Considerations for I/O Clock Jitter on a Source Synchronous Front Side Bus .....	323
Eye Diagram Parameter Extraction of Nano Scale VLSI Interconnects .....	327
Frequency and Time Domain Measurement of Through-Silicon Via (TSV) Failure.....	331
Thermal Characterization of TSV-Based 3D Stacked ICs .....	335
Modeling Broadside Coupled Traces Using Equivalent Per Unit Length (Eq PUL) RLGC Model .....	339
AMillimeter-wave Coplanar Interconnects and Radiators on FR-4 Laminates.....	343
Chip-Package Co-Design for Suppressing Parallel Resonance and Power Supply Noise .....	347
Author Index .....	351