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Day 2 – December 6, 2012

9.00 - 10.0 **F 104**	**Inauguration: Prof. V. S. Rao, Director, BITS Pilani Hyderabad**

Plenary talk

Chair – P. V. Ananda Mohan

10.00 – 11.00 **F 104**	**Microelectronics-based Implantable Devices for Bio-Medical Applications** **Takashi Tokuda** *Nara Institute of Science and Technology, 8916-5 Takayama, Ikoma, Nara, 630-0192, Japan*

DSP Building Blocks & VLSI Technology (Session – A) **Venue: F 104**

Chair - P.A. Govindacharyulu

TIME	TITLE / AUTHOR	
11.30 – 11.45	A Reconfigurable Parallel Prefix Ling Adder with modified Enhanced Flagged Binary Logic ***Soumya Ganguly, Abhishek Mittal and Syed Ershad Ahmed, BITS-Pilani, Hyderabad Campus***	1
11.45 – 12.00	Design and Error Analysis of a Scale Free CORDIC Unit with Corrected Scale Factor ***N Prasad, A4yas Kanta Swain and K. K. Mahapatra, NIT Rourkela***	7
12.00 – 12.15	HotSpot Minimization using Fine-grained DVS Architecture at 90 nm Technology ***Rajdeep Mukherjee, Priyankar Ghosh and Ajit Pal, IIT Kharagpur***	13
12.15 – 12.30	Leakage Power Recovery in Spare Cells by using State Dependent Leakage Tables from Library models ***Vasantha Kumar B.V.P., Synopsys (India) Pvt Ltd, N.S. Murthy Sharma, BVCE College, Odalarevu, K. Lal Kishore, JNTU Ananthapur and Nitika Goel, NIET, Greater Noida***	19
12.30 – 12.45	A Low Power CMOS Voltage Mode SRAM Cell for High Speed VLSI Design ***Rajib Kar, NIT Durgapur, Prashant Upadhyay, M.M. University, Solan, Durbadal Mandal, NIT Durgapur and Sakti Ghoshal, NIT Durgapur***	25
10.45 – 11.00	LOBS: Local Background Subtractor for Video Surveillance ***Kalyan Hati, Pankaj Sa and Banshidhar Majhi, NIT Rourkela***	29

Keynote Session (Women in Engineering)

Chair – Kaleem Fatima

Time / Venue	
2.00 – 2.30 **F 104**	**Microelectronics and Opportunities for Women Engineers** **Y.V.S. Lakshmi** *Center for Development of Telematics (C-DOT), Bangalore*

Women in Engineering (Session B1) **Venue: F 104**

Chair - N. Vasantha

Women in Engineering		
TIME	**TITLE/AUTHOR**	
2.45 – 3.00	Near Lossless Image Compression System ***A.S. Mamatha and Vipula Singh, RNSIT, karnataka***	35
3.00 – 3.15	Studies on the dependence of breakdown voltages LDMOS devices on their structure and doping profiles of LDD regions ***Roji Marjorie, Saveeta School of Engineering, P.A. Govindacharyulu, Vasavi College of Engineering and K. Lal Kishore, JNTU Anantapur***	42
3.15 - 3.30	Design of Highly Efficient Charge Pump for Energy Harvesting RFID Applications ***Shabana Shaik, Asudeb Dutta, Hari Shanker, Chandra Thej, Shiv Singh and Rajesh Pandava, IIT Hyderabad***	46
3.30 – 3.45	Design and Analysis of Five Port Router for Network ON CHIP ***S. Swapna, Ayas Kant Swain and K.K. Mahapatra, NIT-Rourkela***	51

Power Electronics (Session B2) **Venue: F 101**

Chair - U. M. Rao

Power Electronics		
TIME	**TITLE/AUTHOR**	
2.45 – 3.00	A Fast Hysteretic Buck DC-DC Converter with Start-up Overshoot Suppression Technique ***Kun Chun Chang, National Central University, Jhongli, Taiwan, Chin-Long Wey, National Chiao Tung University, Hsinchu, Taiwan***	56
3.00 – 3.15	Bidirectional Flyback DC-DC Converter for Hybrid Electric Vehicle: Utility, Working and PSPICE Computer Model ***Mohd. Kashif, Aligarh Muslim University, Aligarh***	61
3.15 – 3.30	A Voltage-Mode Hysteretic Boost DC-DC Converter with Dual Control Modes ***Chung-Hsien Hsu, Tai-Wei Chang, National Central University, Jhongli, Taiwan and Chin-Long Wey, National Chiao Tung University, Hsinchu, Taiwan***	67
3.30 – 3.45	Comparison of Three Popular Control Strategies Used in Shunt Active Power Filters ***Anant Naik and Uday Kumar Yaragatti, NITK Surathkal***	72

Digital Design (Session C1) **Venue: F 104**

Chair - S.K. Sahoo

DIGITAL DESIGN		
TIME	**TITLE/AUTHOR**	
4.30 – 4.45	Variable Input Delay CMOS logic for Dynamic IR Drop Reduction ***Vasantha Kumar B.V.P., Synopsys (India) Pvt. Ltd, Lal Kishore, JNTU Ananthapur, N.S. Murthy Sharma, BVCE, Odalarevu and A. Rajakumari, BVRIT, Narsapur***	79
4.45 – 5.00	Design of Encoder for Ternary Logic Circuits ***Viswa Saidutt P, Srinivas V, Sai Phaneendra P, BITS-Pilani, Hyderabad Campus and Moorthy Muthukrishnan N, G. Narayanamma Institute of Technology and Science, Hyderabad***	85

Power Electronics (Session C2) **Venue: F 101**

Chair - Banakara Basavaraja

POWER ELECTRONICS		
TIME	**TITLE/AUTHOR**	
4.30 – 4.45	Harmonic Load Impedance modeling of Television Set using Kalman filtering algorithm and Experimental Verification ***Sunil Kumar Gunda, T. Ravi Kumar and D.V.S.S. Siva Sarma, NIT Warangal*** ***(Presenting by Banakara BasavaRaja)***	89
4.45 – 5.00	Control of Buck Converter by Polynomial, PID and PD Controllers ***Madhu kiran, Thota Saradhi, Blekinge Institute of Technology (BTH), Karlskrona, Sweden, Bitra Sridhar and Kanupuru Dileesh, Andhra University, Visakhapatnam***	94

Day 3 – December 7, 2012

Keynote Session

Chair – Y Yoganandam

Time / Venue	
9.00 - 10.00 **F 104**	**Roll out of 3G, 4G and LTE - Progress and Challenges** **T.H. Chowdary** *Director, Center for Telecom Management & Studies*

VLSI Signal Processing (Image and Video) (Session – D) **Venue: F 104**

Chair - Kaleem Fatima

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10.30 – 10.45	Pass-Parallel VLSI Architecture of BPC for Embedded Block Coder in JPEG2000 ***Ramulu Gavvala, Madan Mekala, S Srinivasa Rao, ATRI, Hyderabad and Sharath Chandra, BIET, Hyderabad***	111
10.45 – 11.00	Analysis of Propagation Delay in Mixed Carbon Nanotube Bundle as Global VLSI Interconnects ***Manoj Kumar Majumder, Pankaj Kumar Das, Brajesh Kumar Kaushik and Sudeb Dasgupta, IIT Roorkee***	118

Keynote Session

Chair – Moorthy Muthukrishnan

Time / Venue	
11.15 - 11.45 **F 104**	**MEMS Technology Development at SITAR** **A Linga Moorthy** *CEO, SITAR (Society for Integrated Circuit Technology and Applied Research)*

Analog Mixed Signal VLSI Design (Session – E) **Venue: F 104**

Chair - P.V. Ananda Mohan **Co - Chair - Ramesh Vaddi**

TIME	TITLE/AUTHOR	
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1.00 – 1.15	A Low Power CMOS Current Mode Bandgap Reference Circuit with Low Temperature Coefficient of Output Voltage ***Mahesh Kumar, BITS-Pilani, Hyderabad Campus and Krishna Kumar Movva***	144

Keynote Session (Microelectronics Education)

Chair – M.B. Srinivas

Time / Venue	
2.00 - 2.30 **F 104**	**VLSI Education : Govt. of India Initiatives** **Debashish Dutta** *Senior Director, Ministry of Information and Communication Technologies, Govt. of India*

VLSI Routing (Session – F) **Venue: F 104**

Chair – K. Subbarangiah

TIME	TITLE/AUTHOR	
2.45 – 3.00	Crosstalk Noise Estimation for Generic RLC Trees with Capacitive Coupling ***Rajib Kar, Kapil Khare, Durbadal Mandal, Anup Bhattacharjee, NIT Durgapur and Vikas Maheshwari, ASU, Gurgaon***	150
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Nanotechnology (Session – G) **Venue: F 104**

Chair – N Moorthy Muthukrishnan

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Venue: LTC **Time: 1.30 – 4.00**

Chair – M. Geetha Kumari

TITLE & AUTHOR	
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Venue: LTC **Time: 1.30 - 3.45**

Chair - Subha Mada

TITLE & AUTHOR	
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