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Advance Program

Monday, December 10, 2012

Howard International House

08:40-09:00 **Opening**

Visionary Hall, 1F

09:00-09:40 **Keynote Speech: SiPs making Center Stage**

Dr. Ho-Ming Tong

ASE Group, Taiwan

Visionary Hall, 1F

09:40-10:10 **Break**

10:10-12:15 **Special Session in 3D ICs**

Chairs: Madhavan Swaminathan, Georgia Institute of Technology, USA

Wei-Chung Lo, Industrial Technology Research Institute, Taiwan

Visionary Hall, 1F

S-1 **Design and Manufacturing Innovations in Die Stacking (invited)** **BK!**

John Y. Xie — Altera Corp.

S-2 **(Invited)** BK!

Dinos Huang — ASE Group

S-3 **SI/PI co-integrity design for multi-Gbps interfaces (invited)** **BK!**

Woong Hwan Ryu — Samsung Electronics Co., Ltd.

S-4 **An Electromagnetic Modeling Tool for 3D Integration Design (invited)** **BK!**

Ki Jin Han — Ulsan National Institute of Science and Technology

S-5 **The quest for a new dimension of system integration (invited)** BK!

Sean Lee — TSMC

12:15-14:00 **Lunch**

Garden Cafeteria, 1F

13:20-14:00 **Poster session I** (Detailed program on page XV)

Room 201, 2F

14:00-14:40 **Keynote Speech: New 3D Integration Technology and Fabrication of Prototype 3D LSIs** **BK!**

Prof. Mitsumasa Koyanagi

New Industry Creation Hatchery Center (NICHe), Tohoku University, Japan

Visionary Hall, 1F

14:40-15:40 **Session A: EDA and Testing for 3D IC**

Chairs: An-Yu Kuo, Cadence, US

Yi-Chang Lu, National Taiwan University, Taiwan

Visionary Hall, 1F

15:40-16:20 **Break**

15:40-16:20 **Poster session I** (Detailed program on page XV)
Room 201, 2F

16:20-17:40 **Session B: Power Integrity / Ground Noise**
Chairs: Hideki Asai, Shizuoka University, Japan
Dale Becker, IBM, USA
Visionary Hall, 1F

B-4 **An Explicit and Unconditionally Stable Finite Difference Scheme for the Fast Transient Analysis of a Power Distribution Network** P.25
Norio Nishizaki, Tadatoshi Sekine, Hideki Asai — Shizuoka University

Poster session I:
Monday, December 10, 2012 — Room 201
13:20-14:00 & 15:40-16:20

P1-1. **Multi-Tone EMC Testing Strategy for RF-Devices** P.89
Alessandro Biondi, Hendrik Rogier, Dries Vande Ginste, Daniël De Zutter — Ghent University
(*Best Poster Paper Award Finalist)

P1-2. **Estimating Radiated Emissions from Microstrip Transmission Lines Based on the Imbalance Model** P.93
Hasan Al-Rubaye, Kuganesan Pararajasingam, Mamadou Kane — Advanced Micro Devices
(*Best Poster Paper Award Finalist)

P1-3. **Parasitic Capacitance Cancellation of Integrated EMI Filter by Splitting Ground Windings** P.97
Hui-Fen Huang, Mao Ye, Shao-Fang Zhang, Yan Zhang — South China University of Technology

P1-4. **Cable Radiation from Common Mode Signals and Differential Mode Signals** P.101
Chung-hao Chen*, Javier Pazos[+], Pujitha Davuluri* — *Intel; [+]University of Texas at El Paso
(*Best Poster Paper Award Finalist)

P1-5. **Common-Mode Noise Reduction Using Floating Conductor in LSI Package** P.105
Tohlu Matsushima*, Yuichi Mabuchi[+], Takashi Hisakado*, Osami Wada* — *Kyoto University; [+]Hitachi, Ltd.

P1-6. **Automated Near-Field EMC/EMI Scanning System with Active Electro-Optical Field Probes** P.109
Sven Kuehn*, Martin Wild[+], Peter Sepan[+], Eugene Grobelaar[+], Niels Kuster* — *IT'IS Foundation, ETH Zurich; [+]Schmid+Partner Engineering AG

Tuesday, December 11, 2012

Howard International House

08:40-09:20 **Keynote Speech: Future Directions for Flip Chip Interconnects**

Mr. Bob Sankman
Director of Package Pathfinding, Assembly Test Technology Development, Intel Corporation, USA

Visionary Hall, 1F

09:20-10:20 **Session C: Design and Modeling for High-speed Channels and Interconnects**

Chairs: Moises Cases, The Cases Group, USA
Lih-Tyng Hwang, National Sun Yat-Sen University, Taiwan

Visionary Hall, 1F

C-1 **Investigation of Optimized High-Density Flip-Chip Interconnect Design including Micro Au Bumps and Underfill for Ultrabroadband (DC-40GHz) Applications** P.33
Yotaro Yasu*+, Fumiki Kato+, Katsuya Kikuchi+, * AIST
Shunsuke Nemoto+, Hiroshi Nakagawa+, Kohji Koshiji*, +Tokyo University of Science
Masahiro Aoyagi*+

C-2 **Taper Pad Design to Improve Electrical Performance of BGAs on Wafer Level Package (WLP)** P.29
Chung-Hao Tsai, Vincent Yeh, TSMC
Chuei-Tang Wang, Doug Yu

C-3 **Bended Differential Transmission Line Using Balanced Model for Common-Mode Noise Suppression** P.37
Chia-Han Chang, National Taiwan University of Science and Technology
Ruei-Ying Fang, Chun-Long Wang

10:20-10:50 **Break**

10:50-12:10 **Session D: 3D ICs**

Chairs: Toshio Sudo, Shibaura Inst. of Technology, Japan
Joungho Kim, KAIST, Korea

Visionary Hall, 1F

D-1 **Consideration of MOS Capacitance Effect in TSV Modeling Based on Cylindrical Modal Basis Functions** P.41
Ki Jin Han*, Ulsan National Institute of Science and Technology
Madhavan Swaminathan[+] [+]Georgia Institute of Technology
(*Best Paper Award Finalist)

D-2 **Noise Coupling Analysis between TSV and Active Circuit** P.45
Manho Lee, Jonghyun Cho, Joungho Kim KAIST
(*Best Paper Award Finalist)

D-3 **A Novel TSV Model Considering Nonlinear MOS Effect for Transient Analysis** P.49
Kuan-Yu Chen, Yi-An Sheu, Chi-Hsuan Cheng, National Taiwan University
Jyun-Hong Lin, Yih-Peng Chiou, Tzong-Lin Wu

D-4 **Electrothermal Modelling of Novel Through-Silicon Carbon Nanotube Bundle Vias (TS-CNTBV)** P.53
Yun-Fan Liu, Zheng Yong, Yan-Song Jiao, Zhejiang University
Wen-Sheng Zhao, Wen-Yan Yin

12:10-14:00 **Lunch**

Garden Cafeteria, 1F

13:20-14:00 **Poster session II** (Detailed program on page XXI)

Room 201, 2F

14:00-15:20 **Session E: Electromagnetic Compatibility (EMC)**
Chairs: Jun Fan, Missouri University of Science and Technology, USA
Wen-Yan Yin, Shanghai Jiao Tong University (SJTU), China
Visionary Hall, 1F

E-1 **Development of Near-Field Emission Limit from Radiated-Emission Limit Based on Statistical Approach** P.57
Kye-Yak See*, Ning Fang**, Lin-Biao Wang[+], *Nanyang Technological University
Weishan Soh*, **Beijing University of Aeronautics and Astronautics
Tengiz Svimonishvili*, [+]Continental
Manish Oswal[++], Weng-Yew Chang[+++], [++]Hewlett Packard
Wee-Jin Koh[+++] [+++]DSO National Laboratories

E-2 **WWAN Solution of NB Display Interface through Silicon-Package-Board Co-Design** P.61
Wei-Da Guo, Sam Yang, Renee Lee, Pengchi Chen, Terry Lin — Himax Technologies, Inc.

E-3 **Electromagnetic Emissions from the IC Packaging** P.65
Nick K. H. Huang[*], Li Jun Jiang*, Huichun Yu[+], Gang Li+, Shuai Xu[+], Tao Wang[++], Huasheng Ren[+]
*The University of Hong Kong
[+]Huawei Technologies Co., LTD
[++]IBM STG

E-4 **Mitigation of Signal Vias to Power Plane Coupling Controlling the Return Current** P.69
Antonio Ciccomancini Scogna[*], Jianmin Zhang[+], LianKheng Teoh[++]
[*]CST
[+]CISCO Systems
[++]EASIC

15:20-16:00 **Break**

15:20-16:00 **Poster session II** (Detailed program on page XXI)

Room 201, 2F

16:00-17:20 **Session F: Signal Integrity**
Chairs: Osami Wada, Kyoto University, Japan
Dries Vande Ginste, Ghent University, Belgium
Visionary Hall, 1F

F-1 **Signal Integrity Improvement in Lossy Transmission Line Using Segmental Transmission Line** P.73
Hiroki Shimada*, Shohei Akita*, Yusuke Kuribara*, Ikuo Yoshihara[+], Moritoshi Yasunaga*
*University of Tsukuba
[+]University of Miyazaki

F-2 **A Novel Design of Three-Tap Passive Equalizer** P.77
Po-Chuan Hsieh, Chien-Hsun Chen, Shou-Kuo Sogo Hsu — Foxconn Technology Group

F-3 **Propagation Characteristics of Differential Transmission Lines in Hybrid-Laminated Materials** P.81
Chun-Lin Liao, Danny Ho, Evelyn Kuo, David Lai — TSTL, IBM

F-4 **Systematic Design and Optimization of Bond Wire Antennas using the M3-Approach** P.85
Ivan Ndip, Stephan Guttowski, Fraunhofer IZM Berlin
Herbert Reichl, Klaus-dieter Lang Technische Universität Berlin

17:20-17:40 Award Ceremony/Closing

Poster session II
Tuesday, December 11, 2012 Room 201
13:20-14:00 & 15:20-16:00

P2-1. **Electrical Characterization of Through-Silicon Vias (TSV) with Different Physical Configurations** P.173
Wen-Sheng Zhao*[+], Yong-Xin Guo[+], Wen-Yan Yin* *Zhejiang University
[+]National University of Singapore

P2-2. **Efficient Algorithm for 3-D Thermal Alternating-Direction-Implicit Method** P.177
Wei Choon Tay, Eng Leong Tan Nanyang Technological University

P2-3. **3D Simulation of Substrate Noise Coupling From Through Silicon Via (TSV) and Noise Isolation Methods** P.181
Leo Jyun-Hong Lin, Hsiao-Pu Chang, National Taiwan University
Tzong-Lin Wu, Yih-Peng Chiou

P2-4. **Analysis and Characterization of PDN Impedance and SSO Noise of 4k-IO 3D SiP** P.185
Hiroki Takatani*, Yosuke Tanaka*, *Shibaura-Institute of Technology
Haruya Fujita*, [+]Association of Super-Advanced Electronics Technologies
Yoshiaki Oizono*, Yoshitaka Nabeshima*,
Toshio Sudo*, Atsushi Sakai[+], Shiro Uchiyama[+], Hiroaki Ikeda[+]

P2-5. **Impact of TSV Induced Thermo-mechanical Stress on Semiconductor Device Performance** P.189
Hui Min Lee*, En-Xiao Liu*, *A*STAR
G. S. Samudra[+], Er-Ping Li* [+]National University of Singapore

P2-6. **Process Variation-Aware Floorplanning for 3D Many-Core Processors** P.193
Hyejeong Hong, Jaeil Lim, Sungho Kang Yonsei University