

# **2012 IEEE Electrical Design of Advanced Packaging and Systems Symposium**

**(EDAPS 2012)**

**Taipei, Taiwan  
9 – 11 December 2012**



**IEEE Catalog Number: CFP12EDP-PRT  
ISBN: 978-1-4673-1444-2**

# Advance Program

## Monday, December 10, 2012

Howard International House

- 08:40-09:00 Opening**  
Visionary Hall, 1F
- 09:00-09:40 Keynote Speech: SiPs making Center Stage**  
Dr. Ho-Ming Tong  
ASE Group, Taiwan  
Visionary Hall, 1F
- 09:40-10:10 Break**
- 10:10-12:15 Special Session in 3D ICs**  
Chairs: Madhavan Swaminathan, Georgia Institute of Technology, USA  
Wei-Chung Lo, Industrial Technology Research Institute, Taiwan  
Visionary Hall, 1F
- S-1 Design and Manufacturing Innovations in Die Stacking (invited) °V °**  
John Y. Xie Altera Corp.
- S-2 (Invited) °V °**  
Dinos Huang ASE Group
- S-3 SI/PI co-integrity design for multi-Gbps interfaces (invited) °V °**  
Woong Hwan Ryu Samsung Electronics Co., Ltd.
- S-4 An Electromagnetic Modeling Tool for 3D Integration Design (invited) °V °**  
Ki Jin Han Ulsan National Institute of Science and Technology
- S-5 The quest for a new dimension of system integration (invited) °V °**  
Sean Lee TSMC
- 12:15-14:00 Lunch**  
Garden Cafeteria, 1F
- 13:20-14:00 Poster session I (Detailed program on page XV )**  
Room 201, 2F
- 14:00-14:40 Keynote Speech: New 3D Integration Technology and Fabrication of Prototype 3D LSIs °V °**  
Prof. Mitsumasa Koyanagi  
New Industry Creation Hatchery Center (NICHe), Tohoku University, Japan  
Visionary Hall, 1F
- 14:40-15:40 Session A: EDA and Testing for 3D IC**  
Chairs: An-Yu Kuo, Cadence, US  
Yi-Chang Lu, National Taiwan University, Taiwan  
Visionary Hall, 1F

- A-1 Effective Resistance Approach for DC Analysis of Power Grid on Through-Silicon Interposer (TSI)** P.1  
En-Xiao Liu, Huapeng Zhao, Zaw Z. Oo, A\*STAR  
Er-Ping Li, Joseph Romen Cubillo  
**(\*Best Paper Award Finalist)**
- A-2 Contactless Wafer-Level TSV Connectivity Testing Method Using Magnetic Coupling** P.5  
Jonghoon J. Kim, Heegon Kim, Sukjin Kim, KAIST  
Changhyun Cho, Daniel H. Jung, Joungho Kim,  
Jun So Pak
- A-3 Bandwidth Enhancement in 3DIC CoWoS™ Test Using Direct Probe Technology** P.9  
Hao Chen, Jian-Ting Chen, Shang-Ju Lee, TSMC  
Ken Chou, Cheng-Bin Chen, Sen-Kuei Hsu,  
Hung-Chih Lin, Ching-Nen Peng, Min-Jer Wang
- 15:40-16:20 Break**
- 15:40-16:20 Poster session I** (Detailed program on page XV)  
Room 201, 2F
- 16:20-17:40 Session B: Power Integrity / Ground Noise**  
Chairs: Hideki Asai, Shizuoka University, Japan  
Dale Becker, IBM, USA  
Visionary Hall, 1F
- B-1 A Linear 4-Element Model of VRM---Characteristics Practical Uses and Limitations** P.13  
Edward Hsin-Kuan Hsiung\*, Ruey-Beei Wu\*, \*National Taiwan University  
Yung-Shou Cheng\*, Kai-Bin Wu\* †Intel  
Yuan-Liang Li†, Thonas Su†
- B-2 On-die PDN Design and Analysis for Minimizing Power Supply Noise** P.17  
Hiroki Otsuka, Genki Kubo, Shibaura Institute of Technology  
Ryota Kobayashi, Tatsuya Mido,  
Yoshinori Kobayashi, Hideyuki Fujii, Toshio Sudo
- B-3 Fast Transient Analysis of Power Distribution Network Modeled by Unstructured Meshes by Using Locally Implicit Latency Insertion Method** P.21  
Shingo Okada, Hiroki Kurobe, Shizuoka University  
Tadatoshi Sekine, Hideki Asai

- B-4 An Explicit and Unconditionally Stable Finite Difference Scheme for the Fast Transient Analysis of a Power Distribution Network** P.25  
Norio Nishizaki, Tadatoshi Sekine, Hideki Asai Shizuoka University

**Poster session I:**

Monday, December 10, 2012 Room 201

13:20-14:00 & 15:40-16:20

- P1-1. Multi-Tone EMC Testing Strategy for RF-Devices** P.89  
Alessandro Biondi, Hendrik Rogier, Ghent University  
Dries Vande Ginste, Daniël De Zutter  
**(\*Best Poster Paper Award Finalist)**
- P1-2. Estimating Radiated Emissions from Microstrip Transmission Lines Based on the Imbalance Model** P.93  
Hasan Al-Rubaye, Kuganesan Pararajasingam, Advanced Micro Devices  
Mamadou Kane  
**(\*Best Poster Paper Award Finalist)**
- P1-3. Parasitic Capacitance Cancellation of Integrated EMI Filter by Splitting Ground Windings** P.97  
Hui-Fen Huang, Mao Ye, Shao-Fang Zhang, South China University of Technology  
Yan Zhang
- P1-4. Cable Radiation from Common Mode Signals and Differential Mode Signals** P.101  
Chung-hao Chen\*, Javier Pazos<sup>+</sup>, Pujitha Davuluri\* \*Intel  
<sup>+</sup>University of Texas at El Paso  
**(\*Best Poster Paper Award Finalist)**
- P1-5. Common-Mode Noise Reduction Using Floating Conductor in LSI Package** P.105  
Tohlu Matsushima\*, Yuichi Mabuchi<sup>+</sup>, \*Kyoto University  
Takashi Hisakado\*, Osami Wada\* <sup>+</sup>Hitachi, Ltd.
- P1-6. Automated Near-Field EMC/EMI Scanning System with Active Electro-Optical Field Probes** P.109  
Sven Kuehn\*, Martin Wild<sup>+</sup>, Peter Sepan<sup>+</sup>, \*IT'IS Foundation, ETH Zurich  
Eugene Grobelaar<sup>+</sup>, Niels Kuster\* <sup>+</sup>Schmid+Partner Engineering AG

- P1-7. **Chip-Package-PCB Co-Design: Dealing with Harmonic Desensitization in RF SoC/SiP** P.113  
Fu-Yi Han, Wen Zhou Wu, Herbert Lee, Mediatek Inc.  
Tony Hsieh, Tina Tang, Nan-Cheng Chen
- P1-8. **Chip-Package-PCB Co-Design for Optimization of Wireless Receiver Performance** P.116  
Ruey-Bo Sun, Po-Yang Chang, Mstar Semiconductor  
Ting-Kuang Wang, Chih-Ming Hung
- P1-9. **Ferrite Layer and High Dielectric Constant BaTiO<sub>3</sub> for Power Integrity** P.120  
Huifen Huang, Shaofang Zhang South China University of Technology
- P1-10. **Efficacy of Port and Lane Staggering in reducing IO Power Supply Noise** P.123  
Srinivasan Govindan, Srikrishnan Venkataraman Intel Technology India Private Limited  
**(\*Best Poster Paper Award Finalist)**
- P1-11. **Anti-Resonance Peak Damping of PDN Impedance by On-board Snubber Circuits** P.127  
You Iijima, Masataka Matsumura and Toshio Sudo Shibaura Institute of Technology
- P1-12. **Fast Crosstalk Analysis of Multi-Walled Carbon Nanotube Interconnects** P.131  
Jiaqing Lu, Min Tang, and Junfa Mao Shanghai Jiao Tong University
- P1-13. **Crosstalk-noise Reduction Using Segmental Transmission Line** P.135  
Katsuyuki Seki, Hiroki Shimada, Moritoshi Yasunaga University of Tsukuba
- P1-14. **The Improvement of Signal Quality and Far-End Crosstalk for Coupled Microstrip Line  
Over a Completely Split Ground Plane** P.139  
Ding-Bing Lin, Ruei-Hua Shen National Taipei University of Technology
- P1-15. **Stepped Guard Trace with the Fewest Shorting-Vias to Eliminate the Ringing Noise of  
Coupled Microstrip Lines** P.142  
Ding-Bing Lin\*, Chen-Kuang Wang\*, \*National Taipei University of Technology  
Jui-Hung Chou<sup>+</sup> <sup>+</sup>National Taiwan University
- P1-16. **A Case Study of High-Speed Serial Interface Simulation With IBIS-AMI Models** P.145  
Anil Lingambudi, Greg Edlund, Anand Haridass, Dale Becker IBM

- P1-17. **Influence of Via Stubs with Different Terminations on Time-Domain Transmission Waveform and Eye Diagram in Multilayer PCBs** P.149  
Chi-Lou Yeh\*, Yi-Chin Tsai\*, Che-Ming Hsu\*, \*Chung Yuan Christian University  
Li-Sang Liu<sup>†</sup>, Sheng- Hsun Tsai<sup>†</sup>, Yu Han Kao\*, <sup>†</sup>MiTAC International Corporation  
Guang-Hwa Shiue\*
- P1-18. **A Novel Flexible Printed Circuit Structure for Gigabit Data Transmission** P.153  
Shou-Kuo Sogo Hsu\*, Yu-Chang Pai<sup>†</sup>, \*Foxconn Technology Group  
Po-Chuan Hsieh\* <sup>†</sup>Novatek Microelectronics Corp.
- P1-19. **Enhancement of the Multi-Module Memory Bus for Signal Integrity by Using Genetic Algorithm** P.157  
Chun-Te Wu\*, Ding-Bing Lin<sup>†</sup> \*Dayeh University  
<sup>†</sup>National Taipei University of Technology
- P1-20. **System Development of High-Performance, Low-Cost 1333Mbps LPDDR2 Memory Interface** P.161  
Chung-Hwa Wu, Delbert Liao, Mizar Chang, Mediatek Inc.  
Chaowei Tseng, Herbert Lee, Nan-Cheng Chen
- P1-21. **Disconnection Failure Model and Analysis of TSV-based 3D ICs** P.164  
Daniel H. Jung, Joohee Kim, Heegon Kim, KAIST  
Jonghoon J. Kim, Joungho Kim, Jun So Pak  
**(\*Best Poster Paper Award Finalist)**
- P1-22. **Scalable Modeling of Through Silicon Vias Up to Millimeter-Wave Frequency** P.168  
Kuan-Chung Lu\*, Tzyy-Sheng Horng\*, \*National Sun Yat-Sen University  
Chi-Han Chen<sup>†</sup>, Chang-Ying Hung<sup>†</sup>, <sup>†</sup>Advanced Semiconductor Engineering Inc.  
Pao-Nan Lee<sup>†</sup>, Meng-Jen Wang<sup>†</sup>,  
Chih-Pin Hung<sup>†</sup>, Ho-Ming Tong\*  
**(\*Best Poster Paper Award Finalist)**

Tuesday, December 11, 2012

Howard International House

- 08:40-09:20 Keynote Speech: Future Directions for Flip Chip Interconnects** P.33  
Mr. Bob Sankman  
Director of Package Pathfinding, Assembly Test Technology Development, Intel Corporation, USA  
Visionary Hall, 1F
- 09:20-10:20 Session C: Design and Modeling for High-speed Channels and Interconnects** P.33  
Chairs: Moises Cases, The Cases Group, USA  
Lih-Tyng Hwang, National Sun Yat-Sen University, Taiwan  
Visionary Hall, 1F
- C-1 Investigation of Optimized High-Density Flip-Chip Interconnect Design including Micro Au Bumps and Underfill for Ultrabroadband (DC-40GHz) Applications** P.33  
Yotaro Yasu<sup>\*,+</sup>, Fumiki Kato<sup>+</sup>, Katsuya Kikuchi<sup>+</sup>, \* AIST  
Shunsuke Nemoto<sup>+</sup>, Hiroshi Nakagawa<sup>+</sup>, Kohji Koshiji<sup>\*</sup>, <sup>+</sup>Tokyo University of Science  
Masahiro Aoyagi<sup>\*,+</sup>
- C-2 Taper Pad Design to Improve Electrical Performance of BGAs on Wafer Level Package (WLP)** P.29  
Chung-Hao Tsai, Vincent Yeh, TSMC  
Chuei-Tang Wang, Doug Yu
- C-3 Bended Differential Transmission Line Using Balanced Model for Common-Mode Noise Suppression** P.37  
Chia-Han Chang, National Taiwan University of Science and Technology  
Ruei-Ying Fang, Chun-Long Wang
- 10:20-10:50 Break**
- 10:50-12:10 Session D: 3D ICs**  
Chairs: Toshio Sudo, Shibaura Inst. of Technology, Japan  
Joungho Kim, KAIST, Korea  
Visionary Hall, 1F

- D-1 Consideration of MOS Capacitance Effect in TSV Modeling Based on Cylindrical Modal Basis Functions** P.41  
Ki Jin Han\*, Ulsan National Institute of Science and Technology  
Madhavan Swaminathan<sup>†</sup> <sup>†</sup>Georgia Institute of Technology  
**(\*Best Paper Award Finalist)**
- D-2 Noise Coupling Analysis between TSV and Active Circuit** P.45  
Manho Lee, Jonghyun Cho, Joungho Kim KAIST  
**(\*Best Paper Award Finalist)**
- D-3 A Novel TSV Model Considering Nonlinear MOS Effect for Transient Analysis** P.49  
Kuan-Yu Chen, Yi-An Sheu, Chi-Hsuan Cheng, National Taiwan University  
Jyun-Hong Lin, Yih-Peng Chiou, Tzong-Lin Wu
- D-4 Electrothermal Modelling of Novel Through-Silicon Carbon Nanotube Bundle Vias (TS-CNTBV)** P.53  
Yun-Fan Liu, Zheng Yong, Yan-Song Jiao, Zhejiang University  
Wen-Sheng Zhao, Wen-Yan Yin
- 12:10-14:00 Lunch**  
Garden Cafeteria, 1F
- 13:20-14:00 Poster session II** (Detailed program on page XXI)  
Room 201, 2F
- 14:00-15:20 Session E: Electromagnetic Compatibility (EMC)**  
Chairs: Jun Fan, Missouri University of Science and Technology, USA  
Wen-Yan Yin, Shanghai Jiao Tong University (SJTU), China  
Visionary Hall, 1F
- E-1 Development of Near-Field Emission Limit from Radiated-Emission Limit Based on Statistical Approach** P.57  
Kye-Yak See\*, Ning Fang\*\*, Lin-Biao Wang<sup>†</sup>, <sup>†</sup>Nanyang Technological University  
Weishan Soh\*, <sup>\*\*</sup>Beijing University of Aeronautics and Astronautics  
Tengiz Svimonishvili\*, <sup>†</sup>Continental  
Manish Oswal<sup>††</sup>, Weng-Yew Chang<sup>†††</sup>, <sup>††</sup>Hewlett Packard  
Wee-Jin Koh<sup>†††</sup> <sup>†††</sup>DSO National Laboratories



- E-2 WWAN Solution of NB Display Interface through Silicon-Package-Board**  
**Co-Design** P.61  
Wei-Da Guo, Sam Yang, Renee Lee, Himax Technologies, Inc.  
Pengchi Chen, Terry Lin
- E-3 Electromagnetic Emissions from the IC Packaging** P.65  
Nick K. H. Huang\*, Li Jun Jiang\*, Huichun Yu+, \*The University of Hong Kong  
Gang Li+, Shuai Xu+, Tao Wang\*\*, Huasheng Ren+ +Huawei Technologies Co., LTD  
\*\*IBM STG
- E-4 Mitigation of Signal Vias to Power Plane Coupling Controlling the Return**  
**Current** P.69  
Antonio Ciccomancini Scogna\*, \*CST  
Jianmin Zhang+, +CISCO Systems  
LianKheng Teoh\*\* \*\*EASIC
- 15:20-16:00 Break**
- 15:20-16:00 Poster session II** (Detailed program on page XXI)  
Room 201, 2F
- 16:00-17:20 Session F: Signal Integrity**  
Chairs: Osami Wada, Kyoto University, Japan  
Dries Vande Ginste, Ghent University, Belgium  
Visionary Hall, 1F
- F-1 Signal Integrity Improvement in Lossy Transmission Line Using Segmental**  
**Transmission Line** P.73  
Hiroki Shimada\*, Shohei Akita\*, Yusuke Kuribara\*, \*University of Tsukuba  
Ikko Yoshihara+, Moritoshi Yasunaga\* +University of Miyazaki
- F-2 A Novel Design of Three-Tap Passive Equalizer** P.77  
Po-Chuan Hsieh, Chien-Hsun Chen, Foxconn Technology Group  
Shou-Kuo Sogo Hsu
- F-3 Propagation Characteristics of Differential Transmission Lines in Hybrid-Laminated**  
**Materials** P.81  
Chun-Lin Liao, Danny Ho, Evelyn Kuo, David Lai TSTL, IBM

- F-4 Systematic Design and Optimization of Bond Wire Antennas using the M3-Approach** P.85  
Ivan Ndip, Stephan Guttowski, Fraunhofer IZM Berlin  
Herbert Reichl, Klaus-dieter Lang Technische Universität Berlin

**17:20-17:40 Award Ceremony/Closing**

**Poster session II**

Tuesday, December 11, 2012 Room 201

13:20-14:00 & 15:20-16:00

- P2-1. Electrical Characterization of Through-Silicon Vias (TSV) with Different Physical Configurations** P.173  
Wen-Sheng Zhao<sup>\*,+</sup>, Yong-Xin Guo<sup>+</sup>, Wen-Yan Yin<sup>\*</sup> \*Zhejiang University  
<sup>+</sup>National University of Singapore
- P2-2. Efficient Algorithm for 3-D Thermal Alternating-Direction-Implicit Method** P.177  
Wei Choon Tay, Eng Leong Tan Nanyang Technological University
- P2-3. 3D Simulation of Substrate Noise Coupling From Through Silicon Via (TSV) and Noise Isolation Methods** P.181  
Leo Jyun-Hong Lin, Hsiao-Pu Chang, National Taiwan University  
Tzong-Lin Wu, Yih-Peng Chiou
- P2-4. Analysis and Characterization of PDN Impedance and SSO Noise of 4k-IO 3D SiP** P.185  
Hiroki Takatani<sup>\*</sup>, Yosuke Tanaka<sup>\*</sup>, \*Shibaura-Institute of Technology  
Haruya Fujita<sup>\*</sup>, <sup>+</sup>Association of Super-Advanced Electronics Technologies  
Yoshiaki Oizono<sup>\*</sup>, Yoshitaka Nabeshima<sup>\*</sup>,  
Toshio Sudo<sup>\*</sup>, Atsushi Sakai<sup>+</sup>, Shiro Uchiyama<sup>+</sup>, Hiroaki Ikeda<sup>+</sup>
- P2-5. Impact of TSV Induced Thermo-mechanical Stress on Semiconductor Device Performance** P.189  
Hui Min Lee<sup>\*</sup>, En-Xiao Liu<sup>\*</sup>, \*A\*STAR  
G. S. Samudra<sup>+</sup>, Er-Ping Li<sup>\*</sup> <sup>+</sup>National University of Singapore
- P2-6. Process Variation-Aware Floorplanning for 3D Many-Core Processors** P.193  
Hyejeong Hong, Jaeil Lim, Sungho Kang Yonsei University

- P2-7. **Design Considerations for Radio Frequency 3DICs** P.197  
Ying-Cheng Tseng, Chang-Bao Chang, National Taiwan University  
Chin-Khai Tang, Chi-Hsuan Cheng, Yi-Chang Lu,  
Kun-You Lin, Tzong-Lin Wu, Ruey-Beei Wu
- P2-8. **The Effects of NBTI on 3D Integrated Circuits** P.201  
Cheng-Hong Lin<sup>\*+</sup>, Yi-Chang Lu<sup>\*</sup>, \*National Taiwan University  
Chin-Khai Tang<sup>\*</sup>, Kuen-Yu Tsai<sup>\*</sup> <sup>+</sup>SpringSoft Inc.
- P2-9. **Generalized Complex Inductance for Microstrip Radiation Problems** P.205  
Lap K. Yeung, Ke-Li Wu The Chinese University of HK
- P2-10. **An Efficient Dipole Array Model for the Accurate Prediction of Antennas Radiation Pattern** P.208  
Fang-Pin Xiang, Xing-Chang Wei, and Er-Ping Li Zhejiang University
- P2-11. **A Physically Concise Circuit Model for Electrically Small Structures** P.212  
Lap K. Yeung and Ke-Li Wu The Chinese University of HK
- P2-12. **Chip-Package-PCB Thermal Co-Design for Hot Spot Analysis in SoC** P.215  
Kidd Chen, Ian Hsu, Chungfa Lee Mediatek Inc.
- P2-13. **Slow-Wave Structure to Suppress Differential-to-Common Mode Conversion for Bend Discontinuity of Differential Signaling** P.219  
Lin-Sheng Wu<sup>\*</sup>, Jun-Fa Mao<sup>\*</sup>, Wen-Yan Yin<sup>+</sup> \*Shanghai Jiao Tong University  
<sup>+</sup>Zhejiang University
- P2-14. **Crosstalk Analysis of Multigigabit Links on High Density Interconnects PCB using IBIS AMI Models** P.223  
C. Chastang<sup>\*</sup>, C. Gautier<sup>+</sup>, \*THALES Communications & Security  
A. Amedeo<sup>\*</sup>, F. Costa<sup>+</sup> <sup>+</sup>SATIE CNRS, ENS Cachan
- P2-15. **Signal Integrity Analysis of Graphene Nano-Ribbon (GNR) Interconnects** P.227  
Wen-Sheng Zhao, Wen-Yan Yin Zhejiang University

- P2-16. **The gas microconcentrators in LTCC and MEMS technology for acetone breath analysis** P.231  
Artur Rydosz, Wojciech Maziarz, AGH University of Science and Technology  
Tadeusz Pisarkiewicz, Sławomir Gruszczyński,  
Krzysztof Wincza
- P2-17. **The Database of Embedded Passives for RF-SiP Design** P.235  
Hsun Yu, Wei-Ting Chen, Wei Li, Industrial Technology Research Institute  
Chang-Sheng Chen, Ra-Min Tain, Cheng-Hua Tsai,  
Meng-Sheng Chen, Chang-Chih Liu, Li-Chi Chang,  
Chin-Sun Shyu, Shinn-Juh Lai and Min-Lin Lee
- P2-18. **Optimized Inverter Design of Ring Oscillator based Wafer-Level TSV Connectivity Test (RO-TSV-CT)** P.239  
Jun So Pak\*, Joohee Kim\*, Daniel H. Jung\*, \*KAIST  
Junho Lee<sup>+</sup>, Kunwoo Park<sup>+</sup>, Joungho Kim\* <sup>+</sup>SK Hynix Semiconductor Inc.
- P2-19. **Design and Characterization of Magnetically Coupled On-Chip Current Probe for Monitoring Switching Current in Chip I/O PDN** P.243  
Changhyun Cho, Jonghoon J. Kim, Joungho Kim, Jun So Pak KAIST