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The 18th Asia and South Pacific Design Automation Conference
Technical Program

List of Papers

Remark: The presenter of each paper is marked with "*".

Session 1K Opening & Keynote I
Time: 8:30 - 10:00 Wednesday, January 23, 2013
Chair: Shinji Kimura (Waseda Univ., Japan)

1K-1 (Time: 8:30 - 10:00)

(Keynote Address) From Circuits to Cancer

*Sani Nassif (IBM, U.S.A.)

Session 1A Special Session: Advanced Modeling and Simulation Techniques for Power/Signal Integrity in 3D Design
Time: 10:20 - 12:20 Wednesday, January 23, 2013
Organizer: Hideki Asai (Shizuoka Univ., Japan)

1A-1 (Time: 10:20 - 10:50)

(Invited Paper) Equivalent Circuit Model Extraction for Interconnects in 3D ICs

*A. Ege Engin (San Diego State Univ., U.S.A.)

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1A-2 (Time: 10:50 - 11:20)

(Invited Paper) Unconditionally Stable Explicit Method for the Fast 3-D Simulation of On-Chip Power Distribution Network with Through Silicon Via

*Tadatoshi Sekine, Hideki Asai (Shizuoka Univ., Japan)

pp. 7 - 12

1A-3 (Time: 11:20 - 11:50)

(Invited Paper) Signal Integrity Modeling and Measurement of TSV in 3D IC

*Joungho Kim, Joungho Kim (KAIST, Republic of Korea)

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1A-4 (Time: 11:50 - 12:20)

(Invited Paper) Power Distribution Network Modeling for 3-D ICs with TSV Arrays

Chi-Kai Shen, Yi-Chang Lu, Yih-Peng Chiou, Tai-Yu Cheng, *Tzong-Lin Wu (National Taiwan Univ., Taiwan)

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Session 1B Disruptive NoCs for Next-Generation MPSoCs

Time: 10:20 - 12:20 Wednesday, January 23, 2013

Chairs: Sri Parameswaran (Univ. of New South Wales, Australia), Chung-Ta King (National Tsing Hua Univ., Taiwan)

1B-1 (Time: 10:20 - 10:50)

A Case for Wireless 3D NoCs for CMPs

*Hiroki Matsutani (Keio Univ., Japan), Paul Bogdan, Radu Marculescu (Carnegie Mellon Univ., U.S.A.), Yasuhiro Take, Daisuke Sasaki, Hao Zhang (Keio Univ., Japan), Michihiro Koibuchi (NII, Japan), Tadahiro Kuroda, Hideharu Amano (Keio Univ., Japan)

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1B-2 (Time: 10:50 - 11:20)

Deflection Routing in 3D Network-on-Chip with TSV Serialization

*Jinho Lee, Dongwoo Lee, Sunwook Kim, Kiyoung Choi (Seoul National Univ., Republic of Korea)

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1B-3 (Time: 11:20 - 11:50)

Title MD: Minimal Path-based Approach for Fault-Tolerant Routing in On-Chip Networks

Author Masoumeh Ebrahimi, Masoud Daneshtalab, Juha Plosila (Univ. of Turku, Finland), *Farhad Mehdipour (Kyushu Univ., Japan)

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1B-4 (Time: 11:50 - 12:20)

Title A Dynamic Stream Link for Efficient Data Flow Control in NoC Based Heterogeneous MPSoC

Author Claude Helmstetter, Sylvain Basset, *Romain Lemaire (CEA-Leti, Minatec Campus, France), Michel Langevin, Chuck Pilkington (STMicroelectronics, Ottawa, Canada), Fabien Clermidy (CEA-Leti, Minatec Campus, France), Pierre Paulin (STMicroelectronics, Ottawa, Canada), Pascal Vivet (CEA-Leti, Minatec Campus, France), Didier Fuin (STMicroelectronics, Grenoble, France)

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Session 1C Embedded Systems

Time: 10:20 - 12:20 Wednesday, January 23, 2013

Chairs: Hiroyuki Tomiyama (Ritsumeikan Univ., Japan), Tohru Ishihara (Kyoto Univ., Japan)

1C-1 (Time: 10:20 - 10:50)

Title On Real-Time STM Concurrency Control for Embedded Software with Improved Schedulability

Author *Mohammed Elshambakey, Binoy Ravindran (ECE Dept, Virginia Tech, U.S.A.)

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1C-2 (Time: 10:50 - 11:20)

Title Schedule Integration for Time-Triggered Systems

Author *Florian Sagstetter, Martin Lukasiewycz (TUM CREATE, Singapore), Samarjit Chakraborty (TU Munich, Germany)

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1C-3 (Time: 11:20 - 11:50)

Title: Online Estimation of the Remaining Energy Capacity in Mobile Systems Considering System-Wide Power Consumption and Battery Characteristics

Author: Donghwa Shin (Seoul National Univ., Republic of Korea), Woojoo Lee (Univ. of Southern California, U.S.A.), Kitae Kim
Yanzhi Wang, Qing Xie (Univ. of Southern California, U.S.A.), *Naehyuck Chang (Seoul National Univ., Republic of Korea), Massoud Pedram (Univ. of Southern California, U.S.A.)

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1C-4 (Time: 11:50 - 12:20)

Title: WUCC: Joint WCET and Update Conscious Compilation for Cyber-physical Systems

Author: Yazhi Huang, Mengying Zhao, *Chun Jason Xue (City Univ. of Hong Kong, Hong Kong)

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Session 1D University Design Contest

Time: 10:20 - 12:20 Wednesday, January 23, 2013

Chairs: Hiroshi Kawaguchi (Kobe Univ., Japan), Tetsuo Hironaka (Hiroshima City Univ., Japan)

1D-1 (Time: 10:20 - 10:25)

Title: A 40-nm 144-mW VLSI Processor for Real-time 60-kWord Continuous Speech Recognition

Author: *Guangji He, Takanobu Sugahara, Tsuyoshi Fujinaga, Yuki Miyamoto, Hiroki Noguchi, Shintaro Izumi, Hiroshi Kawaguchi, Masahiko Yoshimoto (Kobe Univ., Japan)

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1D-2 (Time: 10:25 - 10:30)

Title: A 24.5-53.6pJ/pixel 4320p 60fps H.264/AVC Intra-Frame Video Encoder Chip in 65nm CMOS

Author: *Dajiang Zhou, Gang He, Wei Fei, Zhixiang Chen, Jinjia Zhou, Satoshi Goto (Waseda Univ., Japan)

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1D-3 (Time: 10:30 - 10:35)

Title A Low Power Multimedia Processor Implementing Dynamic Voltage and Frequency Scaling Technique

Author Tadayoshi Enomoto, *Nobuaki Kobayashi (Chuo Univ., Japan)

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1D-4 (Time: 10:35 - 10:40)

Title A 40-nm 0.5-V 12.9-pJ/Access 8T SRAM Using Low-Power Disturb Mitigation Technique

Author *Shusuke Yoshimoto, Masaharu Terada, Shunsuke Okumura (Kobe Univ., Japan), Toshikazu Suzuki (Panasonic Corp., Japan), Shinji Miyano (STARC, Japan), Hiroshi Kawaguchi, Masahiko Yoshimoto (Kobe Univ., Japan)

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1D-5 (Time: 10:40 - 10:45)

Title A Physical Unclonable Function Chip Exploiting Load Transistors' Variation in SRAM Bitcells

Author *Shunsuke Okumura, Shusuke Yoshimoto, Hiroshi Kawaguchi (Kobe Univ., Japan), Masahiko Yoshimoto (Kobe Univ./JST CREST, Japan)

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1D-6 (Time: 10:45 - 10:50)

Title Over 10-Times High-speed, Energy Efficient 3D TSV-Integrated Hybrid ReRAM/MLC NAND SSD by Intelligent Data Fragmentation Suppression

Author *Chao Sun (Chuo Univ./Univ. of Tokyo, Japan), Hiroki Fujii (Univ. of Tokyo, Japan), Kousuke Miyaji, Koh Johguchi (Chuo Univ., Japan), Kazuhide Higuchi (Univ. of Tokyo, Japan), Ken Takeuchi (Chuo Univ., Japan)

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1D-7 (Time: 10:50 - 10:55)

Title Highly Reliable Solid-State Drives (SSDs) with Error-Prediction LDPC (EP-LDPC) Architecture and Error-Recovery Scheme

Author *Shuhei Tanakamaru, Yuki Yanagihara (Univ. of Tokyo, Japan), Ken Takeuchi

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1D-8 (Time: 10:55 - 11:00)

Title A 3Gb/s 2.08mm^2 100b Error-Correcting BCH Decoder in 0.13µm CMOS Process

Author *Youngjoo Lee, Hoyoung Yoo, In-Cheol Park (KAIST, Republic of Korea)

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1D-9 (Time: 11:00 - 11:05)

Title A 6.72-Gb/s, 8pJ/bit/iteration WPAN LDPC Decoder in 65nm CMOS

Author *Zhixiang Chen, Xiao Peng, Xiongxin Zhao, Leona Okamura, Dajiang Zhou, Satoshi Goto (Waseda Univ., Japan)

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1D-10 (Time: 11:05 - 11:10)

Title A 7.5Gb/s Referenceless Transceiver for UHDTV with Adaptive Equalization and Bandwidth Scanning Technique in 0.13um CMOS Process

Author *Junyoung Song (Korea Univ., Republic of Korea), Hyunwoo Lee (Hynix Inc., Republic of Korea), Sewook Hwang (Korea Univ., Republic of Korea), Inhwa Jung (Hynix Inc., Republic of Korea), Chulwoo Kim (Korea Univ., Republic of Korea)

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1D-11 (Time: 11:10 - 11:15)

Title A 12.5 Gb/s/Link Non-Contact Multi Drop Bus System with Impedance-Matched Transmission Line Couplers and Dicode Partial-Response Channel Transceivers

Author *Atsutake Kosuge, Wataru Mizuhara, Noriyuki Miura, Masao Taguchi, Hiroki Ishikuro, Tadahiro Kuroda (Keio Univ., Japan)

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1D-12 (Time: 11:15 - 11:20)

Title 315MHz OOK Transceiver with 38-µW Receiver and 36-µW Transmitter in 40-nm CMOS

Author *Shunta Iguchi (Univ. of Tokyo, Japan), Akira Saito (STARC, Japan), Kentaro Honda, Yunfei Zheng (Univ. of Tokyo, Japan), Kazunori Watanabe (STARC, Japan), Takayasu Sakurai, Makoto Takamiya (Univ. of Tokyo, Japan)

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1D-13 (Time: 11:20 - 11:25)

Title A Full 4-Channel 60GHz Direct-Conversion Transceiver

Author *Seitaro Kawai, Ryo Minami, Ahmed Musa, Takahiro Sato, Ning Li, Tatsuya Yamaguchi, Yasuaki Takeuchi, Yuki Tsukui, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan)

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1D-14 (Time: 11:25 - 11:30)

Title A Sub-harmonic Injection-locked Frequency Synthesizer with Frequency Calibration Scheme for Use in 60GHz TDD Transceivers

Author *Teerachot Siriburanon, Wei Deng, Ahmed Musa, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan)

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1D-15 (Time: 11:30 - 11:35)

Title A Fractional-N Harmonic Injection-locked Frequency Synthesizer with 10MHz-6.6GHz Quadrature Outputs for Software-Defined Radios

Author *Wei Deng, Ahmed Musa, Kenichi Okada, Akira Matsuzawa (Tokyo Inst. of Tech., Japan)

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1D-16 (Time: 11:35 - 11:40)

Title A Ring-VCO-Based Sub-Sampling PLL CMOS Circuit with 0.73 ps Jitter and 20.4 mW Power Consumption

Author *Kenta Sogo, Akihiro Toya, Takamaro Kikkawa (Hiroshima Univ., Japan)

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1D-17 (Time: 11:40 - 11:45)

Title Design of a Clock Jitter Reduction Circuit Using Gated Phase Blending Between Self-Delayed Clock Edges

Author *Kiichi Niitsu, Naohiro Harigai, Daiki Hirabayashi, Daiki Oki, Masato Sakurai (Gunma Univ., Japan), Osamu Kobayashi (STARC, Japan), Takahiro J. Yamaguchi, Haruo Kobayashi (Gunma Univ., Japan)

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1D-18 (Time: 11:45 - 11:50)

Title A 25-Gb/s LD Driver with Area-Effective Inductor in a 0.18-µm CMOS

Author *Takeshi Kuboki (Kyoto Univ., Japan), Yusuke Ohtomo (NTT, Japan), Akira Tsuchiya (Kyoto Univ., Japan), Keiji Kishine (Univ. of Shiga Prefecture, Japan), Hidetoshi Onodera (Kyoto Univ., Japan)

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1D-19 (Time: 11:50 - 11:55)

Title A Regulated Charge Pump with Low-Power Integrated Optimum Power Point Tracking Algorithm for Indoor Solar Energy Harvesting

Author *Jungmoon Kim, Chulwoo Kim (Korea Univ., Republic of Korea)

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1D-20 (Time: 11:55 - 12:00)

Title A Low Voltage Buck DC-DC Converter Using On-Chip Gate Boost Technique in 40nm CMOS

Author *Xin Zhang, Po-Hung Chen (Univ. of Tokyo, Japan), Yoshikatsu Ryu (STARC, Japan), Koichi Ishida (Univ. of Tokyo, Japan), Yasuyuki Okuma, Kazunori Watanabe (STARC, Japan), Takayasu Sakurai, Makoto Takamiya (Univ. of Tokyo, Japan)

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1D-21 (Time: 12:00 - 12:05)

Title A 0.35-0.8V 8b 0.5-35MS/s 2bit/step Extremely-low Power SAR ADC

Author *Kentaro Yoshioka, Akira Shikata, Ryota Sekimoto, Tadahiro Kuroda, Hiroki Ishikuro (Keio Univ., Japan)

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Session 2A Special Session: Dependability of on-Chip Systems

Time: 13:40 - 15:40 Wednesday, January 23, 2013
Organizer: Jörg Henkel (Karlsruhe Inst. of Tech., Germany)

2A-1 (Time: 13:40 - 14:20)

Title (Invited Paper) Thermal Management for Dependable on-chip Systems

Author *Jörg Henkel, Thomas Ebi, Hussam Amrouch, Heba Khdr (Karlsruhe Inst. of Tech., Germany)

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2A-2 (Time: 14:20 - 15:00)

Title (Invited Paper) Dependable VLSI Platform using Robust Fabrics

Author *Hidetoshi Onodera (Kyoto Univ., Japan)

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2A-3 (Time: 15:00 - 15:40)

Title (Invited Paper) Variability-Aware Memory Management for Nanoscale Computing

Author *Nikil Dutt (Univ. of California, Irvine, U.S.A.), Puneet Gupta (Univ. of California, Los Angeles, U.S.A.), Alex Nicolau, Luis Angel D. Bathen (Univ. of California, Irvine, U.S.A.), Mark Gottscho (Univ. of California, Los Angeles, U.S.A.)

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Session 2B Logic Synthesis

Time: 13:40 - 15:40 Wednesday, January 23, 2013
Chairs: Yuko Hara-Azumi (NAIST, Japan), Shigeru Yamashita (Ritsumeikan Univ., Japan)

2B-1 (Time: 13:40 - 14:10)

Title MIXSyn: An Efficient Logic Synthesis Methodology for Mixed XOR-AND/OR Dominated Circuits

Author *Luca Amarú, Pierre-Emmanuel Gaillardon, Giovanni De Micheli (Ecole Polytechnique Federale de Lausanne, Switzerland)

Page pp. 133 - 138

2B-2 (Time: 14:10 - 14:40)

Title Optimizing Multi-level Combinational Circuits for Generating Random Bits

Author Chen Wang, *Weikang Qian (Shanghai Jiao Tong Univ., China)

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2B-3 (Time: 14:40 - 15:10)

Title Improving the Mapping of Reversible Circuits to Quantum Circuits Using Multiple Target Lines

Author *Robert Wille, Mathias Soeken, Christian Otterstedt, Rolf Drechsler (Univ. of Bremen, Germany)

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Session 2C Simulation for Thermal and Power Grid Analysis
Time: 13:40 - 15:40 Wednesday, January 23, 2013
Chair: Youngsoo Shin (KAIST, Republic of Korea)

2C-1 (Time: 13:40 - 14:10)

Title I-LUTSim: An Iterative Look-Up Table Based Thermal Simulator for 3-D ICs

Author *Chi-Wen Pan, Yu-Min Lee (National Chiao Tung Univ., Taiwan), Pei-Yu Huang (ITRI, Taiwan), Chi-Ping Yang (National Chiao Tung Univ., Taiwan), Chang-Tzu Lin, Chia-Hsin Lee, Yung-Fa Chou, Ding-Ming Kwai (ITRI, Taiwan)

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2C-2 (Time: 14:10 - 14:40)

Title Compact Nonlinear Thermal Modeling of Packaged Integrated Systems

Author *Zao Liu, Sheldon X.-D. Tan, Hai Wang (Univ. of California, Riverside, U.S.A.), Ashish Gupta (Intel Corp., U.S.A.), Sahana Swarup (Univ. of California, Riverside, U.S.A.)

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2C-3 (Time: 14:40 - 15:10)

Title A Multilevel H-matrix-based Approximate Matrix Inversion Algorithm for

Vectorless Power Grid Verification

Author Wei Zhao, Yici Cai, *Jianlei Yang (Tsinghua Univ., China)

Page pp. 163 - 168

2C-4 (Time: 15:10 - 15:40)

Title Realization of Frequency-Domain Circuit Analysis Through Random Walk

Author Tetsuro Miyakawa, Hiroshi Tsutsui, Hiroyuki Ochi, *Takashi Sato (Kyoto Univ., Japan)

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Session 2D Advanced Routing Techniques for Chip and PCB Design

Time: 13:40 - 15:40 Wednesday, January 23, 2013

Chairs: Toshiyuki Shibuya (Fujitsu Laboratory, Japan), Jai-Ming Lin (National Cheng Kung Univ., Taiwan)

2D-1 (Time: 13:40 - 14:10)

Title A Separation and Minimum Wire Length Constrained Maze Routing Algorithm under Nanometer Wiring Rules

Author *Fong-Yuan Chang, Ren-Song Tsay, Wai-Kei Mak (National Tsing Hua Univ., Taiwan), Sheng-Hsiung Chen (Springsoft, Taiwan)

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2D-2 (Time: 14:10 - 14:40)

Title An ILP-based Automatic Bus Planner for Dense PCBs

Author Pei-Ci Wu (Univ. of Illinois, Urbana-Champaign, U.S.A.), Qiang Ma (Synopsys, Inc., U.S.A.), *Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.)

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2D-3 (Time: 14:40 - 15:10)

Title Layer Minimization in Escape Routing for Staggered-Pin-Array PCBs

Author *Yuan-Kai Ho, Xin-Wei Shih, Yao-Wen Chang (National Taiwan Univ., Taiwan), Chung-Kuan Cheng (Univ. of California, San Diego, U.S.A.)

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2D-4 (Time: 15:10 - 15:40)

Title	Network Flow Modeling for Escape Routing on Staggered Pin Arrays
Author	Pei-Ci Wu, *Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.)
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Session 3A Special Session: Design Automation for Flow-Based Microfluidic Biochips: Connecting Biochemistry to Electronic Design Automation
Time: 16:00 - 18:00 Wednesday, January 23, 2013
Organizer: Tsung-Yi Ho (National Cheng Kung Univ., Taiwan)

3A-1 (Time: 16:00 - 16:30)

Title	(Invited Paper) A Clique-Based Approach to Find Binding and Scheduling Result in Flow-Based Microfluidic Biochips
Author	*Trung Anh Dinh, Shigeru Yamashita (Ritsumeikan Univ., Japan), Tsung-Yi Ho (National Cheng Kung Univ., Taiwan), Yuko Hara-Azumi (NAIST, Japan)
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3A-2 (Time: 16:30 - 17:00)

Title	(Invited Paper) Control Synthesis of the Flow-Based Microfluidic Large-Scale Integration Biochips
Author	Wajid Hassan Minhass, *Paul Pop, Jan Madsen (Tech. Univ. of Denmark, Denmark), Tsung-Yi Ho (National Cheng Kung Univ., Taiwan)
Page	pp. 205 - 212

3A-3 (Time: 17:00 - 17:30)

Title	(Invited Paper) A Network-Flow Based Valve-Switching Aware Binding Algorithm for Flow-Based Microfluidic Biochips
Author	*Kai-Han Tseng, Sheng-Chi You (National Cheng Kung Univ., Taiwan), Wajid Hassan Minhass (Tech. Univ. of Denmark, Denmark), Tsung-Yi Ho (National Cheng Kung Univ., Taiwan), Paul Pop (Tech. Univ. of Denmark, Denmark)
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3A-4 (Time: 17:30 - 18:00)

Title (Invited Paper) Design and Verification Tools for Continuous Fluid Flow-based Microfluidic Devices

Author Jeffrey McDaniel, Aurelila Baez, Brian Crites, Aditya Tammewar, *Philip Brisk (Univ. of California, Riverside, U.S.A.)

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Session 3B System-Level Synthesis and Optimization

Time: 16:00 - 18:00 Wednesday, January 23, 2013

Chairs: Antoine Trouve (ISIT, Japan), Farhad Mehdipour (Kyushu Univ., Japan)

3B-1 (Time: 16:00 - 16:30)

Title Optimal Partition with Block-Level Parallelization in C-to-RTL Synthesis for Streaming Applications

Author *Shuangchen Li, Yongpan Liu (Tsinghua Univ., China), X.Sharon Hu (Univ. of Notre Dame, U.S.A.), Xinyu He, Yining Zhang (Tsinghua Univ., China), Pei Zhang (Y Explorations Inc., U.S.A.), Huazhong Yang (Tsinghua Univ., China)

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Title Multi-Mode Pipelined MPSoCs for Streaming Applications

Author *Haris Javaid, Daniel Witono, Sri Parameswaran (Univ. of New South Wales, Australia)

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3B-3 (Time: 17:00 - 17:30)

Title Network Simplex Method Based Multiple Voltage Scheduling in Power-Efficient High-Level Synthesis

Author *Cong Hao, Song Chen, Takeshi Yoshimura (Waseda Univ., Japan)

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3B-4 (Time: 17:30 - 18:00)

Title VISA Synthesis: Variation-Aware Instruction Set Architecture Synthesis

Author *Yuko Hara-Azumi (NAIST, Japan), Takuya Azumi (Ritsumeikan Univ., Japan), Nikil Dutt (Univ. of California, Irvine, U.S.A.)

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Session 3C Advanced Nanopatterning
Time: 16:00 - 18:00 Wednesday, January 23, 2013
Chair: Hidetoshi Matsuoka (Fujitsu Laboratory, Japan)

3C-1 (Time: 16:00 - 16:30)

Title L-Shape Based Layout Fracturing for E-Beam Lithography

Author Bei Yu, Jhih-Rong Gao, *David Z. Pan (Univ. of Texas, Austin, U.S.A.)

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3C-2 (Time: 16:30 - 17:00)

Title High-throughput Electron Beam Direct Writing of VIA Layers by Character Projection using Character Sets Based on One-dimensional VIA Arrays with Area-efficient Stencil Design

Author *Rimon Ikeno (Univ. of Tokyo, Japan), Takashi Maruyama Tetsuya Iizuka, Satoshi Komatsu, Makoto Ikeda, Kunihiro Asada (Univ. of Tokyo, Japan)

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3C-3 (Time: 17:00 - 17:30)

Title Linear Time Algorithm to Find All Relocation Positions for EUV Defect Mitigation

Author Yuelin Du (Univ. of Illinois, Urbana-Champaign, U.S.A.), Hongbo Zhang, Qiang Ma (Synopsys, Inc., U.S.A.), *Martin D. F. Wong (Univ. of Illinois, Urbana-Champaign, U.S.A.)

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3C-4 (Time: 17:30 - 18:00)

Title Self-Aligned Double and Quadruple Patterning-Aware Grid Routing with Hotspots Control

Author *Chikaaki Kodama (Toshiba Corp., Japan), Hirotaka Ichikawa (Toshiba

Microelectronics Corp., Japan), Koichi Nakayama, Toshiya Kotani, Shigeki Nojima, Shoji Mimotogi, Shinji Miyamoto (Toshiba Corp., Japan), Atsushi Takahashi (Tokyo Inst. of Tech., Japan)

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Session 3D Hardware-Software Co-Optimization for Emerging NVMs
Time: 16:00 - 18:00 Wednesday, January 23, 2013
Chairs: Yun (Eric) Liang (Peking Univ., China), Yiran Chen (Univ. of Pittsburgh, U.S.A.)

3D-1 (Time: 16:00 - 16:30)

Title Compiler-Assisted Refresh Minimization for Volatile STT-RAM Cache

Author Qingan Li (City Univ. of Hong Kong, Hong Kong), Jianhua Li, Liang Shi (Univ. of Science and Tech. of China, China), *Chun Jason Xue (City Univ. of Hong Kong, Hong Kong), Yiran Chen (Univ. of Pittsburgh, U.S.A.), Yanxiang He (Wuhan Univ., China)

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3D-2 (Time: 16:30 - 17:00)

Title Curling-PCM: Application-Specific Wear Leveling for Phase Change Memory based Embedded Systems

Author *Duo Liu (Chongqing Univ., China), Tianzheng Wang (Univ. of Toronto, Canada), Yi Wang, Zili Shao (Hong Kong Polytechnic Univ., Hong Kong), Qingfeng Zhuge, Edwin Sha (Chongqing Univ., China)

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3D-3 (Time: 17:00 - 17:30)

Title Selectively Protecting Error-Correcting Code for Area-Efficient and Reliable STT-RAM Caches

Author *Junwhan Ahn (Seoul National Univ., Republic of Korea), Sungjoo Yoo (POSTECH, Republic of Korea), Kiyoung Choi (Seoul National Univ., Republic of Korea)

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3D-4 (Time: 17:30 - 18:00)

Title Loadsa: A Yield-Driven Top-Down Design Method for STT-RAM Array

Author Wujie Wen, Yaojun Zhang, Lu Zhang, *Yiran Chen (Univ. of Pittsburgh, U.S.A.)

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Session 2K Keynote II
Time: 9:00 - 10:00 Thursday, January 24, 2013
Chair: Shinji Kimura (Waseda Univ., Japan)

2K-1 (Time: 9:00 - 10:00)

Title (Keynote Address) Gearing Up for the Upcoming Technology Nodes

Author Kee Sup Kim (Samsung, Republic of Korea)

Session 4A Special Session: High-Level Synthesis and Parallel Programming Models for FPGAs
Time: 10:20 - 12:20 Thursday, January 24, 2013
Organizer: Yun (Eric) Liang (Peking Univ., China)

4A-1 (Time: 10:20 - 10:50)

Title (Invited Paper) Fractal Video Compression in OpenCL: An Evaluation of CPUs, GPUs, and FPGAs as Acceleration Platforms

Author *Doris Chen, Deshanand Singh (Altera Toronto Technology Center, Canada)

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4A-2 (Time: 10:50 - 11:20)

Title (Invited Paper) High Level Synthesis of Multiple Dependent CUDA Kernels for FPGA

Author Swathi Gurumani, Hisham Cholakkail (Advanced Digital Sciences Center, Singapore), Yun Liang (Peking Univ., China), *Kyle Rupnow (Nanyang Technological Univ., Singapore), Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)

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4A-3 (Time: 11:20 - 11:50)

Title (Invited Paper) The Liquid Metal IP Bridge

Author Perry Cheng, Stephen J. Fink, Rodric Rabbah, *Sunil Shukla (IBM Research, U.S.A.)

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Session 4B Memory Hierarchy Optimization

Time: 10:20 - 12:20 Thursday, January 24, 2013

Chair: Jason Xue (City Univ. of Hong Kong, Hong Kong)

4B-1 (Time: 10:20 - 10:50)

Title TRISHUL: A Single-pass Optimal Two-level Inclusive Data Cache Hierarchy Selection Process for Real-time MPSoCs

Author *Mohammad Shihabul Haque, Akash Kumar, Yajun Ha, Qiang Wu, Shaobo Luo (National Univ. of Singapore, Singapore)

Page pp. 320 - 325

4B-2 (Time: 10:50 - 11:20)

Title Optimizing Translation Information Management in NAND Flash Memory Storage Systems

Author *Qi Zhang, Xuandong Li, Linzhang Wang, Tian Zhang (Nanjing Univ., China), Yi Wang, Zili Shao (Hong Kong Polytechnic Univ., Hong Kong)

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4B-3 (Time: 11:20 - 11:50)

Title An Adaptive Filtering Mechanism for Energy Efficient Data Prefetching

Author *Xianglei Dang, Xiaoyin Wang, Dong Tong, Zichao Xie, Lingda Li, Keyi Wang (Peking Univ., China)

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4B-4 (Time: 11:50 - 12:20)

Title Cache Capacity Aware Thread Scheduling for Irregular Memory Access on Many-Core GPGPUs

Author *Hsien-Kai Kuo, Ta-Kan Yen, Bo-Cheng Charles Lai, Jing-Yang Jou (National

Chiao Tung Univ., Taiwan)

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Session 4C Timing and Power Driven Design Flow

Time: 10:20 - 12:20 Thursday, January 24, 2013

Chairs: Masanori Hashimoto (Osaka Univ., Japan), Sheldon Tan (Univ. of California, Riverside, U.S.A.)

4C-1 (Time: 10:20 - 10:50)

Title Optimization for Overdrive Signoff

Author Tuck-Boon Chan, Andrew B. Kahng, *Jiajia Li, Siddhartha Nath (Univ. of California, San Diego, U.S.A.)

Page pp. 344 - 349

4C-2 (Time: 10:50 - 11:20)

Title Mountain-Mover: An Intuitive Logic Shifting Heuristic for Improving Timing Slack Violating Paths

Author *Xing Wei, Wai-Chung Tang, Yu-Liang Wu (Chinese Univ. of Hong Kong, Hong Kong), Cliff Sze, Charles Alpert (IBM, U.S.A.)

Page pp. 350 - 355

4C-3 (Time: 11:20 - 11:50)

Title Pulsed-Latch ASIC Synthesis in Industrial Design Flow

Author *Sangmin Kim, Duckhwan Kim, Youngsoo Shin (KAIST, Republic of Korea)

Page pp. 356 - 361

4C-4 (Time: 11:50 - 12:20)

Title Power Optimization for Application-Specific 3D Network-on-Chip with Multiple Supply Voltages

Author *Kan Wang, Sheqin Dong (Tsinghua Univ., China)

Page pp. 362 - 367

Session 4D Special Session: Emerging Security Topics in Electronic Designs and Mobile Devices

Time: 10:20 - 12:20 Thursday, January 24, 2013
Organizer: Yiran Chen (Univ. of Pittsburgh, U.S.A.)

4D-1 (Time: 10:20 - 10:50)

Title (Invited Paper) Hardware Security Strategies Exploiting Nanoelectronic Circuits

Author Garrett S. Rose (Air Force Research Laboratory, U.S.A.), *Jeyavijayan Rajendran (New York Univ., U.S.A.), Nathan McDonald (Air Force Research Laboratory, U.S.A.), Ramesh Karri (New York Univ., U.S.A.), Miodrag Potkonjak (Univ. of California, Los Angeles, U.S.A.), Bryant Wysocki (Air Force Research Laboratory, U.S.A.)

Page pp. 368 - 372

4D-2 (Time: 10:50 - 11:20)

Title (Invited Paper) Can We Identify Smartphone App by Power Trace?

Author Mian Dong, Po-Hsiang Lai, *Zhu Li (Samsung Telecommunications America, U.S.A.)

Page pp. 373 - 375

4D-3 (Time: 11:20 - 11:50)

Title (Invited Paper) Secure Storage System and Key Technologies

Author *Jiwu Shu, Zhirong Shen, Wei Xue, Yingxun Fu (Tsinghua Univ., China)

Page pp. 376 - 383

4D-4 (Time: 11:50 - 12:20)

Title (Invited Paper) Mobile User Classification and Authorization Based on Gesture Usage Recognition

Author *Kent W. Nixon, Xiang Chen, Zhi-Hong Mao (Univ. of Pittsburgh, U.S.A.), Kang Li (Rutgers Univ., U.S.A.), Yiran Chen (Univ. of Pittsburgh, U.S.A.)

Page pp. 384 - 389

Session 5A Designers' Forum: Heterogeneous Devices and Multi-Dimensional Integration Design Technologies
Time: 13:40 - 15:40 Thursday, January 24, 2013
Organizer: Akihiko Okubora (Sony, Japan)

5A-1 (Time: 13:40 - 14:10)

Title (Invited Paper) Challenges in Integration of Diverse Functionalities on CMOS

Author *Kazuya Masu, Noboru Ishihara (Tokyo Inst. of Tech., Japan), Toshifumi Konishi (NTT-AT, Japan), Katsuyuki Machida (Tokyo Inst. of Tech., Japan), Hiroshi Toshiyoshi (Univ. of Tokyo, Japan)

Page pp. 390 - 393

5A-2 (Time: 14:10 - 14:40)

Title (Invited Paper) 3DIC from Concept to Reality

Author Frank Lee, Bill Shen, Willy Chen, *Suk Lee (Taiwan Semiconductor Manufacturing Company, Taiwan)

Page pp. 394 - 398

5A-3 (Time: 14:40 - 15:10)

Title (Invited Paper) 2.5D Design Methodology

Author *Sinya Tokunaga (STARC, Japan)

Page pp. 399 - 402

5A-4 (Time: 15:10 - 15:40)

Title (Invited Paper) Design Issues in Heterogeneous 3D/2.5D Integration

Author *Dragomir Milojevic, Pol Marchal, Erik Jan Marinissen, Geert Van der Plas, Diederik Verkest, Eric Beyne (IMEC, Belgium)

Page pp. 403 - 410

Session 5B Analysis and Verification of Reliable Systems
Time: 13:40 - 15:40 Thursday, January 24, 2013
Chairs: Sri Parameswaran (Univ. of New South Wales, Australia), Ittetsu Taniguchi (Ritsumeikan Univ., Japan)
5B-1 (Time: 13:40 - 14:10)

Title Verifying Distributed Controllers using Time-Stamped ECAs

Author *Matthias Kauer, Sebastian Steinhorst, Martin Lukasiewycz (TUM CREATE, Singapore), Dip Goswami, Reinhard Schneider, Samarjit Chakraborty (TU Munich, Germany)

Page pp. 411 - 416

5B-2 (Time: 14:10 - 14:40)

Title Reliability Assessment of Safety-Relevant Automotive Systems in a Model-Based Design Flow

Author *Sebastian Reiter, Michael Pressler, Alexander Viehl (FZI Forschungszentrum Informatik, Germany), Oliver Bringmann, Wolfgang Rosenstiel (Univ. Tuebingen, Germany)

Page pp. 417 - 422

5B-3 (Time: 14:40 - 15:10)

Title Sequential Dependency and Reliability Analysis of Embedded System

Author Hehua Zhang, *Yu Jiang (Tsinghua Univ., China), William N.N Hung (Synopsys, Inc., U.S.A.), Xiaoyu Song (Portland State Univ., U.S.A.), Jiaguang Sun (Tsinghua Univ., China)

Page pp. 423 - 428

5B-4 (Time: 15:10 - 15:40)

Title Processor and DRAM Integration by TSV-Based 3-D Stacking for Power-Aware SOCs

Author Shin-Shiun Chen, Chun-Kai Hsu, *Hsiu-Chuan Shih (National Tsing Hua Univ., Taiwan), Jen-Chieh Yeh (ITRI, Taiwan), Cheng-Wen Wu (National Tsing Hua Univ., Taiwan)

Page pp. 429 - 434

Session 5C Advances in Physical Design

Time: 13:40 - 15:40 Thursday, January 24, 2013

Chairs: Sung Kyu Lim (Georgia Tech, U.S.A.), Yasuhiro Takashima (Univ. of Kitakyushu, Japan)

5C-1 (Time: 13:40 - 14:10)

Title A Flexible Fixed-outline Floorplanning Methodology for Mixed-size Modules

Author *Kai-Chung Chan, Chao-Jam Hsu, Jai-Ming Lin (National Cheng Kung Univ., Taiwan)

Page pp. 435 - 440

5C-2 (Time: 14:10 - 14:40)

Title Optimizing Routability in Large-Scale Mixed-Size Placement

Author Jason Cong (Univ. of California, Los Angeles, U.S.A.), Guojie Luo (Peking Univ., China), *Kalliopi Tsota, Bingjun Xiao (Univ. of California, Los Angeles, U.S.A.)

Page pp. 441 - 446

5C-3 (Time: 14:40 - 15:10)

Title Symmetrical Buffered Clock-Tree Synthesis with Supply-Voltage Alignment

Author Xin-Wei Shih (MediaTek, Taiwan), *Tzu-Hsuan Hsu (Linkwish, Taiwan), Hsu-Chieh Lee (Google, Taiwan), Yao-Wen Chang (National Taiwan Univ., Taiwan), Kai-Yuan Chao (Intel, U.S.A.)

Page pp. 447 - 452

5C-4 (Time: 15:10 - 15:40)

Title BCell: Automatic Layout of Leaf Cells

Author Stefan Hougardy, *Tim Nieberg, Jan Schneider (Univ. of Bonn, Germany)

Page pp. 453 - 460

Session 5D Multi-/Many-Core System Optimization

Time: 13:40 - 15:40 Thursday, January 24, 2013

Chairs: Yuichi Nakamura (NEC, Japan), Yongpan Liu (Tsinghua Univ., China)

5D-1 (Time: 13:40 - 14:10)

Title Register and Thread Structure Optimization for GPUs

Author *Yun Liang (Peking Univ., China), Zheng Cui (Advanced Digital Sciences Center, Illinois at Singapore, Singapore), Kyle Rupnow (Nanyang Technological Univ., Singapore), Deming Chen (Univ. of Illinois, Urbana-Champaign, U.S.A.)

Page pp. 461 - 466

5D-2 (Time: 14:10 - 14:40)

Title: Real-Time Partitioned Scheduling on Multi-Core Systems with Local and Global Memories

Author: *Che-Wei Chang (National Taiwan Univ., Taiwan), Jian-Jia Chen (Karlsruhe Inst. of Tech., Germany), Tei-Wei Kuo (National Taiwan Univ., Taiwan), Heiko Falk (Ulm Univ., Germany)

Page: pp. 467 - 472

5D-3 (Time: 14:40 - 15:10)

Title: Dynamic Thermal Management for Multi-Core Microprocessors Considering Transient Thermal Effects

Author: *Zao Liu (Univ. of California, Riverside, U.S.A.), Tailong Xu (Anhui Univ., China), Sheldon X.-D. Tan (Univ. of California, Riverside, U.S.A.), Hai Wang (UESTC, China)

Page: pp. 473 - 478

5D-4 (Time: 15:10 - 15:40)

Title: BAMSE: A Balanced Mapping Space Exploration Algorithm for GALS-based Manycore Platforms

Author: Mohammad Foroozannejad, Brent Bohnenstiehl, *Soheil Ghiasi (Univ. of California, Davis, U.S.A.)

Page: pp. 479 - 484

Session 6A Designers' Forum: Future Direction and Trend of Embedded GPU

Time: 16:00 - 18:00 Thursday, January 24, 2013

Organizer: Masaitsu Nakajima (Panasonic, Japan), Moderator: Koji Inoue (Kyushu Univ., Japan)

6A-1

Title: (Panel Discussion) Future Direction and Trend of Embedded GPU

Author: Panelists: Jem Davies (ARM, U.S.A.), Hong Jiang (Intel, U.S.A.), Eisaku Ohbuchi (Digital Media Professionals Inc., Japan), Yasushi Sugama (Fujitsu Laboratories, Japan), Tony King-Smith (Imagination Technologies, U.K.)

Session 6B Emerging Technologies

Time: 16:00 - 18:00 Thursday, January 24, 2013
Chairs: Tsung-Yi Ho (National Cheng Kung Univ., Taiwan), Zili Shao (Hong Kong Polytechnic Univ., Hong Kong)

6B-1 (Time: 16:00 - 16:30)

Title	Thermal Simulator of 3D-IC with Modeling of Anisotropic TSV Conductance and Microchannel Entrance Effects
Author	Hanhua Qian, Hao Liang, Chip-Hong Chang, Wei Zhang, *Hao Yu (Nanyang Technological Univ., Singapore)
Page	pp. 485 - 490

6B-2 (Time: 16:30 - 17:00)

Title	A Novel Cell Placement Algorithm for Flexible TFT Circuit with Mechanical Strain and Temperature Consideration
Author	*Juin-Li Lin, Po-Hsun Wu, Tsung-Yi Ho (National Cheng Kung Univ., Taiwan)
Page	pp. 491 - 496

6B-3 (Time: 17:00 - 17:30)

Title	Improving Energy Efficiency for Energy Harvesting Embedded Systems
Author	Yang Ge, Yukan Zhang, *Qinru Qiu (Syracuse Univ., U.S.A.)
Page	pp. 497 - 502

6B-4 (Time: 17:30 - 18:00)

Title	Modeling Variability and Irreproducibility of Nanoelectronic Resistive Switches for Circuit Simulation
Author	*Arne Heittmann, Tobias G. Noll (RWTH Aachen Univ., Germany)
Page	pp. 503 - 508

Session 6C New Directions in Modeling , Simulation, and Integrity

Time: 16:00 - 18:00 Thursday, January 24, 2013

Chairs: Hideki Asai (Shizuoka Univ., Japan), Sheldon Tan (Univ. of California, Riverside, U.S.A.)

6C-1 (Time: 16:00 - 16:30)

Title HS3DPG: Hierarchical Simulation for 3D P/G Network

Author *Shuai Tao, Xiaoming Chen, Yu Wang, Yuchun Ma (Tsinghua Univ., China), Yiyu Shi (Missouri Univ. of Science and Tech., U.S.A.), Hui Wang, Huazhong Yang (Tsinghua Univ., China)

Page pp. 509 - 514

6C-2 (Time: 16:30 - 17:00)

Title Piecewise-Polynomial Associated Transform Macromodeling Algorithm for Fast Nonlinear Circuit Simulation

Author *Yang Zhang, Neric Fong, Ngai Wong (Univ. of Hong Kong, Hong Kong)

Page pp. 515 - 520

6C-3 (Time: 17:00 - 17:30)

Title An Ultra-Compact Virtual Source FET Model for Deeply-Scaled Devices: Parameter Extraction and Validation for Standard Cell Libraries and Digital Circuits

Author *Li Yu, Omar Mysore, Lan Wei, Luca Daniel, Dimitri Antoniadis (MIT, U.S.A.), Ibrahim Elfadel (Masdar Inst. of Science and Tech., United Arab Emirates), Duane Boning (MIT, U.S.A.)

Page pp. 521 - 526

6C-4 (Time: 17:30 - 18:00)

Title On Potential Design Impacts of Electromigration Awareness

Author Andrew B. Kahng, *Siddhartha Nath, Tajana S. Rosing (Univ. of California, San Diego, U.S.A.)

Page pp. 527 - 532

Session 6D Advanced Test Technologies

Time: 16:00 - 18:00 Thursday, January 24, 2013

Chairs: Yasuo Sato (Kyushu Inst. of Tech., Japan), Takashi Sato (Kyoto Univ., Japan)

6D-1 (Time: 16:00 - 16:30)

Title Provably Optimal Test Cube Generation using Quantified Boolean Formula Solving

Author Matthias Sauer, *Sven Reimer (Univ. of Freiburg, Germany), Ilia Polian (Univ. of Passau, Germany), Tobias Schubert, Bernd Becker (Univ. of Freiburg, Germany)

Page pp. 533 - 539

6D-2 (Time: 16:30 - 17:00)

Title Synthesizing Multiple Scan Chains by Cost-Driven Spectral Ordering

Author *Louis Y.-Z. Lin, Christina C.-H. Liao, Charles H.-P. Wen (National Chiao Tung Univ., Taiwan)

Page pp. 540 - 545

6D-3 (Time: 17:00 - 17:30)

Title A Binding Algorithm in High-Level Synthesis for Path Delay Testability

Author *Yuki Yoshikawa (Kure National College of Tech., Japan)

Page pp. 546 - 551

6D-4 (Time: 17:30 - 18:00)

Title Full Exploitation of Process Variation Space for Continuous Delivery of Optimal Delay Test Quality

Author Baris Arslan (Univ. of California, San Diego/Qualcomm, U.S.A.), *Alex Orailoglu (Univ. of California, San Diego, U.S.A.)

Page pp. 552 - 557

Session 3K Keynote III

Time: 9:00 - 10:00 Friday, January 25, 2013

Chair: Shinji Kimura (Waseda Univ., Japan)

3K-1 (Time: 9:00 - 10:00)

Title (Keynote Address) Human, Vehicle and Social Infrastructure System Development

for Sustainable Mobility – Development Innovation based on Large-Scale Simulation –

Author Hiroyuki Watanabe (Toyota Motor Corp., Japan)

Session 7A Special Session: Many-Core Architecture and Software Technology

Time: 10:20 - 12:20 Friday, January 25, 2013
Chairs: Masato Edahiro (Nagoya Univ., Japan), Hiroyuki Tomiyama (Ritsumeikan Univ., Japan)

7A-1 (Time: 10:20 - 10:40)

Title (Invited Paper) SMYLE Project: Toward High-Performance, Low-Power Computing on Manycore-Processor SoCs

Author *Koji Inoue (Kyushu Univ., Japan)

Page pp. 558 - 560

7A-2 (Time: 10:40 - 11:05)

Title (Invited Paper) SMYLEref: A Reference Architecture for Manycore-Processor SoCs

Author *Masaaki Kondo, Son Truong Nguyen (Univ. of Electro-Communications, Japan), Tomoya Hirao, Takeshi Soga, Hiroshi Sasaki, Koji Inoue (Kyushu Univ., Japan)

Page pp. 561 - 564

7A-3 (Time: 11:05 - 11:30)

Title (Invited Paper) SMYLE OpenCL: A Programming Framework for Embedded Many-core SoCs

Author *Hiroyuki Tomiyama, Takuji Hieda, Naoki Nishiyama, Noriko Etani, Ittetsu Taniguchi (Ritsumeikan Univ., Japan)

Page pp. 565 - 567

7A-4 (Time: 11:30 - 11:55)

Title (Invited Paper) Support Tools for Porting Legacy Applications to Multicore

Author Yuri Ardila, *Natsuki Kawai, Takashi Nakamura, Yosuke Tamura (Fixstars Corp., Japan)

Page pp. 568 - 573

7A-5 (Time: 11:55 - 12:20)

Title (Invited Paper) Manycore Processor for Video Mining Applications

Author *Yukoh Matsumoto, Hiroyuki Uchida, Michiya Hagimoto, Yasumori Hibi, Sunao Torii, Masamichi Izumida (TOPS Systems Corp., Japan)

Page pp. 574 - 575

Session 7B Simulation Acceleration

Time: 10:20 - 12:20 Friday, January 25, 2013

Chairs: Farhad Mehdipour (Kyushu Univ., Japan), Antoine Trouve (ISIT, Japan)

7B-1 (Time: 10:20 - 10:50)

Title Native Simulation of Complex VLIW Instruction Sets using Static Binary Translation and Hardware-Assisted Virtualization

Author *Mian-Muhammad Hamayun, Frédéric Pétrot, Nicolas Fournel (TIMA Laboratory, CNRS/INP Grenoble/UJF, France)

Page pp. 576 - 581

7B-2 (Time: 10:50 - 11:20)

Title RExCache: Rapid Exploration of Unified Last-level Cache

Author *Su Myat Min Shwe, Haris Javaid, Sri Parameswaran (Univ. of New South Wales, Australia)

Page pp. 582 - 587

7B-3 (Time: 11:20 - 11:50)

Title An Efficient Hybrid Synchronization Technique for Scalable Multi-Core Instruction Set Simulations

Author *Bo-Han Zeng, Ren-Song Tsay, Ting-Chi Wang (National Tsing Hua Univ., Taiwan)

Page pp. 588 - 593

Session 7C Reliability Analysis and Test
Time: 10:20 - 12:20 Friday, January 25, 2013
Chairs: David Z. Pan (Univ. of Texas, Austin, U.S.A.), Alex Orailoglu (Univ. of California, San Diego, U.S.A.)

7C-1 (Time: 10:20 - 10:50)

Title Statistical Analysis of BTI in the Presence of Process-induced Voltage and Temperature Variations

Author *Farshad Firouzi, Saman Kiamehr, Mehdi B. Tahoori (Karlsruhe Inst. of Tech., Germany)

Page pp. 594 - 600

7C-2 (Time: 10:50 - 11:20)

Title CLASS: Combined Logic and Architectural Soft Error Sensitivity Analysis

Author *Mojtaba Ebrahimi, Liang Chen (Karlsruhe Inst. of Tech., Germany), Hossein Asadi (Sharif Univ. of Tech., Iran), Mehdi B. Tahoori (Karlsruhe Inst. of Tech., Germany)

Page pp. 601 - 607

7C-3 (Time: 11:20 - 11:50)

Title Application Specified Soft Error Failure Rate Analysis using Sequential Equivalence Checking Techniques

Author *Tun Li, Dan Zhu, Sikun Li, Yang Guo (National Univ. of Defense Tech., China)

Page pp. 608 - 613

7C-4 (Time: 11:50 - 12:20)

Title An Adaptive Current-Threshold Determination for IDDQ Testing Based on Bayesian Process Parameter Estimation

Author *Michihiro Shintani, Takashi Sato (Kyoto Univ., Japan)

Page pp. 614 - 619

Session 7D Emerging Technologies in Cyber Systems
Time: 10:20 - 12:20 Friday, January 25, 2013

Chairs: Hao Yu (Nanyang Technological Univ., Singapore), Guojie Luo (Peking Univ., China)

7D-1 (Time: 10:20 - 10:50)

Title: DARNS:A Randomized Multi-modulo RNS Architecture for Double-and-Add in ECC to Prevent Power Analysis Side Channel Attacks

Author: Jude Angelo Ambrose (Univ. of New South Wales, Australia), *Hector Pettenghi, Leonel Sousa (Instituto de Engenharia de Sistemas e Computadores, Portugal)

Page: pp. 620 - 625

7D-2 (Time: 10:50 - 11:20)

Title: ScanPUF: Robust Ultralow-Overhead PUF Using Scan Chain

Author: Yu Zheng, Aswin Raghav Krishna, *Swarup Bhunia (Case Western Reserve Univ., U.S.A.)

Page: pp. 626 - 631

7D-3 (Time: 11:20 - 11:50)

Title: An Efficient Compression Scheme for Checkpointing of FPGA-Based Digital Mockups

Author: *Ting-Shuo Chou (Univ. of California, Irvine, U.S.A.), Chen Huang, Bailey Miller (Univ. of California, Riverside, U.S.A.), Tony Givargis (Univ. of California, Irvine, U.S.A.), Frank Vahid (Univ. of California, Riverside, U.S.A.)

Page: pp. 632 - 637

7D-4 (Time: 11:50 - 12:20)

Title: Maximizing Return on Investment of a Grid-Connected Hybrid Electrical Energy Storage System

Author: Di Zhu, Yanzhi Wang, Siyu Yue, *Qing Xie (Univ. of Southern California, U.S.A.), Naehyuck Chang (Seoul National Univ., Republic of Korea), Massoud Pedram (Univ. of Southern California, U.S.A.)

Page: pp. 638 - 643

Session 8A Designers' Forum: Photonics for Embedded Systems

Time: 13:40 - 15:40 Friday, January 25, 2013

Organizer: Toshiki Sugawara (Hitachi, Japan)

8A-1 (Time: 13:40 - 14:10)

Title (Invited Paper) Silicon Photonics Technology Platform for Embedded and Integrated Optical Interconnect Systems

Author *Peter De Dobbelaere (Luxtera, U.S.A.)

Page pp. 644 - 647

8A-2 (Time: 14:10 - 14:40)

Title (Invited Paper) High-Frequency Circuit Design for 25Gb/s×4 Optical Transceiver

Author *Norio Chujo, Takashi Takemoto, Fumio Yuki, Hiroki Yamashita (Hitachi, Japan)

Page pp. 648 - 651

8A-3 (Time: 14:40 - 15:10)

Title (Invited Paper) Design and Application of Highly Integrated Optical Switches Based on Silicon Photonics

Author *Shigeru Nakamura (NEC, Japan)

Page pp. 652 - 654

8A-4 (Time: 15:10 - 15:40)

Title (Invited Paper) High Performance PIN Ge Photodetector and Si Optical Modulator with MOS Junction for Photonics-Electronics Convergence System

Author *Junichi Fujikata, Masataka Noguchi, Makoto Miura, Masashi Takahashi, Shigeki Takahashi, Tsuyoshi Horikawa, Yutaka Urino, Takahiro Nakamura, Yasuhiko Arakawa (PETRA, Japan)

Page pp. 655 - 656

Session 8B Revisiting Latency and Reliability in Memory Architectures

Time: 13:40 - 15:40 Friday, January 25, 2013

Chairs: Luca Carloni (Columbia Univ., U.S.A.), Fabien Clermidy (CEA-LETI, France)

8B-1 (Time: 13:40 - 14:10)

Title Reevaluating the Latency Claims of 3D Stacked Memories

Author *Daniel W. Chang (Univ. of Wisconsin, Madison, U.S.A.), Gyungsu Byun (West Virginia Univ., U.S.A.), Hoyoung Kim, Minwook Ahn, Soojung Ryu (Samsung

Electronics Co., Ltd., Republic of Korea), Nam S. Kim, Michael Schulte (Univ. of Wisconsin, Madison, U.S.A.)

Page pp. 657 - 662

8B-2 (Time: 14:10 - 14:40)

Title Heterogeneous Memory Management for 3D-DRAM and External DRAM with QoS

Author *Le-Nguyen Tran (Univ. of California, Irvine, U.S.A.), Houman Homayoun (George Mason Univ., U.S.A.), Fadi J. Kurdahi, Ahmed M. Eltawil (Univ. of California, Irvine, U.S.A.)

Page pp. 663 - 668

8B-3 (Time: 14:40 - 15:10)

Title Line Sharing Cache: Exploring Cache Capacity with Frequent Line Value Locality

Author *Keitarou Oka, Hiroshi Sasaki, Koji Inoue (Kyushu Univ., Japan)

Page pp. 669 - 674

8B-4 (Time: 15:10 - 15:40)

Title ShieldUS: A Novel Design of Dynamic Shielding for Eliminating 3D TSV Crosstalk Coupling Noise

Author *Yuan-Ying Chang, Yoshi Shih-Chieh Huang (National Tsing Hua Univ., Taiwan), Vijaykrishnan Narayanan (Pennsylvania State Univ., U.S.A.), Chung-Ta King (National Tsing Hua Univ., Taiwan)

Page pp. 675 - 680

Session 8C New 3D IC Design Techniques

Time: 13:40 - 15:40 Friday, January 25, 2013

Chairs: Guojie Luo (Peking Univ., China), Wai-Kei Mak (National Tsing Hua Univ., Taiwan)

8C-1 (Time: 13:40 - 14:10)

Title High-Density Integration of Functional Modules Using Monolithic 3D-IC Technology

Author *Shreepad Panth (Georgia Tech, U.S.A.), Kambiz Samadi, Yang Du (Qualcomm

Research, U.S.A.), Sung Kyu Lim (Georgia Tech, U.S.A.)

Page pp. 681 - 686

8C-2 (Time: 14:10 - 14:40)

Title Block-level Designs of Die-to-Wafer Bonded 3D ICs and Their Design Quality Tradeoffs

Author *Krit Athikulwongse (Georgia Tech, U.S.A.), Dae Hyun Kim (Cadence, U.S.A.), Moongon Jung, Sung Kyu Lim (Georgia Tech, U.S.A.)

Page pp. 687 - 692

8C-3 (Time: 14:40 - 15:10)

Title Thermal-reliable 3D Clock-tree Synthesis Considering Nonlinear Electrical-thermal-coupled TSV Model

Author Yang Shang, Chun Zhang, *Hao Yu, Chuan Seng Tan (Nanyang Technological Univ., Singapore), Xin Zhao, Sung Kyu Lim (Georgia Tech, U.S.A.)

Page pp. 693 - 698

8C-4 (Time: 15:10 - 15:40)

Title Stacking Signal TSV for Thermal Dissipation in Global Routing for 3D IC

Author *Po-Yang Hsu, Hsien-Te Chen, TingTing Hwang (National Tsing Hua Univ., Taiwan)

Page pp. 699 - 704

Session 8D Advances in Simulation and Formal Verification

Time: 13:40 - 15:40 Friday, January 25, 2013

Chairs: Miroslav Velev (Aries Design Automation, U.S.A.), Andreas Veneris (Univ. of Toronto, Canada)

8D-1 (Time: 13:40 - 14:10)

Title VFCC: A Verification Framework of Cache Coherence using Parallel Simulation

Author *Qiaoli Xiong, Jiangfang Yi, Tianbao Song, Zichao Xie, Dong Tong (Peking Univ., China)

Page pp. 705 - 710

8D-2 (Time: 14:10 - 14:40)

Title: A Computational Model for SAT-based Verification of Hardware-Dependent Low-Level Embedded System Software

Author: *Bernard Schmidt, Carlos Villarraga (Univ. of Kaiserslautern, Germany), Jörg Bormann (-, Germany), Dominik Stoffel, Markus Wedler, Wolfgang Kunz (Univ. of Kaiserslautern, Germany)

Page: pp. 711 - 716

8D-3 (Time: 14:40 - 15:10)

Title: Reviving Erroneous Stability-based Clock-Gating using Partial Max-SAT

Author: Bao Le, *Dipanjan Sengupta, Andreas Veneris (Univ. of Toronto, Canada)

Page: pp. 717 - 722

8D-4 (Time: 15:10 - 15:40)

Title: Simplification of C-RTL Equivalent Checking for Fused Multiply Add Unit using Intermediate Models

Author: *Bin Xue, Prosenjit Chatterjee (Nvidia Corp, U.S.A.), Sandeep K. Shukla (Virginia Tech, U.S.A.)

Page: pp. 723 - 728

Session 9A Designers' Forum: Harmonized Hardware-Software Co-Design and Co-Verification

Time: 16:00 - 18:00 Friday, January 25, 2013

Organizer: Nobuyuki Nishiguchi (STARC, Japan), Moderator: Koichiro Yamashita (Fujitsu Laboratories, Japan)

9A-1

Title: (Panel Discussion) Harmonized Hardware-Software Co-Design and Co-Verification

Author: Panelists: Atsushi Ike (Fujitsu Laboratories, Japan), Hiroyuki Ikegami (Renesas Electronics Corp., Japan), Tsuyoshi Isshiki (Tokyo Inst. of Tech., Japan), Rainer Leupers (RWTH Aachen, Germany), Yosinori Watanabe (Cadence Berkeley Lab, U.S.A.), Tim Kogel (Synopsys, U.S.A.)

Session 9B Memory and Storage Management
Time: 16:00 - 18:00 Friday, January 25, 2013
Chairs: Philip Brisk (Univ. of California, Riverside, U.S.A.), Samarjit Chakraborty (TU Munich, Germany)

9B-1 (Time: 16:00 - 16:30)

Title: Reconstruction of Memory Accesses Based on Memory Allocation Mechanism for Source-Level Simulation of Embedded Software

Author: *Kun Lu, Daniel Müller-Gritschneder, Ulf Schlichtmann (Technische Universität München, Germany)

Page: pp. 729 - 734

9B-2 (Time: 16:30 - 17:00)

Title: Shared Cache Aware Task Mapping for WCRT Minimization

Author: *Huping Ding (National Univ. of Singapore, China), Tulika Mitra (National Univ. of Singapore, Singapore)

Page: pp. 735 - 740

9B-3 (Time: 17:00 - 17:30)

Title: Scratchpad Memory Aware Task Scheduling with Minimum Number of Preemptions on a Single Processor

Author: *Qing Wan, Hui Wu, Jingling Xue (Univ. of New South Wales, Australia)

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9B-4 (Time: 17:30 - 18:00)

Title: Scheduling Multiple Charge Migration Tasks in Hybrid Electrical Energy Storage Systems

Author: Qing Xie, Di Zhu, Yanzhi Wang (Univ. of Southern California, U.S.A.), *Younghyun Kim, Naehyuck Chang (Seoul National Univ., Republic of Korea), Massoud Pedram (Univ. of Southern California, U.S.A.)

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Time: 16:00 - 18:00 Friday, January 25, 2013
Chairs: Sheldon Tan (Univ. of California, Riverside, U.S.A.), Takashi Sato (Kyoto Univ., Japan)

9C-1 (Time: 16:00 - 16:30)

Title: Stable Backward Reachability Correction for PLL Verification with Consideration of Environmental Noise Induced Jitter

Author: Yang Song, Haipeng Fu, *Hao Yu (Nanyang Technological Univ., Singapore), Guoyong Shi (Shanghai Jiao Tong Univ., China)

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9C-2 (Time: 16:30 - 17:00)

Title: Performance Bound and Yield Analysis for Analog Circuits under Process Variations

Author: Xue-Xin Liu (Univ. of California, Riverside, U.S.A.), Adolfo Adair Palma-Rodriguez, Santiago Rodriguez-Chavez (Institute of Astrophysics, Optics, and Electronics, Mexico),*Sheldon X.-D. Tan (Univ. of California, Riverside, U.S.A.), Esteban Tlelo-Cuautle (Institute of Astrophysics, Optics, and Electronics, Mexico), Yici Cai (Tsinghua Univ., China)

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9C-3 (Time: 17:00 - 17:30)

Title: Local Approximation Improvement of Trajectory Piecewise Linear Macromodels through Chebyshev Interpolating Polynomials

Author: Muhammad Umer Farooq, *Likun Xia (Univ. Teknologi PETRONAS, Malaysia)

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Session 9D High-Level and Architectural Synthesis

Time: 16:00 - 18:00 Friday, January 25, 2013
Chairs: Robert Wille (Univ. of Bremen, Germany), Takashi Takenaka (NEC, Japan)

9D-1 (Time: 16:00 - 16:30)

Title: Range and Bitmask Analysis for Hardware Optimization in High-Level Synthesis

Author: *Marcel Gort, Jason H. Anderson (Univ. of Toronto, Canada)

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9D-2 (Time: 16:30 - 17:00)

Title A Gradual Scheduling Framework for Problem Size Reduction and Cross Basic Block Parallelism Exploitation in High-level Synthesis

Author *Hongbin Zheng, Qingrui Liu, Junyi Li, Dihu Chen, Zixin Wang (Sun Yet-sen Univ., China)

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9D-3 (Time: 17:00 - 17:30)

Title Implementing Microprocessors from Simplified Descriptions

Author *Nikhil A. Patil, Derek Chiou (Univ. of Texas, Austin, U.S.A.)

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9D-4 (Time: 17:30 - 18:00)

Title Application-Specific Fault-Tolerant Architecture Synthesis for Digital Microfluidic Biochips

Author *Mirela Alistar, Paul Pop, Jan Madsen (Denmark Technical Univ., Denmark)

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