

# **2012 2nd IEEE CPMT Symposium Japan**

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# Program Session

December 10, 2012

## Room A

### 13:00-14:40 Session 1: High-Speed Optical Transceiver

Session Chair: Shigeru Nakagawa (IBM Research - Tokyo)

Fumio Koyama (Tokyo Institute of Technology)

- 1-1 **(Invited) Integration Technologies and Packaging for Efficient Si Photonics Links** **B#**  
Kannan Raj (Photonics Research Director, Oracle Labs)
- 1-2 **High-stability 25 Gb/s optical transceiver module with flexible polymer wave guide for optical interconnection**  
Naoki Matsushima<sup>1</sup>, Toshiaki Takai<sup>1</sup>, Daichi Kawamura<sup>2</sup>, Yasunobu Matsuoka<sup>2</sup>, Yong Lee<sup>2,3</sup>, Norio Chujo<sup>1</sup>, Takashi Takemoto<sup>2,3</sup>, Hiroki Yamashita<sup>2,3</sup>, Toshiki Sugawara<sup>2</sup>, Toru Yazaki<sup>1</sup> and Shinji Tsuji<sup>2,3</sup> (Yokohama Research Laboratory, Hitachi, Ltd.<sup>1</sup>, Central Research Laboratory, Hitachi, Ltd.<sup>2</sup>, Photonics Electronics Technology Research Association<sup>3</sup>)
- 1-3 **A 25-Gbit/s High-speed Optical-electrical Printed Circuit Board for Chip-to-chip Optical Interconnections**  
Yasunobu Matsuoka<sup>1,2</sup>, Koichiro Adachi<sup>1,2</sup>, Yong Lee<sup>1,2</sup> and Tatemi Ido<sup>1,2</sup> (Central Research Laboratories, Hitachi, Ltd.<sup>1</sup>, Photonics Electronics Technology Research Association<sup>2</sup>)
- 1-4 **Integrated Package for 100G Ethernet Optical Transmitter**  
Nobuyuki Yasui<sup>1</sup>, Koji Shibuya<sup>1</sup>, Tadashi Murao<sup>1</sup>, Takeshi Yamatoya<sup>2</sup>, Keita Mochizuki<sup>1</sup> and Hiroshi Aruga<sup>1</sup> (Information technology R & D Center, Mitsubishi Electric Corporation<sup>1</sup>, High Frequency & Optical Device Works, Mitsubishi Electric Corporation<sup>2</sup>)

### 15:10-16:50 Session 2: Optical Waveguide Technology

Session Chair: Shigenori Aoki (Fujitsu Laboratories LTD.)

Okihiro Sugihara (Tohoku University)

- 2-1 **(Invited) Graded-Index Core Polymer Optical Waveguide for High-Speed and High-Density On-Board Interconnects**  
Takaaki Ishigure (Faculty of Science and Technology, Keio University)
- 2-2 **Improvement of Polynorborene Waveguide Based O/E Module Performance with Microlens Structure**  
Motoya Kaneta, Shinsuke Terada, Akihiro Horimoto, Shinya Arai and Koji Choki (Circuitry with Optical Interconnection Business Development Dept., Sumitomo Bakelite Co., Ltd.)
- 2-3 **Light-induced self-written waveguide for optoelectronic integration devices**  
Tatsuya Yamashita, Daisuke Inoue, Akari Kawasaki, Osamu Watanabe and Manabu Kagami (Toyota Central R&D Labs., Inc.)
- 2-4 **Analysis of inter-channel crosstalk in multi-mode parallel optical waveguide using Beam Propagation Method**  
Takuya Kudo<sup>1</sup> and Takaaki Ishigure<sup>2</sup> (Graduate School of Science and Technology, Keio University<sup>1</sup>, Faculty of Science and Technology, Keio University<sup>2</sup>)

## Room B

### 13:00-14:40 Session 3: Low Temperature Bonding

Session Chair: Nobuhiro Imaizumi (Fujitsu Laboratories LTD.)

Shoji Uegaki (Advanced Semiconductor Engineering)

- 3-1 **Low-temperature bonding of laser diode chips using atmospheric-pressure plasma activation of flat topped Au <sup>\*\*\*\*</sup> & stud bumps with smooth surfaces.**  
Michitaka Yamamoto<sup>1</sup>, Takeshi Sato<sup>1</sup>, Eiji Higurashi<sup>2</sup>, Tadatomo Suga<sup>1</sup> and Renshi Sawada<sup>3</sup> (School of Engineering, The University of Tokyo<sup>1</sup>, Research Center for Advanced Science and Technology, The University of Tokyo<sup>2</sup>, Department of Intelligent Machinery and Systems, Kyushu University<sup>3</sup>)
- 3-2 **Low temperature Cu-Cu direct bonding for 3D-IC by using fine crystal layer<sup>\*\*\*\*\*</sup> &**  
Taiji Sakai, Nobuhiro Imaizumi, Toyoo Miyajima (Fujitsu Laboratories LTD.)
- 3-3 **Room Temperature Microjoining of qVGA Class Area-Bump Array Using Cone Bump <sup>\*\*\*\*\*</sup> \***  
Takanori Shuto, Keiichiro Iwanabe, Li Jing Qiu and Tanemasa Asano (Graduate School of Information Science and Electrical Engineering, Kyushu University)
- 3-4 **Cu wire bonding knows no limit - 28 nm is qualified <sup>\*\*\*\*\*</sup> ( \$**  
Bernd K Appelt, Andy Tseng, Shoji Uegaki, Louie Huang (ASE Group)

### 15:10-16:50 Session 4: Solder Bonding

Session Chair: Shoji Uegaki (Advanced Semiconductor Engineering)

Nobuhiro Imaizumi (Fujitsu Laboratories LTD.)

- 4-1 **Effect of preformed Cu-Sn IMC Layer on Electromigration Reliability of Solder Capped Cu Pillar Bump <sup>\*\*\*\*\*</sup> ) + Interconnection on an organic substrate**  
Yasumitsu Orii<sup>1</sup>, Kazushige Toriyama<sup>1</sup>, Sayuri Kohara<sup>1</sup>, Hirokazu Noma<sup>1</sup>, Keishi Okamoto<sup>1</sup> and Keisuke Uenishi<sup>2</sup> (IBM Research Tokyo<sup>1</sup>, Osaka University<sup>2</sup>)
- 4-2 **Productivity Improvement of Copper Pillar Flip-chip Package by Pre-applied Materials and Press Machine <sup>\*\*\*\*\*</sup> (-**  
Koji Motomura, Hiroki Maruo, Wanyu Tie, Hideki Eifuku, Shoji Sakemi and Tadahiko Sakai (Panasonic Factory Solutions Co., Ltd.)
- 4-3 **Joint Reliability Study of Solder Capped Metal Pillar Bump Interconnections on an Organic Substrate <sup>\*\*\*\*\*</sup> )'**  
Kazushige Toriyama<sup>1</sup>, Yasushi Takeoka<sup>2</sup>, Keishi Okamoto<sup>1</sup>, Hirokazu Noma<sup>1</sup> and Yasumitsu Orii<sup>1</sup> (IBM Japan, IBM Research-Tokyo<sup>1</sup>, IBM Japan Electronics Component Technology<sup>2</sup>)
- 4-4 **Impact Test Performance of Zn-based Die-attach Joints for Power Devices<sup>\*\*\*\*\*</sup> ( )**  
Jenn-Ming Song<sup>1</sup>, Meng-Ju Lin<sup>2</sup>, Yi-Shao Lai<sup>3</sup> and Ying-Ta Chiu<sup>3</sup> (Department of Materials Science and Engineering, National Chung Hsing University<sup>1</sup>, Department of Materials Science and Engineering, National Dong Hwa University<sup>2</sup>, Central Labs, Advanced Semiconductor Engineering, Inc.<sup>3</sup>)

## Room C

### 13:00-14:40 Session 5: R&D from China

Session Chair: Yinghui Wang (University of Tokyo)

Daoguo YANG (Guilin University of Electronic Technology)

5-1 **(Invited) Fast Life-time Assessment of LED Luminaries** \*\*\*\*\*%

Daoguo Yang, Miao Cai, Wenbin Chen and Zhen Zhang (Guilin University of Electronic Technology)

5-2 **(Invited) Solid-state Bonding Using Metallic Cone Layer for Interconnection** \*\*\*\*\*)

Ming Li<sup>1</sup>, Anmin Hu<sup>2</sup>, Zhuo Chen<sup>1</sup>, Qin Lu<sup>1</sup>, Wenjing Zhang<sup>1</sup>, Tadatomo Suga<sup>2</sup>, Yinghui Wang<sup>2</sup>, Eiji Higurashi<sup>2</sup> and Masahisa Fujino<sup>2</sup> (State Key Laboratory of Metal Matrix Composites, Key Laboratory for Thin Film and Microfabrication Technology of the Ministry of Education, School of Material Science and Engineering, Shanghai Jiao Tong University<sup>1</sup>, School of Engineering, University of Tokyo<sup>2</sup>)

5-3 **Ni Barrier for Tin Whisker Mitigation** \*\*\*\*\*\$

Ting Liu<sup>1</sup>, Dongyan Ding<sup>1</sup>, Yiqing Wang<sup>1</sup>, Yu Hu<sup>2</sup>, Yihua Gong<sup>2</sup> and Klaus-Peter Galuschki<sup>3</sup> (Institute of Microelectronic Materials & Technology, School of Materials Science and Engineering, Shanghai Jiao Tong University<sup>1</sup>, Electronic Assembly Processes & Materials, Corporate Technology, Siemens Ltd.<sup>2</sup>, Siemens AG<sup>3</sup>)

### 15:10-16:50 Session 6: R&D from China

Session Chair: Daoguo YANG (Guilin University of Electronic Technology)

Yinghui Wang (University of Tokyo)

6-1 **(Invited) JCAP Technology Introduction** \*\*\*B#

Kim-Hwee Tan (Jiangyin Changdian Advanced Packaging Co., Ltd.)

6-2 **(Invited) Heterogeneous Integration of MEMS Sensor Array and CMOS Readout IC with Through Silicon Via** \*\*\*\*+(  
Interconnects

Qian Wang, Siyi Xie, Tao Wang, Jian Cai, Ziyu Liu, Dong Wu, Mengyun Yue, Zheyao Wang, Shuidi Wang and Songliang Jia (Institute of Microelectronics, Tsinghua University)

6-3 **Electrochemical Analysis of Cathode in TSV Copper Electroplating** \*\*\*\*+-

Haiyong Cao<sup>1</sup>, Xue Feng<sup>1</sup>, Qi Sun<sup>1</sup>, Wei Luo<sup>1</sup>, Huiqin Ling<sup>1</sup>, Jiangyan Sun<sup>2</sup> and Ming Li<sup>1</sup> (Institute of Microelectronic Materials & Technology, School of Materials Science and engineering, Shanghai Jiao Tong University<sup>1</sup>, Shanghai Sinyang Semiconductor Materials Co., Ltd.<sup>2</sup>)

## Room S

### 13:00-14:40 Session 7: System in Packaging

Session Chair: Michitaka Kimura (Renesas Electronics Corporation)  
Kenji Takahashi (Toshiba Corporation)

- 7-1 **(Invited) 3D Packaging Trend - TSV or TMV? B#5**  
Akito Yoshida (Amkor Technology Japan)
- 7-2 **Thin Packaging – What is Next? ,'**  
Bernd K Appelt, Andy Tseng, Shoji Uegaki and Kay Essig (Advanced Semiconductor Engineering Group)
- 7-3 **Large Scale System-in-Package (SiP) Module for Future Networking Products , +**  
Ryusuke Ohta<sup>2</sup>, Mohan Nagar<sup>1</sup>, Mudasir Ahmad<sup>1</sup>, Michiaki Tamagawa<sup>2</sup>, Katsumi Miyata<sup>2</sup> and Takuya Suzuki<sup>2</sup> (Cisco Systems Inc.<sup>1</sup> Fujitsu Integrated Microtechnology Ltd.<sup>2</sup>)
- 7-4 **High Density Package Solutions for Next-Generation Smartphone, Ultrabook and Tablet Computing A#DE**  
Vern Solberg, Wael Zohni and Ilyas Mohammed (Invensas Corporation)

### 15:10-16:50 Session 8: Advanced Packaging

Session Chair: Hiroshi Yamada (Toshiba Corporation)  
Michitaka Kimura (Renesas Electronics Corporation)

- 8-1 **Novel DAF (Die Attach Film) separation technologies for ultra-thin chip - %**  
Shinya Takyu, Tetsuya Kurosawa and Akira Tomono (Toshiba Corporation Semiconductor & Storage Products Company)
- 8-2 **Volume production technologies of passive and active components embedded PWB - )**  
Hiroyuki Saito, Kiyotake Ikura and Naoki Kitajima (Dai Nippon Printing Co., Ltd.)
- 8-3 **Electrical Properties of Flexible Vertically aligned Carbon Nanotube Bumps under Compression A#UJ**  
Masahisa Fujino, Hidenori Terasaka, Tadatomo Suga, Ikuo Soga, Daiyu Kondo, Yoshikatsu Ishizuki and Taisuke Iwai (Department of Precision Engineering, The University of Tokyo)
- 8-4 **(Invited) Challenges of 3D-IC in the Era of Big Data A#DE**  
Yasumitsu Orii (IBM Research Tokyo)

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**Room A**

**9:00-10:45 Session 9: Devices for Optical Interconnect**

Session Chair: Takaaki Ishigure (Keio University)

Tatsuya Yamashita (Toyota Central R&D Labs. Inc.)

- 9-1 **(Invited) Next Generation Optical Interconnect Devices Using Photonic Polymers**  
Okihiro Sugihara (Tohoku University)
- 9-2 **Athermal and Tunable VCSELs with a Thermally Actuated Cantilever Structure for WDM Optical Interconnects**  
Hayato Sano, Norihiko Nakata, Masanori Nakahama, Akihiro Matsutani and Fumio Koyama (Photonic Integration System Research Center, Tokyo Institute of Technology)
- 9-3 **Modeling and Experiment on Low Voltage Slow-Light Electro-absorption Modulators for High-speed and Low Power Consumption Optical Interconnect**  
Syoki Shimizu, Xiaodong Gu, Toshikazu Shimada, Akihiro Matsutani and Fumio Koyama (Photonics Integration System Research Center, Tokyo Institute of Technology)
- 9-4 **Cavity-resonator-integrated Guided-mode Resonance Filter with Reflection Phase Variation**  
Junichi Inoue<sup>1</sup>, Tomonori Ogura<sup>1</sup>, Koji Hatanaka<sup>1</sup>, Kenji Kintaka<sup>2</sup>, Kenzo Nishio<sup>1</sup>, Yasuhiro Awatsuji<sup>1</sup> and Shogo Ura<sup>1</sup> (Kyoto Institute of Technology<sup>1</sup>, National Institute of Advanced Industrial Science and Technology<sup>2</sup>)

**11:00-12:45 Session 10: Optical and Electrical Coupling**

Session Chair: Kannan Raj (Oracle Labs.)

Shogo Ura (Kyoto Institute of Technology)

- 10-1 **Compact multi-fiber receptacle interface for on-board optical interconnection**  
Kota Shikama, Shuichiro Asakawa, Yoshiteru Abe, Shuichi Yanagi, Junya Kobayashi and Tetsuo Takahashi (NTT Photonics Laboratories, NTT Corporation)
- 10-2 **Sn-Ag-Cu-solder-reflow-capable 10-Gb/s × 4-channel very thin high-density parallel-optical modules**  
Kazuya Nagashima, Yozo Ishikawa and Hideyuki Nasu (FITEL Photonics Laboratory, Furukawa Electric Co., Ltd.)
- 10-3 **Development of Low-Cost Elastic Optical Multifiber Connector for Optical Interconnection**  
Tsuyoshi Aoki<sup>1</sup>, Hidenobu Muranaka<sup>1</sup>, Shigenori Aoki<sup>1</sup>, Katsuki Suematsu<sup>2</sup>, Mitsuhiro Iwaya<sup>2</sup> and Masato Shiino<sup>2</sup> (Fujitsu Laboratories Ltd.<sup>1</sup>, Furukawa Electric Co., Ltd.<sup>2</sup>)
- 10-4 **A compound of RGB-splitter and condensers for compact image sensor**  
Tadayuki Hirano<sup>1</sup>, Naoko Shimatani<sup>1</sup>, Kenji Kintaka<sup>2</sup>, Kenzo Nishio<sup>1</sup>, Yasuhiro Awatsuji<sup>1</sup> and Shogo Ura<sup>1</sup> (Kyoto Institute of Technology<sup>1</sup>, National Institute of Advanced Industrial Science and Technology<sup>2</sup>)

**13:40-15:20 Session 11: Optoelectronic Packaging**

Session Chair: Ricky Lee (Hong Kong University of Science and Technology, Hong Kong)

Atsushi Okuno (SANYU REC Co., Ltd.)

- 11-1 **Ultracompact 4x3.4 Gbps Optoelectronic Package for an Active Optical HDMI Cable**  
Norbert Schleppe<sup>1</sup>, Michihiko Nishigaki<sup>1</sup>, Hiroshi Uemura<sup>1</sup>, Hideto Furuyama<sup>1</sup>, Yoshiaki Sugizaki<sup>1</sup>, Hideki Shibata<sup>1</sup> and Yasuhito Koike<sup>2</sup> (Center for Semiconductor Research and Development, Semiconductor & Storage Products Company, Toshiba Corporation<sup>1</sup>, Faculty of Science and Technology, Keio University<sup>2</sup>)
- 11-2 **High Bright White LED Packaging Systems Using Unique Vacuum Printing Technology (VPES)**  
Atsushi Okuno, Yoshiteru Miyawaki, Osamu Tanaka, June Ooki, Makoto Okuda and Hirofumi Torigoe (SANYU REC Co., Ltd.)
- 11-3 **Effects of GaN Blue LED Chips and Phosphors on Optical Performance of White Light LED**  
Huishan Zhao<sup>1,2</sup>, Changying Chen<sup>1</sup> and S. W. Ricky Lee<sup>2</sup> (Department<sup>1</sup> of Optoelectronic Engineering, Jinan University<sup>1</sup>, HKUST LED-FPD Technology R&D Center at Foshan<sup>2</sup>)
- 11-4 **Color Tuning dispense process to minimize color variation**  
Masaru Nonomura (Panasonic Factory Solutions Co., Ltd.)

**15:40-16:55 Session 12: 3D Technology**

Session Chair: Hiroshi Yamada (Toshiba Corporation)

Michitaka Kimura (Renesas Electronics Corporation)

- 12-1 **Temporary Bonding / De-Bonding and Permanent Wafer Bonding Solutions for 3D Integration** +  
Hiroyuki Ishida<sup>1</sup>, Sumant Sood<sup>2</sup>, Christopher Rosenthal<sup>2</sup> and Stefan Lutter<sup>3</sup> (SUSS MicroTec KK<sup>1</sup>, SUSS MicroTec Inc.<sup>2</sup>, SUSS MicroTec Lithography GmbH<sup>3</sup>)
- 12-2 **Low Cost TSV Integration for Advanced Packaging Technologies** %  
Yasuhiro Morikawa, Takahide Murayama, Toshiyuki Sakuishi, Ai Tanaka, Yuu Nakamuta and Koukou Suu (ULVAC, Inc., Institute of Semiconductor and Electronics Technologies)
- 12-3 **Wide Bus Chip-to-Chip Interconnection Technology Using Fine Pitch Bump Joint Array for 3D LSI Chip Stacking** )  
Masahiro Aoyagi<sup>1</sup>, Fumito Imura<sup>1</sup>, Shunsuke Nemoto<sup>1</sup>, Naoya Watanabe<sup>1</sup>, Fumiki Kato<sup>1</sup>, Katsuya Kikuchi<sup>1</sup>, Hiroshi Nakagawa<sup>1</sup>, Michiya Hagimoto<sup>2</sup>, Hiroyuki Uchida<sup>2</sup> and Yukoh Matsumoto<sup>2</sup> (Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology (AIST)<sup>1</sup>, TOPS Systems Corporation<sup>2</sup>)

## Room B

### 9:00-10:45 Session 13: Reliability

Session Chair: Tadahiro Shibutani (Yokohama National University)  
Masao Sakane (Ritsumeikan University)

- 13-1 **Board Level Drop Test Modeling** -  
Masazumi Amagai and Jang Seungmin (Modeling Group, TMG Japan, Texas Instruments )
- 13-2 **Investigation of Fracture Behaviors of Cu-Sn Intermetallics using Impact Test** '  
Chaoran Yang and S. W. Ricky Lee (Department of Mechanical Engineering, Center for Advanced Microsystems Packaging, Hong Kong University of Science & Technology)
- 13-3 **Prognostic health monitoring method for printed circuit boards subjected to random cyclic loads** +  
Kenji Hirohata, Yousuke Hisakuni, Takahiro Omori and Minoru Mukai (Toshiba Corporation, Corporate Research and Development Center)
- 13-4 **A Built-in Electrical Test Circuit for Interconnect Tests in Assembled PCBs** %  
Widianto<sup>1</sup>, Hiroyuki Yotsuyanagi<sup>1</sup>, Akira Ono<sup>2</sup>, Masao Takagi<sup>2</sup>, Zvi Roth<sup>3</sup> and Masaki Hashizume<sup>1</sup> (The University of Tokushima<sup>1</sup>, Kagawa National College of Technology<sup>2</sup>, Florida Atlantic University<sup>3</sup>)

### 11:00-12:45 Session 14: Reliability

Session Chair: Takamoto Ito (Fukui University)  
Kenji Hirohata (Toshiba Corporation)

- 14-1 **Warpage Modeling for 3D Packages** %  
Masazumi Amagai and Yutaka Suzuki (Modeling Group, TMG Japan, Texas Instruments )
- 14-2 **In-situ Observation of Whisker Nucleation in Air with AFM** %  
Hiroshi Onuki and Tadahiro Shibutani (Yokohama National University)
- 14-3 **Low Cycle Fatigue Crack Initiation and Propagation Behavior of Copper Thin Films Used in Electronic Devices** % '  
Tasuku Kambayashi<sup>1</sup>, Masao Sakane<sup>1</sup> and Kenji Hirohata<sup>2</sup> (Department of Mechanical Engineering, Ritsumeikan University<sup>1</sup>, Toshiba Corporation, Corporate Research & Development Center<sup>2</sup>)
- 14-4 **Nondestructive defect analysis solution using combination of Lock-in IR Thermography and high resolution X-ray + CT technology** % +  
Naoki Seimiya (Marubun Corporation)

### 13:40-15:20 Session 15: Material

Session Chair: Takashi Hattori (Hitachi Ltd.)  
Phillip Hall (FUJI MACHINE MFG. Co., Ltd.)

- 15-1 **Development of DAF (Die Attach Film) with functional gettering agent for metal impurities** % \$  
Shinya Takyu, Norihiro Togasaki, Tetsuya Kurosawa, Yuji Yamada, Makiko Tamaoki, Hidekazu Hayashi and Hiroshi Tomita (Toshiba Corporation Semiconductor & Storage Products Company)
- 15-2 **Examination of insoluble anodes used for acid copper plating** % (  
Hideki Hagiwara (EBARA-UDYLITE CO., LTD.)
- 15-3 **Effects of additional Ni and Co on microstructural evolution in Sn-Ag-Bi-In solder under current stressing** % +  
Youngseok Kim<sup>1</sup>, Toru Sugahara<sup>1</sup>, Shijo Nagao<sup>1</sup>, Katsuaki Suganuma<sup>1</sup>, Minoru Ueshima<sup>2</sup>, Hans-Juergen Albrecht<sup>3</sup>, Klaus Wilke<sup>3</sup> and Joerg Strogies<sup>3</sup> (ISIR, Osaka University<sup>1</sup>, Taguchi Laboratory, Senju Metal Industry CO., LTD.<sup>2</sup>, Siemens AG, Corporate Technology<sup>3</sup>)



**15:40-16:55 Session 16: Electric Conductive Material**

Session Chair: Phillip Hall (FUJI MACHINE MFG. Co., Ltd.)

Tomonori Minegishi (Hitachi Chemical Co., Ltd.)

16-1 **Surface Characterization of Resilience Sheet as a Packaging Material for the Metallic Ink Printing**

Kiyokazu Yasuda (Osaka University)

16-2 **Thermal and Electric Conductive Analysis in Isotropical Conductive Adhesive by Modeling 3D Fillers Dispersion Observed by FIB-SEM**

Osamu Arai, Akira Shintai and Akio Sugiura (DENSO Co., Ltd.)

16-3 **Phase transformation of Cu@Ag Core-shell Nanoparticles upon Heating**

Chi-Hang Tsai<sup>1</sup>, Shih-Yun Chen<sup>2</sup>, Jenn-Ming Song<sup>3</sup>, In-Gann Chen<sup>4</sup> and Hsin-Yi Lee<sup>5</sup> (Graduate Institute of Applied Science and Technology, National Taiwan University of Science and Technology<sup>1</sup>, Department of Materials Science and Engineering, National Taiwan University of Science and Technology<sup>2</sup>, Department of Materials Science and Engineering, National Chung Hsing University<sup>3</sup>, Department of Materials Science and Engineering, National Cheng Kung University<sup>4</sup>, National Synchrotron Radiation Research Center<sup>5</sup>)

## Room C

### 9:00-10:45 Session 17: Noise and Crosstalk Reduction

Session Chair: Jianqing Wang (Nagoya Institute of Technology)  
Yutaka Uematsu (Hitachi Ltd.)

- 17-1 **Novel EMI Shielding Methodology on Highly Integration SiP Module**  
Liao Kuo-Hsien, Alex Chi-Hong Chan, Shen Chia Hsien, Lin I-Chia and Huang Hsin Wen (Advanced Semiconductor Engineering Inc.)
- 17-2 **Proposal and analysis of three-phase filter by using mixed-mode S-parameter based on Fortescue transformation**  
Yoshikazu Fujishiro and Kohji Koshiji (Faculty of Science and Technology, Tokyo University of Science)
- 17-3 **VLSI Nano-Scale Interconnect Induced Crosstalk Power Estimation**  
Atefesadat Seyedolhosseini, Nasser Masoumi and Milad Mehri (Advanced VLSI Laboratory, School of Electrical and Computer Engineering, College of Eng., University of Tehran)
- 17-4 **Statistical Study of Nano-Scale VLSI Interconnect Crosstalk and Its Induced Power Estimation**  
Milad Mehri<sup>1</sup>, Resza Sarvari<sup>2</sup> and Atefesadat Seyedolhosseini<sup>1</sup> (School of Electrical and Computer Engineering, College of Eng., University of Tehran<sup>1</sup>, Faculty of Electrical Engineering, Sharif University of Technology<sup>2</sup>)

### 11:00-12:45 Session 18: Integration Technology

Session Chair: Taras Kushta (NEC Corporation)  
Nobuhiro Kuga (Yokohama National University)

- 18-1 **(Invited) 60GHz Antenna Integrated Transmitter Module**  
Noriharu Suematsu, Shoichu Tanifuji, Satoshi Yoshida, Yuya Suzuki, Suguru Kameda, Tadashi Takagi and Kazuo Tsubouchi (Tohoku University)
- 18-2 **3D integration techniques using stacked PCBs and small dipole antenna for wireless sensor nodes**  
Shoichi Oshima, Kenichi Matsunaga, Hiroki Morimura and Mitsuru Harada (NTT Microsystem Integration Laboratories)
- 18-3 **Wireless Body Area Communication using Electromagnetic Resonance Coupling**  
Fukuro Koshiji<sup>1,3</sup>, Nanako Yuyama<sup>1</sup> and Kohji Koshiji<sup>2,3</sup> (School of Science and Engineering, Kokushikan University<sup>1</sup>, Faculty of Science and Technology, Tokyo University of Science<sup>2</sup>, Research Institute for Science and Technology, Tokyo University of Science<sup>3</sup>)
- 18-4 **Development of Human Body Communication Transceiver Based on Impulse Radio Scheme**  
Kageyuki Shikada and Jianqing Wang (Nagoya Institute of Technology)

### 13:40-15:20 Session 19: Circuit Operation Stability

Session Chair: A. Ege Engin (San Diego University)  
Hideki Osaka (Hitachi Ltd.)

- 19-1 **Measurement Results of Substrate Bias Dependency on Negative Bias Temperature Instability Degradation in a 65 nm Process**  
Syuichi Tanihiro<sup>1</sup>, Michitarou Yabuuchi<sup>1</sup> and Kazutoshi Kobayashi<sup>2</sup> (Department of Electronics, Kyoto Institute of Technology<sup>1</sup>, JST. CREST<sup>2</sup>)
- 19-2 **Co-simulation of AC Power Noise of CMOS Microprocessor using Capacitor Charging Modeling**  
Kumpei Yoshikawa and Makoto Nagata (Graduate School of System Informatics, Kobe University)
- 19-3 **Power Supply Noise Suppression By Optimizing On-die PDN Impedance**  
Yoshinori Kobayashi, Ryota Kobayashi, Tatsuya Mido, Genki Kubo, Hiroki Otsuka, Hideyuki Fujii and Toshio Sudo (Shibaura Institute of Technology)
- 19-4 **Macromodeling of Complex Power Delivery Networks for Efficient Transient Simulation**  
A. Ege Engin<sup>1</sup>, Bhavya Adepu<sup>1</sup>, Manabu Kusumoto<sup>2</sup> and Takashi Harada<sup>2</sup> (San Diego State University<sup>1</sup>, NEC Corporation<sup>2</sup>)

**15:40-16:55 Session 20: Power Integrity & Signal Integrity**

Session Chair: Hideki Osaka (Hitachi Ltd.)

Takashi Harada (NEC Corporation)

20-1 **Novel Technology for Power Integrity using by Metal Particle Conductive Layer**

Norifumi Sasaoka<sup>1</sup>, Takafumi Ochi<sup>1</sup>, Masato Oono<sup>1</sup>, Chihiro Ueda<sup>2</sup>, Yutaka Akiyama<sup>2</sup> and Kanji Otsuka<sup>2</sup> (Nippon Kodoshi Corporation<sup>1</sup>, Meisei University<sup>2</sup> )

20-2 **A Signal and Power Integrity Oriented Packaging for Low Cost and High Performance Systems**

Daisuke Iguchi and Hideyuki Umekawa (Fuji Xerox Co., Ltd.)

20-3 **Electromagnetic Band Gap structure for cut off of low frequency noise in 3-D printed circuit board**

Tadahiro Sasaki<sup>1</sup>, Hiroshi Yamada<sup>1</sup>, Kazuhiko Itaya<sup>1</sup>, Tooru Kijima<sup>2</sup> and Kazuhisa Imura<sup>2</sup> (Corporate Research & Development Center, Toshiba Corporation<sup>1</sup>, Toshiba Corporation Social Infrastructure Systems Company<sup>2</sup> )

## Room S

### 9:00-10:45 Session 21: Chip/Wafer Level Packaging

Session Chair: Hideki Sasaki (Renesas Electronics Corporation)  
Shinya Takyu (Toshiba Corporation)

- 21-1 **Development of a Novel Thermal Compression Flip Chip Bonding with Pre-Applied NCF Underfill** \*\*\*\*&+  
Kota Takeda, Takao Koshi, Kenkichi Arai, Yoshihiro Machida, Kiyoshi Oi, Yuka Tamadate, Tsuyoshi Sohara, Yasushi Araki and Takashi Ozawa (IC Assembly Division, Shinko Electric Industries Co., LTD.)
- 21-2 **Using Nano-Porous Au-Ag Sheets as a Joint Layer for Low-Temperature Au-Au Bonding** \*\*\*\*&+  
Hayata Mimatsu<sup>1</sup>, Jun Mizuno<sup>2</sup>, Takashi Kasahara<sup>1</sup>, Mikiko Saito<sup>3</sup>, Hiroshi Nishikawa<sup>3</sup> and Shuichi Shoji<sup>1</sup> (Major in Nano-science and Nano-engineering, Waseda University<sup>1</sup>, Institute for Nanoscience and Nanotechnology, Waseda University<sup>2</sup>, Joining and Welding Research Institute, Osaka University<sup>3</sup>)
- 21-3 **Development of Low Temperature Curable Positive Tone Photosensitive Dielectric Material** \*\*\*\*& %  
Akitoshi Tanimoto<sup>1</sup>, Koichi Abe<sup>1</sup>, Shigeru Nobe<sup>2</sup> and Hiroshi Matsutani<sup>1</sup> (Tsukuba Research Laboratory, Hitachi Chemical Co., Ltd.<sup>1</sup>, Semiconductor Materials Division, Hitachi Chemical Co., Ltd.<sup>2</sup>)
- 21-4 **Low Temperature Bonding Using Sub-micron Au Particles for Wafer-level MEMS Packaging** \*\*\*\*& (   
Shin Ito<sup>1</sup>, Jun Mizuno<sup>1</sup>, Hiroyuki Ishida<sup>2</sup>, Toshinori Ogashiwa<sup>3</sup>, Yukio Kanehira<sup>3</sup>, Hiroshi Murai<sup>3</sup>, Fumihiko Wakui<sup>4</sup> and Shuichi Shoji<sup>1</sup> (Waseda University<sup>1</sup>, SUSS MicroTec KK.<sup>2</sup>, Tanaka Kikinzoku Kogyo K.K.<sup>3</sup>, Tokyo Institute of Technology<sup>4</sup>)

### 11:00-12:45 Session 22: 3-D Integration by ASET "Dream Chip Project"

Session Chair: Kanji Otsuka (Meisei University)  
Masahiro Aoyagi (National Institute of Advanced Industrial Science and Technology)

- 22-1 **Chip-Based Hetero-Integration Technology for High-Performance 3D Stacked Image Sensor** \*\*\*\*& ,  
Yuki Ohara<sup>1</sup>, Kang Wook Lee<sup>1</sup>, Koji Kiyoyama<sup>1,2</sup>, Shigehide Konno<sup>1</sup>, Yutaka Sato<sup>1</sup>, Shuichi Watanabe<sup>1,3</sup>, Atsushi Yabata<sup>1,3</sup>, Harufumi Kobayashi<sup>3</sup>, Tadashi Kamada<sup>3</sup>, Jichel Bea<sup>1</sup>, Mariappan Murugesan<sup>1</sup>, Hiroyuki Hashimoto<sup>1</sup>, Tadafumi Fukushima<sup>1</sup>, Tetsu Tanaka<sup>1</sup> and Mitsumasa Koyanagi<sup>1</sup> (Tohoku University<sup>1</sup>, Nagasaki Institute of Applied Science<sup>2</sup>, Association of Super-Advanced Electronics Technologies (ASET)<sup>3</sup>)
- 22-2 **(Invited) Heterogeneous 3D Stacking Technology Developments in ASET** \*\*\*\*& &  
Hiroaki Ikeda (Association of Super-Advanced Electronics Technologies (ASET))
- 22-3 **Thermal Stress and Die-Warpage Analyses of 3D Die Stacks on Organic Substrates** \*\*\*\*& \*  
Sayuri Kohara, Kuniaki Sueoka, Akihiro Horibe, Keiji Matsumoto, Fumiaki Yamada and Yasumitsu Orii (Association of Super-Advanced Electronics Technologies (ASET))
- 22-4 **Study for CMOS device characteristics affected by Ultra Thin Wafer Thinning** \*\*\*\* \$\$  
Haruo Shimamoto<sup>1</sup>, Chuichi Miyazaki<sup>1</sup>, Yoshiyuki Abe<sup>1</sup>, Shigeaki Saito<sup>1</sup>, Kosuke Kitaichi<sup>1</sup>, Shoji Yasunaga<sup>1</sup>, Kang Wook Lee<sup>2</sup>, Tetsu Tanaka<sup>2</sup> and Mitsumasa Koyanagi<sup>2</sup> (Association of Super-Advanced Electronics Technologies (ASET)<sup>1</sup>, Tohoku University<sup>2</sup>)

### 13:40-15:20 Session 23: 3-D Integration by ASET "Dream Chip Project"

Session Chair: Kenichi Takeda (Association of Super-Advanced Electronics Technologies (ASET) )  
Haruo Shimamoto (Association of Super-Advanced Electronics Technologies (ASET) )

- 23-1 **Three-dimensional Integration Scheme using Hybrid Wafer Bonding and Via-last TSV Process** \*\*\*\* \$ (   
Kenichi Takeda, Mayu Aoki, Kazuyuki Hozawa, Futoshi Furuta, Azusa Yanagisawa, Hidekazu Kikuchi, Toshio Mitsuhashi and Harufumi Kobayashi (Association of Super-Advanced Electronics Technologies (ASET) )
- 23-2 **Introduction of the automotive application of TSV device** \*\*\*\* \$ ,  
Tadashi Kamada (Association of Super-Advanced Electronics Technologies (ASET) )
- 23-3 **3D System Simulation Study of Power Integrity using Si Interposer with Distribution TSV Decoupling Capacitors** \*\*\*\* %&  
Kazuo Kohno<sup>2</sup>, Yasuhiro Kitamura<sup>1</sup>, Tadashi Kamada<sup>1</sup>, Junji Ohara<sup>1</sup>, Yutaka Akiyama<sup>2</sup>, Chihiro Ueda<sup>2</sup> and Kanji Otsuka<sup>2</sup> (Association of Super-Advanced Electronics Technologies (ASET)<sup>1</sup>, Collaborative Research Center, Meisei University<sup>2</sup>)

**15:40-16:55 Session 24: 3-D Integration by ASET "Dream Chip Project"**

Session Chair: Hiroaki Ikeda (Association of Super-Advanced Electronics Technologies (ASET) )

Tadashi Kamada (Association of Super-Advanced Electronics Technologies (ASET) )

- 24-1 **Transient Response Characteristics of Through Silicon Via in High Resistivity Silicon Interposer** \*\*\*\*\* %  
Naoya Watanabe<sup>1</sup>, Chihiro Ueda<sup>2</sup>, Fumiaki Fujii<sup>2</sup>, Yutaka Akiyama<sup>2</sup>, Katsuya Kikuchi<sup>1</sup>, Yasuhiro Kitamura<sup>3</sup>, Toshio Gomyo<sup>3</sup>, Toshikazu Ookubo<sup>3</sup>, Tetsuya Koyama<sup>3</sup>, Tadashi Kamada<sup>3</sup>, Masahiro Aoyagi<sup>1</sup> and Kanji Otsuka<sup>2</sup> (Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology (AIST)<sup>1</sup>, Collaborative Research Center, Meisei University<sup>2</sup>, Association of Super-Advanced Electronics Technologies (ASET)<sup>3</sup> )
- 24-2 **PDN Characteristics of 3D-SiP with a Wide-bus Structure under 4k-IO Operations** \*\*\*\*\* &\$  
Atsushi Sakai<sup>1</sup>, Shigeru Yamada<sup>1</sup>, Takashi Kariya<sup>1</sup>, Shiro Uchiyama<sup>1</sup>, Hiroaki Ikeda<sup>1</sup>, Haruya Fujita<sup>2</sup>, Hiroki Takatani<sup>2</sup>, Yosuke Tanaka<sup>2</sup>, Yoshiaki Oizono<sup>2</sup>, Yoshitaka Nabeshima<sup>2</sup> and Toshio Sudo<sup>2</sup> (Association of Super-Advanced Electronics Technologies (ASET)<sup>1</sup>, Shibaura Institute of Technology<sup>2</sup>)
- 24-3 **A Highly Reliable Single-Crystal Silicon RF-MEMS Switch Using Au Sub-micron Particles for Wafer Level LTCC** \*\*\*\*\* &  
**Cap Packaging**  
Takashi Katsuki<sup>1</sup>, Tadashi Nakatani<sup>1</sup>, Hisao Okuda<sup>2</sup>, Osamu Toyoda<sup>2</sup>, Satoshi Ueda<sup>1</sup> and Fuihiko Nakazawa<sup>1</sup> (Association of Super-Advanced Electronics Technologies (ASET)<sup>1</sup>, Fujitsu Laboratories Ltd.<sup>2</sup> )

**December 12, 2012**

**Room A**

**10:00-11:45 Session 25 Interconnect**

Session Chair: Yutaka Uematsu (Hitachi Ltd.)

Daisuke Iguchi (Fuji Xerox Co., Ltd.)

- 25-1 **Characterization of Signal Via Structure in Multilayer Printed Circuit Board up to 50GHz** & Taiga Fukumori and Daisuke Mizutani (Fujitsu Laboratories Ltd.)
- 25-2 **Study of the insertion loss of a differential pair of through holes for the 25Gbps serial interconnect** & Go Shinkai, Satoshi Muraoka, Masayoshi Yagu, Yutaka Uematsu and Hideki Osaka (Yokohama Research Laboratory, Hitachi Ltd.)
- 25-3 **Novel Compact Bandpass Filters for High-Density Packaging Applications** & Taras Kushta and Takashi Harada (Central Research Laboratories, NEC Corporation)

**Room B**

**10:00-11:45 Session 26: Material for Printed Wiring Board**

Session Chair: Takumi Ueno (Shinshu University)

Yutaka Nomura (Hitachi Chemical Co., Ltd.)

- 26-1 **Development of Low CHE, Negative-Tone, Photo-Definable Polyimide for HDD suspension** (\$) Masayuki Ohe<sup>1</sup>, Tomonori Minegishi<sup>2</sup>, Kawasaki Dai<sup>1</sup>, Keiko Suzuki<sup>1</sup>, Taku Konno<sup>1</sup> and Takahiro Hidaka<sup>2</sup> (Hitachi Chemical DuPont MicroSystems Ltd.<sup>1</sup>, Hitachi Chemical Co., Ltd.<sup>2</sup>)
- 26-2 **Build-up Electrical Insulation Material for High Speed & High-frequency** ( ' Tomoki Kunikawa, Toshiaki Tanaka, Hiroshi Kouyanagi and Kazutaka Shirahase (IM Project, R&D Center, Sekisui Chemical Co., Ltd.)
- 26-3 **Formation of Circuit Patterns on the Only Modification Area Using Selective Electroless Deposition** ( + Kunihiro Baba<sup>1</sup>, Masaharu Sugimoto<sup>1</sup>, Mitsuhiro Watanabe<sup>1</sup> and Tetsuo Yumoto<sup>2</sup> (Japan Surface Treatment Institute Co., Ltd.<sup>1</sup>, SANKYO KASEI Co., Ltd.<sup>2</sup>)

**Room C**

**10:00-11:45 Session 27: Component & Circuit**

Session Chair: Fukuro Koshiji (Kokushikan University)

Takashi Harada (NEC Corporation)

- 27-1 **Influence of the power-consumption at non-fundamental frequency on Passive intermodulation generation** ( % Kohei Takada, Daijiro Ishibashi and Nobuhiro Kuga (Faculty of Engineering, Yokohama National University)
- 27-2 **Influence of a foam supporter on passive intermodulation measurement using standing-wave coaxial tube method** ( ' ) Daijiro Ishibashi and Nobuhiro Kuga (Graduate school of Engineering, Yokohama National University)
- 27-3 **Fundamental Study of Direct Current Resistance Effect on Transmission Line Characteristics** ( ' )- Kaoru Hashimoto, Kazuo Kohno, Yutaka Akiyama, Chihiro Ueda and Kanji Otsuka (Collaborative Research Center, Meisei University)
- 27-4 **Investigation on the Mutual Inductance of On-Chip Transformers** ( ' ' ) Heng-Ming Hsu, Sih-Han Lai, Meng-Syun Chen and Hsien-Feng Liao (Department of Electrical Engineering, National Chung-Hsing University )

**Room S**

**10:00-11:45 Session 28: Cooling /Thermal**

Session Chair: Kishio Yokouchi (Fujitsu Interconnect Technologies Ltd.)

Atsushi Nakamura (Renesas Electronics Corporation)

28-1 **(Invited) Phase change Cooling for Energy-Efficient cooling ICT systems** \*\*\*\*\* \*

Minoru Yoshikawa, Kenichi Inaba, Arihiro Matsunaga and Hitoshi Sakamoto (NEC Corporation)

28-2 **Impact of Energy Relaxation Time on Heat Generation in Silicon with Electro-Thermal Analysis** \*\*\*\*\* +%

Tomoyuki Hatakeyama, Risako Kibushi and Masaru Ishizuka (Toyama Prefectural University)

28-3 **Investigation of Thermal Management Method for Coil and Capacitor in Automobile ECU** \*\*\*\*\* +(

Shinya Kawakita<sup>1</sup>, Shiro Yamashita<sup>1</sup>, Nobutake Tsuyuno<sup>2</sup>, Hideto Yoshinari<sup>3</sup> and Yujiro Kaneko<sup>3</sup> (Yokohama Research Lab., Hitachi Ltd.<sup>1</sup>, Hitachi Research Lab., Hitachi Ltd.<sup>2</sup>, Hitachi Automotive Systems, Ltd.<sup>3</sup>)

28-4 **Experimental Study on Thermal Performance of Loop Heat Pipes with Flat Evaporator for LSI Package** \*\*\*\*\* +,

Takeshi Shioga, Susumu Ogata and Yoshihiro Mizuno (Fujitsu Laboratories LTD.)