

# **2013 Seventh IEEE/ACM International Symposium on Networks-on-Chip**

**(NoCS 2013)**

**Tempe, Arizona, USA  
21 – 24 April 2013**



**IEEE Catalog Number: CFP13NOC-POD  
ISBN: 978-1-4673-6491-1**

## *NOCS 2013 Table of Contents*

### **Session 1: Emerging Technology: Optics, Wireless and 3D**

#### **Energy-efficient Adaptive Wireless NoCs Architecture 1**

Dominic DiTomaso, Ohio University; Avinash Kodi, Ohio University; David Matolak, Ohio University; Savas Kaya, Ohio University; Soumyasanta Laha, Ohio University; William Rayess, Ohio University

#### **PROBE: Prediction-based Optical Bandwidth Scaling for Energy-efficient NoCs 9**

Li Zhou, Ohio University; Avinash Karanth Kodi, Ohio University

#### **3D Logarithmic Interconnect: Stacking Multiple L1 Memory Dies Over Multi-Core Clusters 17**

Erfan Azarkhish, University of Bologna; Igor Loi, University of Bologna; Luca Benini, University of Bologna

#### **Leveraging the geometric properties of on-chip transmission line structures to improve interconnect performance: A case study in 65nm 19**

Shomit Das, University of Utah; Georgios Manetas, Mentor Graphics Corporation; Kenneth S. Stevens, University of Utah; Roberto Suaya, Mentor Graphics Corporation

### **Session 2: Routing Algorithms**

#### **GCA:Global Congestion Awareness for Load Balance in Networks-on-Chip 21**

Mukund Ramakrishna, Texas A&M University; Paul V. Gratz, Texas A&M University; Alexander Sprintson, Texas A&M University

#### **Headfirst Sliding Routing: A Time-Based Routing Scheme for Bus-NoC Hybrid 3-D Architecture 29**

Takahiro Kagami, Keio University; Hiroki Matsutani, Keio University; Michihiro Koibuchi, National Institute of Informatics; Hideharu Amano, Keio University

#### **A Greedy Approach for Latency-bounded Deadlock-free Routing Path Allocation for Application-specific NoCs 37**

Amit Verma, TU Muenchen; Pritpal S. Multani, TU Muenchen; Daniel Mueller-Gritschneider, TU Muenchen; Vladimir Todorov, Intel Mobile Communications GmbH; Ulf Schlichtmann, TU Muenchen

#### **A Deadlock-Free Routing Algorithm Requiring No Virtual Channel on 3D-NoCs with Partial Vertical Connections 44**

Jinho Lee, Seoul National University; Kiyoungh Choi, Seoul National University

#### **Snet, a flexible, Scalable NETWORK paradigm for manycore architectures 46**

Celine Azar, CEA LIST; Stephane Chevobbe, CEA LIST; Yves Lhuillier, CEA LIST; Jean-Philippe Diguët, Université de Bretagne Sud

### **Session 3: Fault Tolerance and Reliability**

**An NoC and Cache Hierarchy Substrate to Address Effective Virtualization and Fault-Tolerance** 48  
Mario Lodde, Universitat Politecnica de Valencia; Jose Flich, Universitat Politecnica de Valencia

**Minimal-Path Fault-Tolerant Approach Using Connection-Retaining Structure in Networks-on-Chip** 56  
Masoumeh Ebrahimi, University of Turku; Masoud Daneshtalab, University of Turku; Juha Plosila, University of Turku; Hannu Tenhunen, University of Turku

**Backward Probing Deadlock Detection for Networks-on-Chip** 64  
Yean-Ru Chen, National Taiwan University; Zi-Rong Wang, National Taiwan University; Pao-Ann Hsiung, National Chung Cheng University; Sao-Jie Chen, National Taiwan University; Meng-Hsun Tsai, National Cheng Kung University

### **Session 4: Simulation and Modeling**

**Scalable Parallel Simulation of Networks on Chip** 66  
Marcus Eggenberger, Universitat Stuttgart; Martin Radetzki, Universitat Stuttgart

**Per-Flow Delay Bound Analysis Based on a Formalized Microarchitectural Model** 74  
Xueqian Zhao, KTH Royal Institute of Technology; Zhonghai Lu, KTH Royal Institute of Technology

**An Accurate and Scalable Analytic Model for Round-Robin Arbitration in Network-on-Chip** 82  
Erik Fischer, Technische Universitat Dresden; Gerhard P. Fettweis, Technische Universitat Dresden

**Physical Planning for the Architectural Exploration of Large-Scale Chip Multiprocessors** 90  
Javier de San Pedro, Universitat Politecnica de Catalunya; Nikita Nikitin, Universitat Politecnica de Catalunya; Jordi Cortadella, Universitat Politecnica de Catalunya; Jordi Petit, Universitat Politecnica de Catalunya

### **Session 5: Potpourri**

**Accelerating Atomic Operations on GPGPUs** 92  
Sean Franey, University of Wisconsin - Madison; Mikko Lipasti, University of Wisconsin - Madison

**A Speculative Arbiter Design to Enable High-Frequency Many-VC Router in NoCs** 100  
Bo Zhao, University of Pittsburgh; Youtao Zhang, University of Pittsburgh; Jun Yang, University of Pittsburgh

**Quadrisection-Based Task Mapping on Many-Core Processors for Energy-Efficient On-Chip Communication** 108  
Nithin Michael, Cornell University; Yao Wang, Cornell University; G. Edward Suh, Cornell University; Ao Tang, Cornell University

## **Session 6: Network Architecture**

### **On Self-tuning Networks-on-Chip for Dynamic Network-Flow Dominance Adaptation 110**

Xiaohang Wang, Guangzhou Institute of Advanced Technology; Terrence Mak, The Chinese University of Hong Kong; Mei Yang, University of Nevada - Las Vegas; Yingtao Jiang, University of Nevada - Las Vegas; Masoud Daneshtalab, University of Turku; Maurizio Palesi, University of Enna

### **Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NOCs 118**

Syed Minhaj Hassan, Georgia Institute of Technology; Sudhakar Yalamanchili, Georgia Institute of Technology

### **Dynamic Traffic Distribution among Hierarchy Levels in Hierarchical Networks-on-Chip (NoCs) 126**

Ran Manevich, Technion - Israel Institute of Technology; Israel Cidon, Technion - Israel Institute of Technology; Avinoam Kolodny, Technion - Israel Institute of Technology