

2013 50th ACM/EDAC/IEEE Design Automation Conference (DAC 2013)

**Austin, Texas, USA
29 May – 7 June 2013**

Pages 1-644



**IEEE Catalog Number: CFP13DAC-PRT
ISBN: 978-1-4503-2071-9**

TABLE OF CONTENTS

MAPPING ON MULTI/MANY-CORE SYSTEMS: SURVEY OF CURRENT AND EMERGING TRENDS	1
<i>A. Singh, M. Shafique, A. Kumar, J. Henkel</i>	
WORKLOAD AND USER EXPERIENCE-AWARE DYNAMIC RELIABILITY MANAGEMENT IN MULTICORE PROCESSORS	11
<i>P. Mercati, A. Bartolini, T. Rosing, L. Benini, F. Paterna</i>	
LIVENESS EVALUATION OF A CYCLO-STATIC DATAFLOW GRAPH	17
<i>M. Benazouz, A. Mumier-Kordon, T. Hujsa, B. Bodin</i>	
DOUBLE PATTERNING LITHOGRAPHY-AWARE ANALOG PLACEMENT	24
<i>H. Chien, H. Ou, T. Chen, Y. Kuan, Y. Chang</i>	
SIMULTANEOUS ANALOG PLACEMENT AND ROUTING WITH CURRENT FLOW AND CURRENT DENSITY CONSIDERATIONS	30
<i>H. Ou, H. Chien, Y. Chang</i>	
COUPLING-AWARE LENGTH-RATIO-MATCHING ROUTING FOR CAPACITOR ARRAYS IN ANALOG INTEGRATED CIRCUITS	36
<i>K. Ho, H. Ou, Y. Chang, H. Tsao</i>	
DIGITAL-ASSISTED NOISE-ELIMINATING TRAINING FOR MEMRISTOR CROSSBAR-BASED ANALOG NEUROMORPHIC COMPUTING ENGINE	42
<i>B. Liu, M. Hu, H. Li, Z. Mao, Y. Chen, T. Huang, W. Zhang</i>	
DYNAMIC BEHAVIOR OF CELL SIGNALING NETWORKS – MODEL DESIGN AND ANALYSIS AUTOMATION	48
<i>N. Miskov-Zivanov, D. Marculescu, J. Faeder</i>	
DEFECT TOLERANCE IN NANODEVICE-BASED PROGRAMMABLE INTERCONNECTS: UTILIZATION BEYOND AVOIDANCE	54
<i>J. Cong, B. Xiao</i>	
AN EFFICIENT AND EFFECTIVE ANALYTICAL PLACER FOR FPGAS	62
<i>T. Lin, P. Banerjee, Y. Chang</i>	
THROUGHPUT-ORIENTED KERNEL PORTING ONTO FPGAS	68
<i>A. Papakonstantinou, J. Cong, D. Chen, Y. Liang, W. Hwu</i>	
MEMORY PARTITIONING FOR MULTIDIMENSIONAL ARRAYS IN HIGH-LEVEL SYNTHESIS	78
<i>Y. Wang, P. Li, P. Zhang, C. Zhang, J. Cong</i>	
BALANCING SECURITY AND UTILITY IN MEDICAL DEVICES?	86
<i>M. Rostami, W. Burleson, F. Koushanfar, A. Juels</i>	
TOWARDS TRUSTWORTHY MEDICAL DEVICES AND BODY AREA NETWORKS	92
<i>M. Zhang, A. Raghunathan, N. Jha</i>	
LOW-ENERGY ENCRYPTION FOR MEDICAL DEVICES: SECURITY ADDS AN EXTRA DESIGN DIMENSION	98
<i>J. Fan, O. Reparaz, V. Rozic, I. Verbauwhede</i>	
AGING-AWARE COMPILER-DIRECTED VLIW ASSIGNMENT FOR GPGPU ARCHITECTURES	104
<i>A. Rahimi, L. Benini, R. Gupta</i>	
EXPLOITING PROGRAM-LEVEL MASKING AND ERROR PROPAGATION FOR CONSTRAINED RELIABILITY OPTIMIZATION	110
<i>M. Shafique, S. Rehman, P. Aceituno, J. Henkel</i>	
REGIMAP: REGISTER-AWARE APPLICATION MAPPING ON COARSE-GRAINED RECONFIGURABLE ARCHITECTURES (CGRAS)	119
<i>M. Hamzeh, A. Shrivastava, S. Vrudhula</i>	
POLYHEDRAL MODEL BASED MAPPING OPTIMIZATION OF LOOP NESTS FOR CGRAS	129
<i>D. Liu, S. Yin, L. Liu, S. Wei</i>	
IMPROVING ENERGY GAINS OF INEXACT DSP HARDWARE THROUGH RECIPROCATIVE ERROR COMPENSATION	137
<i>A. Lingamneni, A. Basu, K. Palem, C. Piguet, C. Enz</i>	
EARLY PARTIAL EVALUATION IN A JIT-COMPILED, RETARGETABLE INSTRUCTION SET SIMULATOR GENERATED FROM A HIGH-LEVEL ARCHITECTURE DESCRIPTION	145
<i>H. Wagstaff, M. Gould, B. Franke, N. Topham</i>	

XDRA: EXPLORATION AND OPTIMIZATION OF LAST LEVEL CACHE FOR ENERGY REDUCTION IN DDR DRAMS	151
<i>S. Min, H. Javaid, S. Parameswaran</i>	
TOWARDS VARIATION-AWARE SYSTEM-LEVEL POWER ESTIMATION OF DRAMS: AN EMPIRICAL APPROACH	161
<i>K. Chandrasekar, C. Weis, B. Akesson, N. Wehn, K. Goossens</i>	
TEASE: A SYSTEMATIC ANALYSIS FRAMEWORK FOR EARLY EVALUATION OF FINFET-BASED ADVANCED TECHNOLOGY NODES	169
<i>A. Mallik, P. Zuber, T. Liu, B. Chava, B. Ballal, P. Bario, R. Baert, K. Croes, J. Ryckaert, M. Badaroglu, A. Mercha, D. Verkest</i>	
STITCH-AWARE ROUTING FOR MULTIPLE E-BEAM LITHOGRAPHY	175
<i>S. Fang, I. Liu, Y. Chang</i>	
AUTOMATIC DESIGN RULE CORRECTION IN PRESENCE OF MULTIPLE GRIDS AND TRACK PATTERNS	181
<i>N. Salodkar, S. Rajagopalan, S. Batterywala, S. Bhattacharya</i>	
MULTIPLE CHIP PLANNING FOR CHIP-INTERPOSER CODESIGN	187
<i>Y. Ho, Y. Chang</i>	
GPU-BASED N-DETECT TRANSITION FAULT ATPG	193
<i>K. Liao, S. Hsu, J. Li</i>	
POST-SILICON CONFORMANCE CHECKING WITH VIRTUAL PROTOTYPES	201
<i>L. Lei, F. Xie, K. Cong</i>	
ON TESTING TIMING-SPECULATIVE CIRCUITS	207
<i>F. Yuan, Y. Liu, W. Jone, Q. Xu</i>	
AN ATE ASSISTED DFD TECHNIQUE FOR VOLUME DIAGNOSIS OF SCAN CHAINS	213
<i>S. Kundu, S. Chattopadhyay, I. Sengupta, R. Kapur</i>	
PREDICTING FUTURE TECHNOLOGY PERFORMANCE	219
<i>A. Asenov, C. Alexander, C. Riddet, E. Towie</i>	
PREDICTING FUTURE PRODUCT PERFORMANCE: MODELING AND EVALUATION OF STANDARD CELLS IN FINFET TECHNOLOGIES	225
<i>V. Kleeberger, H. Graeb, U. Schlichtmann</i>	
THE ITRS DESIGN TECHNOLOGY AND SYSTEM DRIVERS ROADMAP: PROCESS AND STATUS	231
<i>A. Kahng</i>	
PROACTIVE CIRCUIT ALLOCATION IN MULTIPLANE NOCS	237
<i>A. Abousamra, A. Jones, R. Melham</i>	
A HETEROGENEOUS MULTIPLE NETWORK-ON-CHIP DESIGN: AN APPLICATION-AWARE APPROACH	247
<i>A. Mishra, O. Mutlu, C. Das</i>	
DESIGNING ENERGY-EFFICIENT NOC FOR REAL-TIME EMBEDDED SYSTEMS THROUGH SLACK OPTIMIZATION	257
<i>J. Zhan, N. Stoimenov, J. Ouyang, L. Thiele, V. Narayanan, Y. Xie</i>	
RISO: RELAXED NETWORK-ON-CHIP ISOLATION FOR CLOUD PROCESSORS	263
<i>H. Lu, G. Yan, Y. Han, B. Fu, X. Li</i>	
SMART HILL CLIMBING FOR AGILE DYNAMIC MAPPING IN MANY-CORE SYSTEMS	269
<i>M. Fattah, M. Daneshalab, P. Liljeberg, J. Plosila</i>	
HCI-TOLERANT NOC ROUTER MICROARCHITECTURE	275
<i>D. Ancajas, J. Nickerson, K. Chakraborty, S. Roy</i>	
OPTIMIZATION OF QUANTUM CIRCUITS FOR INTERACTION DISTANCE IN LINEAR NEAREST NEIGHBOR ARCHITECTURES	285
<i>A. Shafaei, M. Saeedi, M. Pedram</i>	
LEQA: LATENCY ESTIMATION FOR A QUANTUM ALGORITHM MAPPED TO A QUANTUM CIRCUIT FABRIC	291
<i>M. Dousti, M. Pedram</i>	
PARETO EPSILON-DOMINANCE AND IDENTIFIABLE SOLUTIONS FOR BIOCAD MODELING	298
<i>C. Angione, J. Costanza, P. Lio, G. Nicosia, G. Carapezza</i>	
DESIGN OF CYBERPHYSICAL DIGITAL MICROFLUIDIC BIOCHIPS UNDER COMPLETION-TIME UNCERTAINTIES IN FLUIDIC OPERATIONS	307
<i>Y. Luo, K. Chakrabarty, T. Ho</i>	
GENE MODIFICATION IDENTIFICATION UNDER FLUX CAPACITY UNCERTAINTY	314
<i>M. Yousofshahi, M. Orshansky, K. Lee, S. Hassoun</i>	

A FIELD-PROGRAMMABLE PIN-CONSTRAINED DIGITAL MICROFLUIDIC BIOCHIP	319
<i>D. Grissom, P. Brisk</i>	
BDS-MAJ: A BDD-BASED LOGIC SYNTHESIS TOOL EXPLOITING MAJORITY LOGIC DECOMPOSITION	328
<i>L. Amaru, P. Gaillardson, G. Micheli</i>	
TOWARDS OPTIMAL PERFORMANCE-AREA TRADE-OFF IN ADDERS BY SYNTHESIS OF PARALLEL PREFIX STRUCTURES	334
<i>S. Roy, M. Choudhury, R. Puri, D. Pan</i>	
SYNTHESIS OF FEEDBACK DECODERS FOR INITIALIZED ENCODERS	342
<i>K. Tu, J. Jiang</i>	
ON LEARNING-BASED METHODS FOR DESIGN-SPACE EXPLORATION WITH HIGH-LEVEL SYNTHESIS	348
<i>H. Liu, L. Carloni</i>	
RUNTIME DEPENDENCY ANALYSIS FOR LOOP PIPELINING IN HIGH-LEVEL SYNTHESIS	355
<i>M. Alle, A. Morvan, S. Derrien</i>	
A HIGH-LEVEL SYNTHESIS FLOW FOR THE IMPLEMENTATION OF ITERATIVE STENCIL LOOP ALGORITHMS ON FPGA DEVICES	365
<i>A. Nacci, V. Rana, F. Bruschi, D. Sciuto, I. Beretta, D. Atienza</i>	
CROSS-LAYER RACETRACK MEMORY DESIGN FOR ULTRA HIGH DENSITY AND LOW POWER CONSUMPTION	371
<i>Z. Sun, W. Wu, H. Li</i>	
IMPROVING THE ENERGY EFFICIENCY OF HARDWARE-ASSISTED WATCHPOINT SYSTEMS	377
<i>V. Karakostas, S. Tomic, O. Unsal, M. Nemirovsky, A. Cristal</i>	
LOW-POWER AREA-EFFICIENT LARGE-SCALE IP LOOKUP ENGINE BASED ON BINARY-WEIGHTED CLUSTERED NETWORKS	383
<i>N. Onizawa, W. Gross</i>	
REAL-TIME USE-AWARE ADAPTIVE MIMO RF RECEIVER SYSTEMS FOR ENERGY EFFICIENCY UNDER BER CONSTRAINTS	389
<i>D. Banerjee, S. Devarakond, S. Sen, A. Chatterjee</i>	
IMPROVING CHARGING EFFICIENCY WITH WORKLOAD SCHEDULING IN ENERGY HARVESTING EMBEDDED SYSTEMS	396
<i>Y. Zhang, Y. Ge, Q. Qiu</i>	
CREATION OF ESL POWER MODELS FOR COMMUNICATION ARCHITECTURES USING AUTOMATIC CALIBRATION	404
<i>S. Schurmans, D. Zhang, D. Auras, R. Leupers, G. Ascheid, X. Chen, L. Wang</i>	
A TRANSMISSION GATE PHYSICAL UNCLONABLE FUNCTION AND ON-CHIP VOLTAGE-TO-DIGITAL CONVERSION TECHNIQUE	410
<i>R. Chakraborty, C. Larnach, D. Acharyya, J. Plusquellic</i>	
RESP: A ROBUST PHYSICAL UNCLONABLE FUNCTION RETROFITTED INTO EMBEDDED SRAM ARRAY	420
<i>Y. Zheng, M. Hashemian, S. Bhunia</i>	
VERITRUST: VERIFICATION FOR HARDWARE TRUST	429
<i>J. Zhang, F. Yuan, L. Wei, Z. Sun, Q. Xu</i>	
RASTER: RUNTIME ADAPTIVE SPATIAL/TEMPORAL ERROR RESILIENCY FOR EMBEDDED PROCESSORS	437
<i>T. Li, M. Shafiqe, J. Ambrose, S. Rehman, J. Henkel, S. Parameswaran</i>	
ABCD-L: APPROXIMATING CONTINUOUS LINEAR SYSTEMS USING BOOLEAN MODELS	444
<i>A. Karthik, J. Roychowdhury</i>	
BAYESIAN MODEL FUSION: LARGE-SCALE PERFORMANCE MODELING OF ANALOG AND MIXED-SIGNAL CIRCUITS BY REUSING EARLY-STAGE DATA	453
<i>F. Wang, W. Zhang, S. Sun, X. Li, C. Gu</i>	
EFFICIENT MOMENT ESTIMATION WITH EXTREMELY SMALL SAMPLE SIZE VIA BAYESIAN INFERENCE FOR ANALOG/MIXED-SIGNAL VALIDATION	459
<i>C. Gu, E. Chiprout, X. Li</i>	
VERIFICATION OF DIGITALLY-INTENSIVE ANALOG CIRCUITS VIA KERNEL RIDGE REGRESSION AND HYBRID REACHABILITY ANALYSIS	466
<i>H. Lin, P. Li, C. Myers</i>	
MACHINE-LEARNING-BASED HOTSPOT DETECTION USING TOPOLOGICAL CLASSIFICATION AND CRITICAL FEATURE EXTRACTION	472
<i>Y. Yu, G. Lin, I. Jiang, C. Chiang</i>	

A NOVEL FUZZY MATCHING MODEL FOR LITHOGRAPHY HOTSPOT DETECTION	478
<i>S. Lin, J. Chen, J. Li, W. Wen, S. Chang</i>	
AN EFFICIENT LAYOUT DECOMPOSITION APPROACH FOR TRIPLE PATTERNING LITHOGRAPHY	484
<i>J. Kuang, E. Young</i>	
E-BLOW: E-BEAM LITHOGRAPHY OVERLAPPING AWARE STENCIL PLANNING FOR MCC SYSTEM	490
<i>B. Yu, K. Yuan, J. Gao, D. Pan</i>	
AUTOMATIC CLUSTERING OF WAFER SPATIAL SIGNATURES	497
<i>W. Zhang, X. Li, S. Saxena, A. Strojwas, R. Rutenbar</i>	
MULTIDIMENSIONAL ANALOG TEST METRICS ESTIMATION USING EXTREME VALUE THEORY AND STATISTICAL BLOCKADE	503
<i>S. Haralampos-G., P. Faubet, F. Mohamed, Y. Courant</i>	
HIGH-THROUGHPUT TSV TESTING AND CHARACTERIZATION FOR 3D INTEGRATION USING THERMAL MAPPING	510
<i>K. Dev, G. Woods, S. Reda</i>	
ON EFFECTIVE AND EFFICIENT IN-FIELD TSV REPAIR FOR STACKED 3D ICs	516
<i>L. Jiang, F. Ye, Q. Xu, K. Chakrabarty, B. Eklow</i>	
CLOUD PLATFORMS AND EMBEDDED COMPUTING – THE OPERATING SYSTEMS OF THE FUTURE	522
<i>J. Rellermeyer, S. Lee, M. Kistler</i>	
TESELLATION: REFACTORING THE OS AROUND EXPLICIT RESOURCE CONTAINERS WITH CONTINUOUS ADAPTATION	528
<i>J. Colmenares, G. Eads, S. Hofmeyr, S. Bird, M. Moreto, D. Chou, B. Gluzman, E. Roman, D. Bartolini, N. Mor, K. Asanovic, J. Kubiatowicz</i>	
THE AUTONOMIC OPERATING SYSTEM RESEARCH PROJECT – ACHIEVEMENTS AND FUTURE DIRECTIONS	538
<i>D. Bartolini, R. Cattaneo, G. Durelli, M. Maggio, M. Santambrogio, F. Sironi</i>	
ROLE OF POWER GRID IN SIDE CHANNEL ATTACK AND POWER-GRID-AWARE SECURE DESIGN	548
<i>X. Wang, W. Yueh, D. Roy, S. Narasimhan, Y. Zheng</i>	
NUMCHECKER: DETECTING KERNEL CONTROL-FLOW MODIFYING ROOTKITS BY USING HARDWARE PERFORMANCE COUNTERS	557
<i>X. Wang, R. Karri</i>	
HIGH-PERFORMANCE HARDWARE MONITORS TO PROTECT NETWORK PROCESSORS FROM DATA PLANE ATTACKS	564
<i>H. Chandrikakutty, D. Unmikrishnan, R. Tessier, T. Wolf</i>	
COMPILER-BASED SIDE CHANNEL VULNERABILITY ANALYSIS AND OPTIMIZED COUNTERMEASURES APPLICATION	570
<i>G. Agosta, A. Barenghi, M. Maggi, G. Pelosi</i>	
LIGHTING THE DARK SILICON BY EXPLOITING HETEROGENEITY ON FUTURE PROCESSORS	576
<i>Y. Zhang, L. Peng, X. Fu, Y. Hu</i>	
SIMULTANEOUS MULTITHREADING SUPPORT IN EMBEDDED DISTRIBUTED MEMORY MPSOCS	583
<i>R. Garibotti, L. Ost, R. Busseuil, M. Kourouma, C. Adeniyi-Jones, G. Sassatelli, M. Robert</i>	
APPLE: ADAPTIVE PERFORMANCE-PREDICTABLE LOW-ENERGY CACHES FOR RELIABLE HYBRID VOLTAGE OPERATION	590
<i>B. Maric, J. Abella, M. Valero</i>	
AN OPTIMIZED PAGE TRANSLATION FOR MOBILE VIRTUALIZATION	598
<i>Y. Lee, C. Hsueh</i>	
SCALABLE VECTORLESS POWER GRID CURRENT INTEGRITY VERIFICATION	604
<i>Z. Feng</i>	
CONSTRAINT ABSTRACTION FOR VECTORLESS POWER GRID VERIFICATION	612
<i>X. Xiong, J. Wang</i>	
THE IMPACT OF ELECTROMIGRATION IN COPPER INTERCONNECTS ON POWER GRID INTEGRITY	618
<i>V. Mishra, S. Sapatnekar</i>	
TINYSPICE: A PARALLEL SPICE SIMULATOR ON GPU FOR MASSIVELY REPEATED SMALL CIRCUIT SIMULATIONS	624
<i>L. Han, X. Zhao, Z. Feng</i>	

AN OPTIMAL ALGORITHM OF ADJUSTABLE DELAY BUFFER INSERTION FOR SOLVING CLOCK SKEW VARIATION PROBLEM	632
<i>J. Kim, D. Joo, T. Kim</i>	
SMART NON-DEFAULT ROUTING FOR CLOCK POWER REDUCTION	638
<i>A. Kahng, S. Kang, H. Lee</i>	
ROUTING CONGESTION ESTIMATION WITH REAL DESIGN CONSTRAINTS	645
<i>W. Liu, Y. Wei, C. Sze, C. Alpert, Z. Li, Y. Li, N. Viswanathan</i>	
SPACER-IS-DIELECTRIC-COMPLIANT DETAILED ROUTING FOR SELF-ALIGNED DOUBLE PATTERNING LITHOGRAPHY	653
<i>Y. Du, Q. Ma, H. Song, J. Shiely, G. Luk-Pat, A. Miloslavsky, M. Wong</i>	
21ST CENTURY DIGITAL DESIGN TOOLS	659
<i>W. Dally, C. Malachowsky, S. Keckler</i>	
SYSTEM ARCHITECTURE AND SOFTWARE DESIGN FOR ELECTRIC VEHICLES	665
<i>M. Lukasiewicz, S. Steinhorst, S. Andalarn, F. Sagstetter, P. Waszecki, W. Chang, M. Kauer, P. Mundhenk, S. Shanker, S. Fahmy, S. Chakraborty</i>	
MODEL-BASED DEVELOPMENT AND VERIFICATION OF CONTROL SOFTWARE FOR ELECTRIC VEHICLES	671
<i>D. Goswami, M. Lukasiewicz, M. Kauer, S. Steinhorst, A. Masrur, S. Chakraborty, S. Ramesh</i>	
HYBRID ENERGY STORAGE SYSTEMS AND BATTERY MANAGEMENT FOR ELECTRIC VEHICLES	680
<i>S. Park, Y. Kim, N. Chang</i>	
RELIABILITY CHALLENGES FOR ELECTRIC VEHICLES: FROM DEVICES TO ARCHITECTURE AND SYSTEMS SOFTWARE	686
<i>G. Georakos, U. Schlichtmann, R. Schneider, S. Chakraborty</i>	
RELIABLE ON-CHIP SYSTEMS IN THE NANO-ERA: LESSONS LEARNT AND FUTURE TRENDS	695
<i>J. Henkel, L. Bauer, N. Dutt, P. Gupta, S. Nassif, M. Shafique, M. Tahoori, N. Wehn</i>	
A LAYOUT-BASED APPROACH FOR MULTIPLE EVENT TRANSIENT ANALYSIS	705
<i>M. Ebrahimi, H. Asadi, M. Tahoori</i>	
QUANTITATIVE EVALUATION OF SOFT ERROR INJECTION TECHNIQUES FOR ROBUST SYSTEM DESIGN	711
<i>H. Cho, S. Mirkhani, C. Cher, J. Abraham, S. Mitra</i>	
EFFICIENTLY TOLERATING TIMING VIOLATIONS IN PIPELINED MICROPROCESSORS	721
<i>K. Chakraborty, B. Cozzens, S. Roy, D. Ancajas</i>	
HIERARCHICAL DECODING OF DOUBLE ERROR CORRECTING CODES FOR HIGH SPEED RELIABLE MEMORIES	729
<i>Z. Wang</i>	
POWER BENEFIT STUDY FOR ULTRA-HIGH DENSITY TRANSISTOR-LEVEL MONOLITHIC 3D ICS	736
<i>Y. Lee, D. Limbrick, S. Lim</i>	
RAPID EXPLORATION OF PROCESSING AND DESIGN GUIDELINES TO OVERCOME CARBON NANOTUBE VARIATIONS	746
<i>G. Hills, J. Zhang, C. Mackin, M. Shulaker, H. Wei, H. Wong, S. Mitra</i>	
MINIMUM-ENERGY STATE GUIDED PHYSICAL DESIGN FOR NANOMAGNET LOGIC	756
<i>S. Liu, G. Csaba, X. Hu, E. Varga, M. Niemier, G. Bernstein, W. Porod</i>	
ULTRA LOW POWER ASSOCIATIVE COMPUTING WITH SPIN NEURONS AND RESISTIVE CROSSBAR MEMORY	763
<i>M. Sharad, D. Fan, K. Roy</i>	
UNDERSTANDING THE TRADE-OFFS IN MULTI-LEVEL CELL RERAM MEMORY DESIGN	769
<i>C. Xu, D. Niu, N. Muralimanohar, N. Jouppi, Y. Xie</i>	
EXPLORING TUNNEL-FET FOR ULTRA LOW POWER ANALOG APPLICATIONS: A CASE STUDY ON OPERATIONAL TRANSCONDUCTANCE AMPLIFIER	775
<i>A. Trivedi, S. Carlo, S. Mukhopadhyay</i>	
ENERGY-OPTIMAL SRAM SUPPLY VOLTAGE SCHEDULING UNDER LIFETIME AND ERROR CONSTRAINTS	781
<i>A. Calimera, E. Macii, M. Poncino</i>	
RELAX-AND-RETIME: A METHODOLOGY FOR ENERGY-EFFICIENT RECOVERY BASED DESIGN	787
<i>S. Ramasubramanian, S. Venkataramani, A. Parandhaman, A. Raghunathan</i>	
POST-PLACEMENT VOLTAGE ISLAND GENERATION FOR TIMING-SPECULATIVE CIRCUITS	793
<i>R. Ye, F. Yuan, Z. Sun, W. Jone, Q. Xu</i>	

ANALYSIS AND CHARACTERIZATION OF INHERENT APPLICATION RESILIENCE FOR APPROXIMATE COMPUTING	799
<i>V. Chippa, S. Chakradhar, K. Roy, A. Raghunathan</i>	
DYNAMIC VOLTAGE AND FREQUENCY SCALING FOR SHARED RESOURCES IN MULTICORE PROCESSOR DESIGNS.....	808
<i>X. Chen, Z. Xu, H. Kim, P. Gratz, J. Hu, M. Kishinevsky, U. Ogras, R. Ayoub</i>	
ENERGY OPTIMIZATION BY EXPLOITING EXECUTION SLACKS IN STREAMING APPLICATIONS ON MULTIPROCESSOR SYSTEMS	815
<i>A. Singh, A. Das, A. Kumar</i>	
VERIFYING SYSTEMC USING AN INTERMEDIATE VERIFICATION LANGUAGE AND SYMBOLIC SIMULATION	822
<i>H. Le, D. Große, V. Herdt, R. Drechsler</i>	
HANDLING DESIGN AND IMPLEMENTATION OPTIMIZATIONS IN EQUIVALENCE CHECKING FOR BEHAVIORAL SYNTHESIS	828
<i>Z. Yang, K. Hao, S. Ray, F. Xie</i>	
A COUNTEREXAMPLE-GUIDED INTERPOLANT GENERATION ALGORITHM FOR SAT-BASED MODEL CHECKING.....	834
<i>C. Wu, C. Lai, C. Huang</i>	
A ROBUST CONSTRAINT SOLVING FRAMEWORK FOR MULTIPLE CONSTRAINT SETS IN CONSTRAINED RANDOM VERIFICATION.....	840
<i>B. Wu, C. Huang</i>	
SIMULATION KNOWLEDGE EXTRACTION AND REUSE IN CONSTRAINED RANDOM PROCESSOR VERIFICATION	847
<i>W. Chen, L. Wang, J. Bhadra, M. Abadir</i>	
HARDWARE-EFFICIENT ON-CHIP GENERATION OF TIME-EXTENSIVE CONSTRAINED-RANDOM SEQUENCES FOR IN-SYSTEM VALIDATION.....	853
<i>A. Kinsman, H. Ko, N. Nicolici</i>	
THE ROLE OF CASCADE, A CYCLE-BASED SIMULATION INFRASTRUCTURE, IN DESIGNING THE ANTON SPECIAL-PURPOSE SUPERCOMPUTERS.....	859
<i>J. Grossman, B. Towles, J. Bank, D. Shaw</i>	
TOWARDS STRUCTURED ASICs USING POLARITY-TUNABLE SI NANOWIRE TRANSISTORS	868
<i>P. Gaillardon, M. Marchi, L. Amaru, S. Bobba, D. Sacchetto, Y. Leblebici, G. Micheli</i>	
SACHA: THE STANFORD CARBON NANOTUBE CONTROLLED HANDSHAKING ROBOT.....	872
<i>M. Shulaker, J. Rethy, G. Hills, H. Chen, G. Gielen, H. Wong, S. Mitra</i>	
ELECTRICAL ARTIFICIAL SKIN USING ULTRAFLEXIBLE ORGANIC TRANSISTOR	875
<i>T. Sekitani, T. Sakurai, T. Yokota, T. Someya, M. Takamiya</i>	
RELAYS DO NOT LEAK – CMOS DOES.....	878
<i>H. Fariborzi, F. Chen, R. Nathanael, I. Chen, L. Hutin, R. Lee, T. Liu, V. Stojanovic</i>	
SINGLE-PHOTON IMAGE SENSORS.....	882
<i>E. Charbon, F. Regazzoni</i>	
NON-VOLATILE FPGAS BASED ON SPINTRONIC DEVICES.....	886
<i>O. Goncalves, G. Prenat, G. Pendina, B. Diény</i>	
A NOVEL ANALYTICAL METHOD FOR WORST CASE RESPONSE TIME ESTIMATION OF DISTRIBUTED EMBEDDED SYSTEMS	889
<i>J. Kim, H. Oh, J. Choi, H. Ha, S. Ha</i>	
OPTIMIZATIONS FOR CONFIGURING AND MAPPING SOFTWARE PIPELINES IN MANY CORE SYSTEMS	899
<i>J. Jahn, S. Pagani, S. Kobbe, J. Chen, J. Henkel</i>	
A SCENARIO-BASED RUN-TIME TASK MAPPING ALGORITHM FOR MPSOCS.....	907
<i>W. Quan, A. Pimentel</i>	
EARLY EXPLORATION FOR PLATFORM ARCHITECTURE INSTANTIATION WITH MULTI-MODE APPLICATION PARTITIONING	913
<i>P. Agrawal, P. Raghavan, M. Hartman, N. Sharma, L. Perre, F. Catthoor</i>	
COARX: A COPROCESSOR FOR ARX-BASED CRYPTOGRAPHIC ALGORITHMS	921
<i>K. Shahzad, A. Khalid, Z. Rakossy, G. Paul, A. Chattopadhyay</i>	
RECONFIGURABLE PIPELINED COPROCESSOR FOR MULTI-MODE COMMUNICATION TRANSMISSION	931
<i>L. Tiang, J. Ambrose, S. Parameswaran</i>	
ACCELERATORS FOR BIOLOGICALLY-INSPIRED ATTENTION AND RECOGNITION.....	939
<i>M. Park, C. Zhang, M. Debole, S. Kestur, V. Narayanan, M. Irwin</i>	

STOCHASTIC CIRCUITS FOR REAL-TIME IMAGE-PROCESSING APPLICATIONS	945
<i>A. Alaghi, C. Li, J. Hayes</i>	
AN EVENT-DRIVEN SIMULATION METHODOLOGY FOR INTEGRATED SWITCHING POWER SUPPLIES IN SYSTEMVERILOG	951
<i>J. Jang, M. Park, J. Kim</i>	
A NEW TIME-STEPPING METHOD FOR CIRCUIT SIMULATION	958
<i>G. Fang</i>	
TIME-DOMAIN SEGMENTATION BASED MASSIVELY PARALLEL SIMULATION FOR ADCS	968
<i>Z. Ye, B. Wu, S. Han, Y. Li</i>	
A DIRECT FINITE ELEMENT SOLVER OF LINEAR COMPLEXITY FOR LARGE-SCALE 3-D CIRCUIT EXTRACTION IN MULTIPLE DIELECTRICS	974
<i>B. Zhou, H. Liu, D. Jiao</i>	
FPGA CODE ACCELERATORS - THE COMPILER PERSPECTIVE	980
<i>W. Najjar, J. Villarreal</i>	
CAN CAD CURE CANCER?	986
<i>S. Krishnawarny, B. Bodenmiller, D. Pe'er</i>	
LET'S PUT THE CAR IN YOUR PHONE!	988
<i>M. Geier, M. Becker, D. Yunge, B. Dietrich, R. Schneider, D. Goswami, S. Chakraborty</i>	
THE UNDETECTABLE AND UNPROVABLE HARDWARE TROJAN HORSE	990
<i>S. Wei, M. Potkonjak</i>	
PATH TO A TERABYTE OF ON-CHIP MEMORY FOR PETABIT PER SECOND BANDWIDTH WITH < 5WATTS OF POWER	992
<i>S. Ghosh</i>	
RECONCILING REAL-TIME GUARANTEES AND ENERGY EFFICIENCY THROUGH UNLOCKED-CACHE PREFETCHING	994
<i>E. Wuerges, R. Oliveira, L. Santos</i>	
INTEGRATED INSTRUCTION CACHE ANALYSIS AND LOCKING IN MULTITASKING REAL-TIME SYSTEMS	1003
<i>H. Ding, Y. Liang, T. Mitra</i>	
PRECISE TIMING ANALYSIS FOR DIRECT-MAPPED CACHES	1013
<i>S. Andalarn, A. Girault, R. Sinha, P. Roop, J. Reineke</i>	
SSDM: SMART STACK DATA MANAGEMENT FOR SOFTWARE MANAGED MULTICORES (SMMS)	1023
<i>J. Lu, K. Bai, A. Shrivastava</i>	
TAMING THE COMPLEXITY OF COORDINATED PLACE AND ROUTE	1031
<i>J. Hu, M. Kim, I. Markov</i>	
ROUTABILITY-DRIVEN PLACEMENT FOR HIERARCHICAL MIXED-SIZE CIRCUIT DESIGNS	1038
<i>M. Hsu, Y. Chen, C. Huang, T. Chen, Y. Chang</i>	
RIPPLE 2.0: HIGH QUALITY ROUTABILITY-DRIVEN PLACEMENT VIA GLOBAL ROUTER INTEGRATION	1044
<i>X. He, T. Huang, W. Chow, J. Kuang, K. Lam, W. Cai, E. Young</i>	
OPTIMIZATION OF PLACEMENT SOLUTIONS FOR ROUTABILITY	1050
<i>W. Liu, C. Koh, Y. Li</i>	
EXPLORATION WITH UPGRADEABLE MODELS USING STATISTICAL METHODS FOR PHYSICAL MODEL EMULATION	1059
<i>B. Miller, F. Vahid, T. Givargis</i>	
MODULAR SYSTEM-LEVEL ARCHITECTURE FOR CONCURRENT CELL BALANCING	1065
<i>M. Kauer, S. Naranayaswami, S. Steinhorst, M. Lukasiewicz</i>	
A METHOD TO ABSTRACT RTL IP BLOCKS INTO C++ CODE AND ENABLE HIGH-LEVEL SYNTHESIS	1075
<i>N. Bombieri, H. Liu, F. Fummi, L. Carloni</i>	
DMR3D: DYNAMIC MEMORY RELOCATION IN 3D MULTICORE SYSTEMS	1084
<i>D. Ancajas, K. Chakraborty, S. Roy</i>	
POWER GATING APPLIED TO MP-SOCS FOR STANDBY-MODE POWER MANAGEMENT	1093
<i>D. Flynn</i>	
POWER MANAGEMENT AND DELIVERY FOR HIGH-PERFORMANCE MICROPROCESSORS	1098
<i>T. Karnik, M. Pant, S. Borkar</i>	
FLEXIBLE ON-CHIP POWER DELIVERY FOR ENERGY EFFICIENT HETEROGENEOUS SYSTEMS	1101
<i>B. Calhoun, K. Craig</i>	

POWER AND SIGNAL INTEGRITY CHALLENGES IN 3D SYSTEMS	1107
<i>M. Corbalan, A. Keval, T. Toms, D. Lisk, R. Radojicic, M. Nowak</i>	
UNDERPOWERING NAND FLASH: PROFITS AND PERILS	1111
<i>H. Tseng, L. Grupp, S. Swanson</i>	
NEW ERA: NEW EFFICIENT RELIABILITY-AWARE WEAR LEVELING FOR ENDURANCE ENHANCEMENT OF FLASH STORAGE DEVICES	1117
<i>M. Yang, Y. Chang, C. Tsao, P. Huang</i>	
SAW: SYSTEM-ASSISTED WEAR LEVELING ON THE WRITE ENDURANCE OF NAND FLASH DEVICES	1123
<i>C. Wang, W. Wong</i>	
PERFORMANCE ENHANCEMENT OF GARBAGE COLLECTION FOR FLASH STORAGE DEVICES: AN EFFICIENT VICTIM BLOCK SELECTION DESIGN	1132
<i>C. Tsao, Y. Chang, M. Yang</i>	
DURACACHE: A DURABLE SSD CACHE USING MLC NAND FLASH	1138
<i>R. Liu, C. Yang, C. Li, G. Chen</i>	
DISTRIBUTED STABLE STATES FOR PROCESS NETWORKS – ALGORITHM, ANALYSIS, AND EXPERIMENTS ON INTEL SCC	1144
<i>D. Rai, L. Schor, N. Stoimenov, L. Thiele</i>	
DISTRIBUTED RUN-TIME RESOURCE MANAGEMENT FOR MALLEABLE APPLICATIONS ON MANY-CORE PLATFORMS	1154
<i>I. Anagnostopoulos, V. Tsoutouras, A. Bartzas, D. Soudris</i>	
NETSHIP: A NETWORKED VIRTUAL PLATFORM FOR LARGE-SCALE HETEROGENEOUS DISTRIBUTED EMBEDDED SYSTEMS	1160
<i>Y. Jung, J. Park, M. Petracca, L. Carloni</i>	
EXPLOITING JUST-ENOUGH PARALLELISM WHEN MAPPING STREAMING APPLICATIONS IN HARD REAL-TIME SYSTEMS	1170
<i>J. Zhai, M. Bamakhrama, T. Stefanov</i>	
ON ROBUST TASK-ACCURATE PERFORMANCE ESTIMATION	1178
<i>Y. Xu, B. Wang, R. Hasholzner, R. Rosales, J. Teich</i>	
STOCHASTIC RESPONSE-TIME GUARANTEE FOR NON-PREEMPTIVE, FIXED-PRIORITY SCHEDULING UNDER ERRORS	1184
<i>P. Axer, R. Ernst</i>	
HADES: ARCHITECTURAL SYNTHESIS FOR HETEROGENEOUS DARK SILICON CHIP MULTI-PROCESSORS	1191
<i>Y. Turakhia, B. Raghunathan, S. Garg, D. Marculescu</i>	
HIERARCHICAL POWER MANAGEMENT FOR ASYMMETRIC MULTI-CORE IN DARK SILICON ERA	1198
<i>T. Muthukaruppan, M. Pricopi, V. Venkataramani, T. Mitra, S. Vishin</i>	
PEAK POWER REDUCTION AND WORKLOAD BALANCING BY SPACE-TIME MULTIPLEXING BASED DEMAND-SUPPLY MATCHING FOR 3D THOUSAND-CORE MICROPROCESSOR	1207
<i>S. Manoj, K. Wang, H. Yu</i>	
TECHNIQUES FOR ENERGY-EFFICIENT POWER BUDGETING IN DATA CENTERS	1213
<i>X. Zhan, S. Reda</i>	
TEMPERATURE AWARE THREAD BLOCK SCHEDULING IN GPGPUS	1220
<i>R. Nath, R. Ayoub, T. Rosing</i>	
VAWOM: TEMPERATURE AND PROCESS VARIATION AWARE WEAROUT MANAGEMENT IN 3D MULTICORE ARCHITECTURE	1226
<i>H. Tajik, H. Hornayoun, N. Dutt</i>	
ON THE POTENTIAL OF 3D INTEGRATION OF INDUCTIVE DC-DC CONVERTER FOR HIGH-PERFORMANCE POWER DELIVERY	1234
<i>S. Carlo, W. Yueh, S. Mukhopadhyay</i>	
FULL-CHIP MULTIPLE TSV-TO-TSV COUPLING EXTRACTION AND OPTIMIZATION IN 3D ICS	1242
<i>T. Song, C. Liu, Y. Peng, S. Lim</i>	
AN ACCURATE SEMI-ANALYTICAL FRAMEWORK FOR FULL-CHIP TSV-INDUCED STRESS MODELING	1249
<i>Y. Li, D. Pan</i>	
SPEEDING UP COMPUTATION OF THE MAX/MIN OF A SET OF GAUSSIANS FOR STATISTICAL TIMING ANALYSIS AND OPTIMIZATION	1257
<i>V. Kuruvilla, D. Sinha, J. Piaget, C. Visweswariah, N. Chandrachoodan</i>	

INTIMEFIX: A LOW-COST AND SCALABLE TECHNIQUE FOR IN-SITU TIMING ERROR MASKING IN LOGIC CIRCUITS	1264
<i>F. Yuan, Q. Xu</i>	
IMPROVING PUF SECURITY WITH REGRESSION-BASED DISTILLER	1270
<i>C. Yin, G. Qu</i>	
ON THE CONVERGENCE OF MAINSTREAM AND MISSION-CRITICAL MARKETS	1276
<i>S. Girbal, M. Moreto, A. Grasset, J. Abella, E. Quinones, F. Cazorla, S. Yehia</i>	
Author Index	