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5-3 - 16:40
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5-4 - 17:05
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SESSION 6 - Technology Focus Session - 3D and Emerging Memory [Shunju II]
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Chairpersons: H.-T. Lue, Macronix International Co., Ltd.
J. Zahurak, Micron Technology Inc.

6-1 - 15:50 (Invited)
Bit Cost Scalable (BiCS) Technology for Future Ultra High Density Storage Memories, A. Nitayama and H. Aochi, Center for Semiconductor Research & Development, Semiconductor & Storage Products Company, Toshiba Corp., Japan

6-2 - 16:15 (Invited)
Comprehensive Understanding of Conductive Filament Characteristics and Retention Properties for Highly Reliable ReRAM, S. Muraoka*, T. Ninomiya, Z. Wei, K. Katayama, R. Yasuhara, and T. Takagi, Automotive & Industrial Systems Company*, Panasonic Corp., Japan

6-3 - 16:40
Enhancement of Switching Margin by Utilizing Superior Pinned Layer Stability for Sub-20nm Perpendicular STT-MRAM, W.C. Lim, Y.J. Lee, J.M. Lee, W.K. Kim, J.H. Kim, K.W. Kim, K.S. Kim, Y.S. Park, H.J. Shin, S.H. Park, J.H. Kim, J.H. Jeong, M.A. Kang, Y.H. Kim, W.J. Kim, S.Y. Kim, Y.C. Cho, H.L. Park, H.S. Ahn, J.H. Park, S.C. Oh, S.O. Park, S. Jeong, S.W. Nam, H.K. Kang and E.S. Jung, Samsung Electronics Co., Ltd., Korea

6-4 - 17:05
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Circuits SESSION 1 - Welcome Session [Shunju I, II]
Wednesday, June 12, 8:30-8:45
Chairpersons: H. Kabuo, Panasonic Corp.
J. Gealow, Analog Devices, Inc.

1-1 - 8:30
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M. Nagata, Kobe Univ.
V. De, Intel Corp.

Executive Panel "Message for the Future of VLSI" [Shunju I, II]
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C. Sodini, Massachusetts Institute of Technology

Panelists: S. Kohyama
T. Sugano
B. Brodersen
D. Buss

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V. Chandra, ARM

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3-3 - 11:20
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3-4 - 11:45
A 0.9 pJ/bit, 12.8 GByte/s WideIO Memory Interface in a 3D-IC NoC-Based MPSoC, D. Dutoit*, C. Bernard*, S. Chéramy*, F. Clermidy*, Y. Thonnart*, P. Vivet*, C. Freund**, V. Guérin**, S. Guilhot**, S. Lecomte**, G. Qualizza**, J. Pruvost***, Y. Dodo***, N. Hotelier*** and J. Michailos***, *CEA, Leti, Minatec, **ST-Ericsson and ***STMicrolectronics, France

3-5 - 12:10
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Chairpersons: M. Masahara, AIST
T. Skotnicki, STMicroelectronics

7-1 - 10:30
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7-3 - 11:20
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7-4 - 11:45
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7-5 - 12:10
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SESSION 8 - ReRAM 1 [Shunju II]
Wednesday, June 12, 10:30-12:35
Chairpersons: N. Kasai, Tohoku Univ.
M. Jurczak, imec

8-1 - 10:30
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8-2 - 10:55
A Novel High Performance WO$_x$ ReRAM Based on Thermally-Induced SET Operation, W.-C. Chien, M.-H. Lee, F.-M. Lee, W.-C. Chen, D.-Y. Lee, Y.-Y. Lin, E.-K. Lai, H.-L. Lung, K.-Y. Hsieh and C.-Y. Lu, Macronix International Co., Ltd., Taiwan

8-3 - 11:20
Reliability Significant Improvement of Resistive Switching Memory by Dynamic Self-Adaptive Write Method, Y.L. Song*, Y. Meng*, X.Y. Xue*, F.J. Xiao*, Y. Liu*, B. Chen*, Y.Y. Lin*, Q.T. Zou**, R. Huang** and J.G. Wu**, *Fudan Univ. and **Semiconductor Manufacturing International Corp., China

8-4 - 11:45
A Novel Conducting Bridge Resistive Memory Using a Semiconducting Dynamic E-Field Moderating Layer, F.M. Lee, Y.Y. Lin, W.C. Chien, D.Y. Lee, M.H. Lee, W.C. Chen, H.L. Lung, K.Y. Hsieh and C.Y. Lu, Macronix International Co., Ltd., Taiwan

8-5 - 12:10
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Technology / Circuits Jumbo Joint Focus Session 1 - Design Enablement [Shunju I]
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Chairpersons: K. Kobayashi, Kyoto Institute of Technology
G. Yeap, Qualcomm Inc.

JJ1-1- 13:55 (Invited)
Enabling Circuit Design Using FinFETs through Close Ecosystem Collaboration, B.J. Sheu*, C.-S. Chang*, Y.-H. Chen*, K. Wang*, K.-J. Chen*, Y.-C. Peng*, L.-C. Tien*, M.-H. Song*, C. Hou*, J.Y.-C. Sun* and C. Hu**, *TSMC, Taiwan and **Univ. of California, USA

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JJ1-3 - 14:45
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JJ1-4 - 15:10
Process and Local Layout Effect Interaction on a High Performance Planar 20nm CMOS, F. Sato*, R. Ramachandran*, H.Van Meer**, K.H. Cho***, A. Ozbek*, X. Yang**, Y. Liu**, Z. Li*, X. Wu**, S. Jain*, H. Utomo*, U. Kwon*, Y. Park***, W.L. Tan**, X. Dai**, W. Lai*, J. Kim***, D. Jones**, M. Ganz**, D.H. Bae***, R. Lallement****, S.C. Vemula**, T. Kwon**, P. Lee**, Y. Qi**, M. Weybright*, A. Scholze*, R. Bingert****, J. King*, M. Sherony*, M. Eller**, H. Shang*, K. Tabakman*, V. Narayanan*, S. Samavedam** and R. Divakaruni*, *IBM Microelectronics, **GLOBALFOUNDRIES, ***Samsung Electronics and ****STMicroelectronics, USA

JJ1-5 - 15:35
0.5V Image Processor with 563 GOPS/W SIMD and 32bit CPU Using High Voltage Clock Distribution (HVCD) and Adaptive Frequency Scaling (AFS) with 40nm CMOS, M. Nomura*, A. Muramatsu*, H. Takeno*, S. Hattori*, D. Ogawa*, M. Nasu*, K. Hirairi*, S. Kumashiro*, S. Moriwaki*, Y. Yamamoto*, S. Miyano*, Y. Hiraku*, I. Hayashi*, K. Yoshioka**, A. Shikata**, H. Ishikuro**, M. Ahn***, Y. Okuma*, X. Zhang***, Y. Ryu*, K. Ishida***, M. Takamiya***, T. Kuroda**, H. Shinohara* and T. Sakurai***, *Semiconductor Technology Academic Research Center (STARC), **Keio Univ. and ***The Univ. of Tokyo, Japan

Chairpersons: K. Miyashita, Toshiba Corp.
G. Lehmann, Infineon Technologies AG

JJ1-6- 16:10 (Invited)
Design for ESD Protection at Its Limits, H. Gossner, Intel Mobile Communications Group, Germany

JJ1-7 - 16:35
Application of Low-Noise TIA ICs for Novel Sensing of MOSFET Noise up to the GHz Region, K. Ohmori*,**, R. Hasunuma*,**, S. Yamamoto***, Y. Tamura***, H. Jiang****, N. Ishihara****, K. Masu**** and K. Yamada*,**, *Univ. of Tsukuba, **JST-CREST, ***D-Clue Technologies and ****Tokyo Institute of Technology, Japan

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First Demonstration of a Full 28nm High-k/Metal Gate Circuit Transfer from Bulk to UTBB FDSOI Technology through Hybrid Integration, D. Golanski*, P. Fonteneau*, C. Fenouillet-Beranger**,*, A. Cros*, F. Monsieur, N. Guitard*, C.-A. Legrand*, A. Dray*, C. Richier*, H. Beckrich*, P. Mora*, G. Bidal, O. Weber**,*, O. Saxod*, J.-R. Manouvrier*, P. Galy*, N. Planes* and F. Arnaud*, *ST Microelectronics and **CEA-LETI MINATEC, France

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2.6GHz Ultra-Wide Voltage Range Energy Efficient Dual A9 in 28nm UTBB FD-SOI, D. Jacquet, G. Cesana, P. Flatresse, F. Arnaud, P. Menut, F. Hasbani, T. Di Gilio, C. Lecocq, T. Roy, A.Chhabra, C. Grover, O. Minez, J. Uginet, G. Durieu, F. Nyer, C. Adobati, R. Wilson and D. Casalotto, STMicroelectronics, France

SESSION 9 - PCRAM and MRAM [Shunju II]
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Chairpersons: J. S. Roh, SK hynix, Inc.
K. Attenborough, NXP Central R&D

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Charge Injection Super-Lattice Phase Change Memory for Low Power and High Density Storage Device Applications, N. Takaura*, T. Ohyanagi*, M. Kitamura*, M. Tai*, M. Kinoshita*, K. Akita*, T. Morikawa*, S. Kato**, M. Araidai**, K. Kamiya**, T. Yamamoto** and K. Shiraishi**, *Low-power Electronics Association & Project and **Univ. of Tsukuba, Japan

9-2 - 14:20
A Scalable Volume-Confined Phase Change Memory Using Physical Vapor Deposition, S.C. Lai*, S. Kim**, M. BrightSky**, Y. Zhu**, E. Joseph**, R. Bruce**, H.Y. Cheng*, A. Ray**, S. Raoux**, J.Y. Wu*, T.Y. Wang*, N.Sosa Cortes**, C.M. Lin*, Y.Y. Lin*, R. Cheek**, E.K. Lai*, M.H. Lee*, H.L. Lung* and C. Lam**, *Macronix International Co., Ltd., Taiwan and **IBM T. J. Watson Research Center, USA

9-3 -14:45
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9-4 - 15:10
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9-5 - 15:35
Low-Current Domain Wall Motion MRAM with Perpendicularly Magnetized CoFeB/MgO Magnetic Tunnel Junction and Underlying Hard Magnets, T. Suzuki*, H. Tanigawa*, Y. Kobayashi*, K. Mori*, Y. Ito*, Y. Ozaki*, K. Suemitsu*, T. Kitamura*, K. Nagahara*, E. Kariyada*, N. Ohshima*, S. Fukami**, M. Yamanouchi**, S. Ikeda**, M. Hayashi***, M. Sakao* and H. Ohno**, *Renesas Electronics Corp., **Tohoku Univ. and ***National Institute for Materials Science, Japan

SESSION 10 - More than Moore [Suzaku I, II]
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Chairpersons: Y. Nakao, Rohm Co., Ltd.
W. Maszara, GLOBALFOUNDERIES

10-1 - 16:10
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10-2 - 16:35
Scaling Strategy for Low Power RF Applications with Multi Gate Oxide Dual Work Function (DWF) MOSFETs Utilizing Self-Aligned Integration Scheme, T. Miyata, S. Kawanaka, A. Hokazono, T. Ohguro and Y. Toyoshima, Toshiba Corp., Japan

10-3 - 17:00
Time of Flight Image Sensor with 7µm Pixel and 640x480 Resolution, S. Kim, S. Cha, H. Park, J. Gong, Y. Noh, W. Kim, S. Lee, D.-K. Min, W. Kim, T.-C. Kim and E. Jung, Samsung Electronics Co., Ltd., Korea

10-4 - 17:25
A MEMS-Based Charge Pump, Y. Lin, W.-C. Li and C.T.-C. Nguyen, Univ. of California, USA

SESSION 11 - NAND and 3D NVM [Shunju II]
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J. Alsmeier, SanDisk

11-1 - 16:10
A Novel Bit Alterable 3D NAND Flash Using Junction-Free P-Channel Device with Band-to-Band Tunneling Induced Hot-Electron Programming, H.-T. Lue, K.-P. Chang, C.-P. Chen, T.-H. Yeh, T.-H. Hsu, P.-Y. Du, Y.-H. Shih and C.-Y. Lu, Macronix International Co., Ltd., Taiwan

11-2 - 16:35
A New Read Method Suppressing Effect of Random Telegraph Noise in NAND Flash Memory by Using Hysteretic Characteristic, M.-K. Jeong*, S.-M. Joe*, H.-J. Kang*, K.-R. Han**, G. Cho**, S.-K. Park**, B.-G. Park* and J.-H. Lee*, *Seoul National Univ. and **SK hynix Inc., Korea

11-3 - 17:00
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11-4 - 17:25
3D Vertical RRAM – Scaling Limit Analysis and Demonstration of 3D Array Operation, S. Yu*, H.-Y. Chen*, Y. Deng**, B. Gao**, Z. Jiang*, J. Kang** and H.-S. P. Wong*, *Stanford Univ., USA and **Beijing Univ., China

SESSION 12 - ReRAM 2 [Shunju II]
Thursday, June 13, 8:30-10:10
Chairpersons: K. Tateiwa, Panasonic Corp.
C. Mazure, Soitec Group

12-1 - 8:30
Understanding of the Intrinsic Characteristics and Memory Trade-Offs of Sub-µA Filamentary RRAM Operation, L. Goux*, A. Fantini*, R. Degraeve*, N. Raghavan*,**, R. Nigon*, S. Strangio*, G. Kar*, D.J. Wouters*,**, Y.Y. Chen*,**, M. Komura***, F.De Stefano**, V.V. Afanas'ev** and M. Jurczak*, *imec, ** KU Leuven and ***Toshiba Corp., Belgium

12-2 - 8:55
RTN Insight to Filamentary Instability and Disturb Immunity in Ultra-Low Power Switching HfO_x and AlO_x RRAM, N. Raghavan*,**, R. Degraeve*, L. Goux*, A. Fantini*,**, D.J. Wouters*,**, G. Groeseneken*,** and M. Jurczak*, *imec and **KU Leuven, Belgium

12-3 - 9:20
Self-Rectifying Bipolar TaO_x/TiO_2 RRAM with Superior Endurance Over 10^{12} Cycles for 3D High-Density Storage-Class Memory, C.-W. Hsu*, I.-T. Wang*, C.-L. Lo*, M.-C. Chiang**, W.-Y. Jang**, C.-H. Lin** and T.-H. Hou*, *National Chiao Tung Univ. and **Winbond Electronics Corp., Taiwan

12-4 - 9:45
Multi-Layer Tunnel Barrier ($Ta_2O_5/TaO_x/TiO_2$) Engineering for Bipolar RRAM Selector Applications, J. Woo*, W. Lee**, S. Park,** S. Kim**, D. Lee*, G. Choi*, E. Cha*, J.H. Lee*, W.Y. Jung*, C.G. Park* and H. Hwang*, *Pohang Univ. of Sci. and Tech. (POSTECH) and **Gwangju Institute of Sci. and Tech. (GIST), Korea

Circuits SESSION 9 - Technology / Circuits Joint Focus Session - Emerging Memories [Shunju I]
Thursday, June 13, 10:30-12:35
Chairpersons: R. Takemura, Hitachi, Ltd.
F. Hamzaoglu, Intel Corp.

9-1 - 10:30
1Mb 0.41 µm² 2T-2R Cell Nonvolatile TCAM with Two-Bit Encoding and Clocked Self-Referenced Sensing, J. Li*, R. Montoye*, M. Ishii**, K. Stawiasz*, T. Nishida***, K. Maloney****, G. Ditlow*, S. Lewis****, T. Maffitt****, R. Jordan****, L. Chang* and P. Song*, *IBM T. J. Watson Research Center, USA, **IBM Tokyo Research Lab, ***IBM Japan Services Company Ltd., Japan and ****IBM Burlington, USA

9-2 - 10:55
Fabrication of a 99%-Energy-Less Nonvolatile Multi-Functional CAM Chip Using Hierarchical Power Gating for a Massively-Parallel Full-Text-Search Engine, S. Matsunaga*, N. Sakimura**, R. Nebashi**, Y. Tsuji**, A. Morioka**, T. Sugibayashi**, S. Miura**, H. Honjo**, K. Kinoshita*, H. Sato*, S. Fukami*, M. Natsui*, A. Mochizuki*, S. Ikeda*, T. Endoh*, H. Ohno* and T. Hanyu*, *Tohoku Univ. and **NEC Corp., Japan

9-3 - 11:20
A 250-MHz 256b-I/O 1-Mb STT-MRAM with Advanced Perpendicular MTJ Based Dual Cell for Nonvolatile Magnetic Caches to Reduce Active Power of Processors, H. Noguchi, K. Kushida, K. Ikegami, K. Abe, E. Kitagawa, S. Kashiwada, C. Kamata, A. Kawasumi, H. Hara and S. Fujita, Toshiba Corp., Japan

9-4 - 11:45
A 1.5nsec/2.1nsec Random Read/Write Cycle 1Mb STT-RAM Using 6T2MTJ Cell with Background Write for Nonvolatile e-Memories, T. Ohsawa*, S. Miura**, K. Kinoshita*, H. Honjo**, S. Ikeda*, T. Hanyu*, H. Ohno* and T. Endoh*, *Tohoku Univ. and **NEC Corp., Japan

9-5 - 12:10
Area-Efficient Embedded RRAM Macros with Sub-5ns Random-Read-Access-Time Using Logic-Process Parasitic-BJT- Switch (0T1R) Cell and Read-Disturb-Free Temperature-Aware Current-Mode Read Scheme, M.-F. Chang*, C.-C. Kuo*, S.-S. Sheu**, C.-J. Lin*, Y.-C. King*, Z.-H. Lin**, K.-L. Su**, Y.-S. Chen**, W.-P. Lin**, H.-Y. Lee**, C.-H. Tsai**, W.-S. Chen**, F.T. Chen**, T.-K. Ku**, M.-J. Kao**, M.-J. Tsai**, J.-J. Wu*,***, Y.-D. Chih*** and S. Natarajan***, *National Tsing Hua Univ., **ITRI and ***TSMC, Taiwan

SESSION 13 - RTN [Suzaku III]
Thursday, June 13, 10:30-12:10
Chairpersons: S. Yamakawa, Sony Corp.
M. Mehrotra, Texas Instruments, Inc.

13-1 - 10:30
Experimental Study of Channel Doping Concentration Impacts on Random Telegraph Signal Noise and Successful Noise Suppression by Strain Induced Mobility Enhancement, J. Chen, Y. Higashi, I. Hirano and Y. Mitani, Toshiba Corp., Japan

13-2 - 10:55
Deep Understanding of AC RTN in MuGFETs through New Characterization Method and Impacts on Logic Circuits, J. Zou*, R. Wang*, M. Luo*, R. Huang*, N. Xu**, P. Ren*, C. Liu*, W. Xiong***, J. Wang****, J. Liu****, J. Wu****, W. Wong****, S. Yu****, H. Wu****, S.-W. Lee**** and Y. Wang*, *Beijing Univ., China, **Univ. of California, USA, ***AMD GmbH, Germany and ****Semiconductor Manufacturing International Corp. (SMIC), China

13-3 - 11:20
RTN Induced Frequency Shift Measurements Using a Ring Oscillator Based Circuit, Q. Tang*, X. Wang*, J. Keane** and C.H. Kim*, *Univ. of Minnesota and **Intel Corp., USA

13-4 - 11:45
Degradation of Time Dependent Variability Due to Interface State Generation, M. Toledano-Luque*, B. Kaczer*, J. Franco*, P.J. Roussel*, M. Bina**, T. Grasser**, M. Cho*, P. Weckx*.*** and G. Groeseneken*.***, *imec, Belgium, **TUWien, Austria and ***KU Leuven, Belgium

SESSION 14 - Process Technology [Shunju II]
Thursday, June 13, 10:30-12:35
Chairpersons: S. Choi, Samsung Electronics Co., Ltd.
C.-P. Chang, Applied Materials, Inc.

14-1 - 10:30
Highly Scalable Effective Work Function Engineering Approach for Multi-V_T Modulation of Planar and FinFET-Based RMG High-k Last Devices for (Sub-)22nm Nodes, A. Veloso*, G. Boccardi*, L.-Å. Ragnarsson*, Y. Higuchi**, J.W. Lee***, E. Simoen*, P.J. Roussel*, M.J. Cho,* S.A. Chew*, T. Schram*, H. Dekkers*, A.Van Ammel*, T. Witters*, S. Brus*, A. Dangol*, V. Paraschiv*, E. Vecchio*, X. Shi*, F. Sebaai*, K. Kellens*, N. Heylen*, K. Devriendt*, O. Richard*, H. Bender*, T. Chiarella*, H. Arimura***, A. Thean* and N. Horiguchi*, *imec, **Panasonic Corp. and ***KU Leuven, Belgium

14-2 - 10:55
Heated Implantation with Amorphous Carbon CMOS Mask for Scaled FinFETs, M. Togo*, Y. Sasaki*, G. Zschätzsch**, G. Boccardi*, R. Ritzenthaler*, J.W. Lee*, F. Khaja***, B. Colombeau***, L. Godet***, P. Martin***,S. Brus*, S.E. Altamirano*, G. Mannaert*, H. Dekkers*, G. Hellings*, N. Horiguchi*, W. Vandervorst* and A. Thean*, *imec, **KU Leuven, Belgium and **Applied Materials, USA

14-3 - 11:20
NFET Effective Work Function Improvement via Stress Memorization Technique in Replacement Metal Gate Technology, Y. Liu*, H.V. Meer*, O. Gluschenkov**, X. Yang*, F. Sato**, K.H. Cho***, M. Ganz*, H. Utomo**, Y. Wang**, U. Kwon**, H. Kothari****, W. Mcmahon*, S. Uppal*, M. Jin***, C. Tian**, W. Lai**, R. Ramachandran**, E. Josse****, S. Jain**, V. Narayanan**, M. Eller*, S. Samavedam*, H. Shang** and R. Divakaruni**, *GLOBALFOUNDRIES, **IBM Microelectronics, ***Samsung Electronics and ****STMicroelectronics, USA

14-4 - 11:45
Barrier Height Reduction to 0.15eV and Contact Resistivity Reduction to 9.1×10^{-9} Ω-cm² Using Ultrathin TiO_{2-x} Interlayer between Metal and Silicon, A. Agrawal*, J. Lin*, B. Zheng**, S. Sharma**, S. Chopra**, K. Wang*, A. Gelatos**, S. Mohney*and S. Datta*, *The Pennsylvania State Univ. and **Applied Materials, USA

14-5 - 12:10
64nm Pitch Interconnects: Optimized for Designability, Manufacturability and Extendibility, C. Goldberg* , S.H. Park**, B.Y. Kim*, S.B. Law***, B. Hamieh*, J. Jung**, B.H. Kim**, S.H. Rhee***, M. Oh***, M. Mobley***, E. Laffosse***, A. Kim****, A. Thomas****, P. Malinge*, T.Fryxell***, K.J. Lim**, I.S. Park**, B. Bahierathan*, F. Wu***, B. Erenturk***, W.C. Jeon**, H.C. Choi**, Y.J. Park**, H.Kim**, T.Q. Chen***, S. Thibaut*, C. Niu*, J. Zhang*, R. Filippi****, E. Kaltalioglu****, R. Achanta****, P.-C. Wang****, H. Yang*, J.P. Geronimi*, F. Pagette***, V. Chauhan***, A. Ogino****, R. Srivastava***, R. Koshy***, F. Baumann****, A. Simon****, J. Nag****, T. Cheng****, J.Fitzsimmons****, W. Tseng****, Y. Lin***, Z. Sun***, T. Bolom***, T.-M. Ko****, L. Clevenger****, J. Kim**, J. Sudijono*** and R. Sampson*, *STMicroelectronics, **Samsung Electronics, ***GLOBALFOUNDRIES and ****IBM Microelectronics, USA

Luncheon Talk [Suzaku II]
Thursday, June 13, 12:45-14:05
Organizer: H. Kabuo, Panasonic Corp.

Symbiosis with Lightning Which Is One of the Most Spectacular Natural Phenomenon, T. Kudo, Otowa Electric Co., Ltd., Japan

Technology / Circuits Jumbo Joint Focus Session 2 - SRAM [Shunju I]
Thursday, June 13, 14:20-18:20
Chairpersons: T. Tanaka, Fujitsu Semiconductor Ltd.
S. Sridhara, Texas Instruments

JJ2-1- 14:20 (Invited)
Fully-Depleted Planar Technologies and Static RAM, T. Hook*, K. Cheng**, B. Doris**, A. Khakifirooz**, Q. Liu****, S. Ponoth**, C. Radens*** and M. Vinet*****, *IBM SRDC, **IBM Albany, ***IBM East Fishkill, ****STMicroelectronics, *****LETI, USA

JJ2-2 - 14:45
A 20nm 0.6V 2.1μW/MHz 128kb SRAM with No Half Select Issue by Interleave Wordline and Hierarchical Bitline Scheme, H. Fujiwara, M. Yabuuchi, M. Morimoto, K. Tanaka, M. Tanaka, N. Maeda, Y. Tsukamoto and K. Nii, Renesas Electronics Corp., Japan

JJ2-3 - 15:10
FDSOI Process/Design Full Solutions for Ultra Low Leakage, High Speed and Low Voltage SRAMs, R. Ranica*, N. Planes*, O. Weber**, O. Thomas**, S. Haendler*, D. Noblet*, D. Croain*, C. Gardin* and F. Arnaud*, *STMicroelectronics and **CEA, LETI, MINATEC, France

JJ2-4 - 15:35
Ultralow-Voltage Operation of Silicon-on-Thin-BOX (SOTB) 2Mbit SRAM Down to 0.37 V Utilizing Adaptive Back Bias, Y. Yamamoto*, H. Makiyama*, H. Shinohara*, T. Iwamatsu*, H. Oda*, S. Kamohara*, N. Sugii*, Y. Yamaguchi*, T. Mizutani** and T. Hiramoto**, *Low-power Electronics Association & Project (LEAP) and **The Univ. of Tokyo, Japan

Chairpersons: H. Yamauchi, Fukuoka Institute of Technology
J. Cheek, Freescale

JJ2-5- 16:15 (Invited)
Enhancing SRAM Performance by Advanced FinFET Device and Circuit Technology Collaboration for 14nm Node and Beyond, K. Endo, S. O'uchi, T. Matsukawa, Y. Liu, K. Sakamoto, W. Mizubayashi, S. Migita, Y. Morita, H. Ota, E. Suzuki and M. Masahara, Nanoelectronics Research Institute, National Institute of Advanced Industrial Sci. and Tech., Japan

JJ2-6 - 16:40
Dual-V_{CC} 8T-Bitcell SRAM Array in 22nm Tri-Gate CMOS for Energy-Efficient Operation across Wide Dynamic Voltage Range, J. Kulkarni, M. Khellah, J. Tschanz, B. Geuskens, R. Jain, S. Kim and V. De, Intel Corp., USA

JJ2-7 - 17:05
A 10 nm Si-Based Bulk FinFETs 6T SRAM with Multiple Fin Heights Technology for 25% Better Static Noise Margin, M.-C. Chen*, C.-H. Lin*, Y.-F. Hou*, Y.-J. Chen*, C.-Y. Lin*, F.-K. Hsueh*, H.-L. Liu*, C.-T. Liu*, B.-W. Wang**, H.-C. Chen*, C.-C. Chen*, S.-H. Chen*, C.-T. Wu*, T.-Y. Lai*, M.-Y. Lee*, B.-W. Wu*, C.-S. Wu*, I. Yang*, Y.-P. Hsieh***, C.H. Ho*, T. Wang**, A.B. Sachid****, C. Hu**** and F.-L. Yang*, *National Nano Device Labs. (NDL), **National Chiao-Tung Univ., ***National Cheng Kung Univ., Taiwan and ****UC Berkeley, USA

JJ2-8 - 17:30
A 210mV 7.3MHz 8T SRAM with Dual Data-Aware Write-Assists and Negative Read Wordline for High Cell-Stability, Speed and Area-Efficiency, C.-F. Chen*, T.-H. Chang*, L.-F. Chen*, M.-F. Chang* and H. Yamauchi**, *National Tsing Hua Univ., Taiwan and **Fukuoka Institute of Technology, Japan

JJ2-9 - 17:55
A 22nm 2.5MB Slice On-Die L3 Cache for the Next Generation Xeon® Processor, W. Chen, S.-L. Chen, S. Chiu, R. Ganesan, V. Lukka, W.W. Mar and S. Rusu, Intel Corp., USA

SESSION 15 - Nanowire [Shunju II]
Thursday, June 13, 14:20-16:00
Chairpersons: B.H. Lee, Gwangju Institute of Sci. and Tech.
B.-K. Liew, nVidia

15-1 - 14:20
Innovative Through-Si 3D Lithography for Ultimate Self-Aligned Planar Double-Gate and Gate-All-Around Nanowire Transistors, R. Coquand*,**,***, S. Monfray*, S. Barraud**, M.P. Samson*,**, C. Arvet*,**, J. Pradelles**, J. Bustos*,**, L. Martin**, L. Tosti**, P. Perreau**, J.M. Hartmann**, J. Lacord*, M. Cassé**, L. Clement*, A. Pofelski*, K. Lepinay*, G. Ghibaudo***, O. Faynot**, T. Poiroux**, F. Boeuf*, T. Skotnicki* and B. De Salvo**, *STMicroelectronics, **CEA, LETI, Minatec and ***IMEP-LAHC, France

15-2 - 14:45
Systematic Understanding of Channel-Size Dependence of Low-Frequency Noise in 10nm-Diameter Tri-Gate Nanowire MOSFETs, M. Saitoh, K. Ota, C. Tanaka and T. Numata, Toshiba Corp., Japan

15-3 - 15:10
Scaling of Ω-Gate SOI Nanowire N- and P-FET Down to 10nm Gate Length: Size- and Orientation-Dependent Strain Effects, S. Barraud*, R. Coquand*,***,****, V. Maffini-Alvaro*, M.-P. Samson***, J.-M. Hartmann*, L. Tosti*, M. Cassé*, V.-H. Nguyen**, F. Triozon*, Y.-M. Niquet**, C. Tabone*, P. Perreau, F. Allain*, C. Vizioz*, C. Comboroure*,***, F. Aussenac*, S. Monfray***, G. Ghibaudo****, F. Boeuf***, B.De Salvo* and O. Faynot*, *CEA, LETI, **CEA, INAC, MINATEC, ***STMicroelectronics and ****IMEP-LAHC, France

15-4 - 15:35
Performance of GAA Poly-Si Nanosheet (2nm) Channel of Junctionless Transistors with Ideal Subthreshold Slope, H.-B. Chen*, Y.-C. Wu**, C.-Y. Chang*, M.-H. Han*, N.-H. Lu** and Y.-C. Cheng**, *National Chiao-Tung Univ. and **National Tsing Hua Univ., Taiwan

SESSION 16 - Beyond CMOS [Shunju II]
Thursday, June 13, 16:15-17:55
Chairpersons: H. Morimura, NTT Corp.
T. Palacios, Massachusetts Institute of Technology

16-1 - 16:15
Synthetic Electric Field Tunnel FETs: Drain Current Multiplication Demonstrated by Wrapped Gate Electrode Around Ultrathin Epitaxial Channel, Y. Morita, T. Mori, S. Migita, W. Mizubayashi, A. Tanabe, K. Fukuda, T. Matsukawa, K. Endo, S. O'uchi, Y.X. Liu, M. Masahara and H. Ota, Green Nanoelectronics Center (GNC), Nanoelectronics Research Institute (NeRI) and National Institute of Advanced Industrial Sci. and Tech. (AIST), Japan

16-2 - 16:40
Neural Network Based on a Three-Terminal Ferroelectric Memristor to Enable On-Chip Pattern Recognition, Y. Kaneko, Y. Nishitani, M. Ueda and A. Tsujimura, Panasonic Corp., Japan

16-3 - 17:05
Performance of Threshold Switching in Chalcogenide Glass for 3D Stackable Selector, S. Kim, Y.-B. Kim, K.M. Kim, S.-J. Kim, S.R. Lee, M. Chang, E. Cho, M.-J. Lee, D. Lee, C.J. Kim, U.-I. Chung and I.-K. Yoo, Samsung Advanced Institute of Technology, Korea

16-4 - 17:30
Bidirectional TaO-Diode-Selected, Complementary Atom Switch (DCAS) for Area-Efficient, Nonvolatile Crossbar Switch Block, K. Okamoto, M. Tada, N. Banno, T. Sakamoto, M. Miyamura, N. Iguchi, T. Nohisa and H. Hada, Low-power Electronics Association & Project (LEAP), Japan

SESSION 17 - Late News [Suzaku II]
Thursday, June 13, 16:15-17:00
Chairpersons: T. Iwamatsu, Renesas Electronics Corp.

17-1 - 16:15 (Late News)
Record Extrinsic Transconductance (2.45 mS/μm at V_{DS} = 0.5 V) InAs/$In_{0.53}Ga_{0.47}As$ Channel MOSFETs Using MOCVD Source-Drain Regrowth, S. Lee, C.-Y. Huang, A.D. Carter, D.C. Elias, J.J.M. Law, V. Chobpattana, S. Krämer, B.J. Thibeault, W. Mitchell, S. Stemmer, A.C. Gossard and M.J.W. Rodwell, Univ. of California, USA

17-2 - 16:30 (Late News)
Experimental Analysis and Modeling of Self Heating Effect in Dielectric Isolated Planar and Fin Devices, S. Lee, R. Wachnik, P. Hyde, L. Wagner, J. Johnson, A. Chou, A. Kumar, S. Narasimha, T. Standaert, B. Greene, T. Yamashita, J. Johnson, K. Balakrishnan, H. Bu, S. Springer, G. Freeman, W. Henson and E. Nowak, IBM Semiconductor Research and Development Center, USA

17-3 - 16:45 (Late News)
High-Voltage Complementary BEOL-FETs on Cu Interconnects Using N-type IGZO and P-type SnO Dual Oxide Semiconductor Channels, H. Sunamura, K. Kaneko, N. Furutake, S. Saito, M. Narihiro, M. Hane and Y. Hayashi, Renesas Electronics Corp., Japan