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SESSION 3 - Technology / Circuits Joint Focus Session - 3D Integrated Circuits & Applications [Suzaku I, II]

Wednesday, June 12, 10:30-12:35

Chairpersons: R. Kuppuswamy, Intel India
V. Chandra, ARM

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An Extra Low-Power 1Tbit/s Bandwidth PLL/DLL-Less eDRAM PHY Using 0.3V Low-Swing IO for 2.5D CoWoS Application, M.-S. Lin, C.-C. Tsai, C.-H. Chang, W.-H. Huang, Y.-Y. Hsu, S.-C. Yang, C.-M. Fu, M.-H. Chou, T.-C. Huang, C.-F. Chen, T.-C. Huang, S. Adham, M.-J. Wang, W.W. Shen and A. Mehta, TSMC, Taiwan

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3D IC Heterogeneous Integration of GPS RF Receiver, Baseband, and DRAM on CoWoS with System BIST Solution, W.S. Liao, H.N. Chen, K.K. Yen, E.H. Yeh, F.W. Kuo, T.J. Yeh, F. Kuo, C.P. Jou, S. Liu, F.L. Hsueh, H.C. Lin, C.N. Peng, M.J. Wang, W.C. Wu, S.P. Hu, M.F. Chen, S.Y. Hou, S.P. Jeng, C.H. Yu, K.C. Yee and D. Yu, TSMC, Taiwan

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3D Stackable Vertical-Gate BE-SONOS NAND Flash with Layer-Aware Program-and-Read Schemes and Wave-Propagation Fail-Bit-Detection against Cross-Layer Process Variations, C.-H. Hung*, Y.-S. Yang***, Y.-J. Kuo**, T.-N. Lai**, S.-J. Shen**, J.-Y. Hsu**, S.-N. Hung*, H.-T. Lue*, M.-F. Chang**, Y.-H. Shih*, S.-L. Huang*, T.-W. Chen*, T.S. Chen*, C.K. Chen*, C.-Y. Hung* and C.-Y. Lu*, *Macronix International Co., Ltd and **National Tsing Hua Univ., Taiwan

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3-4 - 11:45

A 0.9 pJ/bit, 12.8 GByte/s WideIO Memory Interface in a 3D-IC NoC-Based MPSoC, D. Dutoit*, C. Bernard*, S. Chéramy*, F. Clermidy*, Y. Thonnart*, P. Vivet*, C. Freund**, V. Guérin**, S. Guilhot**, S. Lecomte**, G. Qualizza**, J. Pruvost**, Y. Dodo***, N. Hotelier*** and J. Michailos***, *CEA, Leti, Minatoc, **ST-Ericsson and ***STMicroelectronics, France

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Technology / Circuits Jumbo Joint Focus Session 1 - Design Enablement [Shunju I]

Wednesday, June 12, 13:55-17:50

Chairpersons: K. Kobayashi, Kyoto Institute of Technology
G. Yeap, Qualcomm Inc.

JJ1-1 - 13:55

(Invited)

Enabling Circuit Design Using FinFETs through Close Ecosystem Collaboration, B.J. Sheu*, C.-S. Chang*, Y.-H. Chen*, K. Wang*, K.-J. Chen*, Y.-C. Peng*, L.-C. Tien*, M.-H. Song*, C. Hou*, J.Y.-C. Sun* and C. Hu**, *TSMC, Taiwan and **Univ. of California, USA

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JJ1-3 - 14:45

LAYOUT-INDUCED STRESS EFFECTS IN 14NM & 10NM FINFETs AND THEIR IMPACT ON PERFORMANCE, M.G. Bardoni*, V. Moroz**, G. Eneman*, P. Schuddinck*, M. Dehan*, D. Yakimets*, D. Jang*, G. Van der Plas*, A. Mercha*, A. Thean*, D. Verkest* and A. Steegen*, *imec, Belgium and **Synopsys, Inc., USA

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JJ1-4 - 15:10

Process and Local Layout Effect Interaction on a High Performance Planar 20nm CMOS, F. Sato*, R. Ramachandran*, H. Van Meer**, K.H. Cho***, A. Ozbek*, X. Yang**, Y. Liu**, Z. Li*, X. Wu**, S. Jain*, H. Utomo*, U. Kwon*, Y. Park***, W.L. Tan**, X. Dai**, W. Lai*, J. Kim***, D. Jones**, M. Ganz**, D.H. Bae***, R. Lallement****, S.C. Vemula**, T. Kwon**, P. Lee**, Y. Qi**, M. Weybright*, A. Scholze*, R. Bingert****, J. King*, M. Sherony*, M. Eller**, H. Shang*, K. Tabakman*, V. Narayanan*, S. Samavedam** and R. Divakaruni*, *IBM Microelectronics, **GLOBALFOUNDRIES, ***Samsung Electronics and ****STMicroelectronics, USA

T116

JJ1-5 - 15:35

0.5V Image Processor with 563 GOPS/W SIMD and 32bit CPU Using High Voltage Clock Distribution (HVCD) and Adaptive Frequency Scaling (AFS) with 40nm CMOS, M. Nomura*, A. Muramatsu*, H. Takeno*, S. Hattori*, D. Ogawa*, M. Nasu*, K. Hirairi*, S. Kumashiro*, S. Moriwaki*, Y. Yamamoto*, S. Miyano*, Y. Hiraku*, I. Hayashi*, K. Yoshioka**, A. Shikata**, H. Ishikuro**, M. Ahn***, Y. Okuma*, X. Zhang***, Y. Ryu*, K. Ishida***, M. Takamiya***, T. Kuroda**, H. Shinohara* and T. Sakurai***, *Semiconductor Technology Academic Research Center (STARC), **Keio Univ. and ***The Univ. of Tokyo, Japan

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Chairpersons: K. Miyashita, Toshiba Corp.
G. Lehmann, Infineon Technologies AG

JJ1-6 - 16:10

(Invited)*** %

Design for ESD Protection at Its Limits, H. Gossner, Intel Mobile Communications Group, Germany

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JJ1-7 - 16:35

Application of Low-Noise TIA ICs for Novel Sensing of MOSFET Noise up to the GHz Region, K. Ohmori***, R. Hasunuma***, S. Yamamoto***, Y. Tamura***, H. Jiang****, N. Ishihara****, K. Masu**** and K. Yamada***, *Univ. of Tsukuba, **JST-CREST, ***D-Clue Technologies and ****Tokyo Institute of Technology, Japan

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JJ1-8 - 17:00

First Demonstration of a Full 28nm High-k/Metal Gate Circuit Transfer from Bulk to UTBB FDSOI Technology through Hybrid Integration, D. Golanski*, P. Fonteneau*, C. Fenouillet-Beranger**, A. Cros*, F. Monsieur, N. Guitard*, C.-A. Legrand*, A. Dray*, C. Richier*, H. Beckrich*, P. Mora*, G. Bidal, O. Weber**, O. Saxod*, J.-R. Manouvrier*, P. Galy*, N. Planes* and F. Arnaud*, *ST Microelectronics and **CEA-LETI MINATEC, France

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SESSION 4 - Circuits for Biomedical Applications [Suzaku III]

Wednesday, June 12, 13:55-16:00

Chairpersons: C.Y. Lee, National Chiao Tung Univ.
N. Van Helleputte, imec

4-1 - 13:55

A 200-Channel 10µW 0.04mm² Dual-Mode Acquisition IC for High Density MEA, J. Guo, W. Ng, J. Yuan and M. Chan, Hong Kong Univ. of Sci. and Tech., China

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A Neurochemical Pattern Generator SoC with Switched-Electrode Management for Single-Chip Electrical Stimulation and 9.3µW, 78pA_{rms}, 400V/s FSCV Sensing, B. Bozorgzadeh*, D.P. Covey**, C.D. Howard**, P.A. Garris** and P. Mohseni*, *Case Western Reserve Univ. and **Illinois State Univ., USA

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4-3 - 14:45

A 28.6µW Mixed-Signal Processor for Epileptic Seizure Detection, T.-J. Chen*, S.-C. Lee*, C.-H. Yang*, C.-F. Chiu** and H. Chiueh*, *National Chiao Tung Univ. and **National Chip Implementation Center, Taiwan

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4-4 - 15:10

A 1024-Channel CMOS Microelectrode-Array System with 26'400 Electrodes for Recording and Stimulation of Electro-Active Cells In-Vitro, M. Ballini*, J. Müller*, P. Livi*, Y. Chen*, U. Frey**, A. Shadmani*, I.L. Jones*, W. Gong*, M. Fiscella*, M. Radivojevic*, D. Bakkum*, A. Stettler*, F. Heer* and A. Hierlemann*, *ETH Zurich, Switzerland and **RIKEN, Japan

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4-5 - 15:35

A 51fA/HZ^{0.5} Low Power Heterodyne Impedance Analyzer for Electrochemical Impedance Spectroscopy, J. Guo, W. Ng, J. Yuan and M. Chan, Hong Kong Univ. of Sci. and Tech., China

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SESSION 5 - Delta-Sigma Modulators [Suzaku I, II]

Wednesday, June 12, 13:55-16:00

Chairpersons: S. Doshu, Panasonic Corp.
E. Fogleman, MaxLinear

5-1 - 13:55

A 75.1dB SNDR 840MS/s CT ΔΣ Modulator with 30MHz Bandwidth and 46.4fJ/conv FOM in 55nm CMOS, C.-L. Lo, C.-Y. Ho, H.-C. Tsai and Y.-H. Lin, MediaTek Inc., Taiwan

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5-2 - 14:20

A 69dB SNDR, 25MHz BW, 800MS/s Continuous-Time Bandpass ΔΣ ADC Using DAC Duty Cycle Control for Low Power and Reconfigurability, H. Chae and M.P. Flynn, Univ. of Michigan, USA

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A 66dB SNDR 15MHz BW SAR Assisted ΔΣ ADC in 22nm Tri-Gate CMOS, C.C. Lee, E. Alpman, S. Weaver, C.-Y. Lu and J. Rizk, Intel Corp., USA

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A 379nW 58.5dB SNDR VCO-Based ΔΣ Modulator for Bio-Potential Monitoring, Y.-D. Chang, C.-H. Weng, T.-H. Lin and C.-K. Wang, National Taiwan Univ., Taiwan

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5-5 - 15:35

A 4.1mW, 12-bit ENOB, 5MHz BW, VCO-Based ADC with On-Chip Deterministic Digital Background Calibration in 90nm CMOS, S. Rao, K. Reddy, B. Young and P.K. Hanumolu, Oregon State Univ., USA

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Chairpersons: K. Agawa, Toshiba Corp.
B.P. Ginsburg, Texas Instruments

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A 2dB NF Receiver with 10mA Battery Current Suitable for Coexistence Applications, A. Mirzaei, M. Mikhemar, D. Murphy and H. Darabi, Broadcom Corp., USA

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A Low-Cost SAW-Less GSM/GPRS SoC with Integrated Connectivity and 32-kHz Crystal Removal in 55nm, C.-M. Hung, C.-C. Lin, S.-C. Yen, P.-Y. Chang, Y.-T. Lee, S.-C. Tseng, M.-Y. Hsieh, J.-Y. Ding, Y.-T. Chen, Y.-C. Wang, J.-Q. Chen, K.-C. Chen, P.-M. Wang, H.-J. Wei and M.-C. Wu, MStar Semiconductor Inc., Taiwan

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6-3 - 17:00

A 1.15V Low Power Mobile ISDB-Tsb/Tmm/T and DVB-T Tuner SoC in 40nm CMOS, S. Uemura, G. Hayashi, A. Sawada, T. Nasu, T. Kono, Y. Hosokawa, J. Koide, Y. Okumura, A. Ohara, K. Takahashi, K. Miyano and H. Kimura, Panasonic Corp., Japan

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6-4 - 17:25

Two-Channel Receiver Back-End Using Statistically Calibrated HRM with >70dB 3rd and 5th Harmonic Rejection for Carrier Aggregation in 32nm CMOS, E. Alpman*, M. Verhelst**, and H. Lakdawala*, *Intel Corp., USA and **KU Leuven, Belgium

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SESSION 7 - Plenary Session [Suzaku I, II]

Thursday, June 13, 8:45-10:05

Chairpersons: H. Kabuo, Panasonic Corp.
J. Gealow, Analog Devices, Inc.

7-1 - 8:45

(Invited)

Perspectives on Mobile Devices and Their Impact on Semiconductor Technologies, S.-W. Jeong, H.-D. Cho, J.-W. Hwang and H.-K. Kwon, Samsung Electronics, Korea

C82

7-2 - 9:25

(Invited)

Glass for the Future: Displays and Semiconductors, P. L. Bocko, and G. R. Trott, Corning Inc., USA

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SESSION 8 - Pipeline ADCs [Suzaku I]

Thursday, June 13, 10:30-12:35

Chairpersons: M. Ito, Renesas Electronics Corp.
G. Van der Plas, imec

8-1 - 10:30

A 5.4GS/s 12b 500mW Pipeline ADC in 28nm CMOS, J. Wu, A. W.-T. Chou, C.-H. Yang, Y. Ding, Y.-J. Ko, S.-T. Lin, W. Liu, C.-M. Hsiao, M.-H. Hsieh, C.-C. Huang, J.-J. Hung, K.Y. Kim, M. Le, T. Li, W.-T. Shih, A. Shrivastava, Y.-C. Yang, C.-Y. Chen and H.-S. Huang, Broadcom Corp., USA

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8-2 - 10:55

A 75.9dB-SNDR 2.96mW 29fJ/Conv-Step Ringamp-Only Pipelined ADC, B. Hershberg** and U.-K. Moon*, *Oregon State Univ., USA and **imec, Belgium

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A 70MS/s 69.3dB SNDR 38.2fJ/Conversion-Step Time-Based Pipelined ADC, T. Oh, H. Venkatram and U.-K. Moon, Oregon State Univ., USA

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A 12-Bit, 200-MS/s, 11.5-mW Pipeline ADC Using a Pulsed Bucket Brigade Front-End, N. Dolev, M. Kramer and B. Murmann, Stanford Univ., USA

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A 10-Bit 800-MHz 19-mW CMOS ADC, S.-H.W. Chiang, H. Sun and B. Razavi, Univ. of California, USA

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Thursday, June 13, 10:30-12:35

Chairpersons: R. Takemura, Hitachi, Ltd.
F. Hamzaoglu, Intel Corp.

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1Mb 0.41 μm² 2T-2R Cell Nonvolatile TCAM with Two-Bit Encoding and Clocked Self-Referenced Sensing, J. Li*, R. Montoye*, M. Ishii**, K. Stawiasz*, T. Nishida***, K. Maloney****, G. Ditlow*, S. Lewis****, T. Maffitt****, R. Jordan****, L. Chang* and P. Song*, *IBM T. J. Watson Research Center, USA, **IBM Tokyo Research Lab, ***IBM Japan Services Company Ltd., Japan and ****IBM Burlington, USA

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Fabrication of a 99%-Energy-Less Nonvolatile Multi-Functional CAM Chip Using Hierarchical Power Gating for a Massively-Parallel Full-Text-Search Engine, S. Matsunaga*, N. Sakimura**, R. Nebashi**, Y. Tsuji**, A. Morioka**, T. Sugibayashi**, S. Miura**, H. Honjo**, K. Kinoshita*, H. Sato*, S. Fukami*, M. Natsui*, A. Mochizuki*, S. Ikeda*, T. Endoh*, H. Ohno* and T. Hanyu*, *Tohoku Univ. and **NEC Corp., Japan

C106

9-3 - 11:20

A 250-MHz 256b-I/O 1-Mb STT-MRAM with Advanced Perpendicular MTJ Based Dual Cell for Nonvolatile Magnetic Caches to Reduce Active Power of Processors, H. Noguchi, K. Kushida, K. Ikegami, K. Abe, E. Kitagawa, S. Kashiwada, C. Kamata, A. Kawasumi, H. Hara and S. Fujita, Toshiba Corp., Japan

C108

9-4 - 11:45

A 1.5nsec/2.1nsec Random Read/Write Cycle 1Mb STT-RAM Using 6T2MTJ Cell with Background Write for Nonvolatile e-Memories, T. Ohsawa*, S. Miura**, K. Kinoshita*, H. Honjo**, S. Ikeda*, T. Hanyu*, H. Ohno* and T. Endoh*, *Tohoku Univ. and **NEC Corp., Japan

C110

9-5 - 12:10

Area-Efficient Embedded RRAM Macros with Sub-5ns Random-Read-Access-Time Using Logic-Process Parasitic-BJT-Switch (0T1R) Cell and Read-Disturb-Free Temperature-Aware Current-Mode Read Scheme, M.-F. Chang*, C.-C. Kuo*, S.-S. Sheu**, C.-J. Lin*, Y.-C. King*, Z.-H. Lin**, K.-L. Su**, Y.-S. Chen**, W.-P. Lin**, H.-Y. Lee**, C.-H. Tsai**, W.-S. Chen**, F.T. Chen**, T.-K. Ku**, M.-J. Kao**, M.-J. Tsai**, J.-J. Wu****, Y.-D. Chih*** and S. Natarajan***, *National Tsing Hua Univ., **ITRI and ***TSMC, Taiwan

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Luncheon Talk [Suzaku II]

Thursday, June 13, 12:45-14:05

Organizer: H. Kabuo, Panasonic Corp.

Symbiosis with Lightning Which Is One of the Most Spectacular Natural Phenomenon, T. Kudo, Otowa Electric Co., Ltd., Japan

Technology / Circuits Jumbo Joint Focus Session 2 - SRAM [Shunju I]

Thursday, June 13, 14:20-18:20

Chairpersons: T. Tanaka, Fujitsu Semiconductor Ltd.
S. Sridhara, Texas Instruments

JJ2-1- 14:20

(Invited)

Fully-Depleted Planar Technologies and Static RAM, T. Hook*, K. Cheng**, B. Doris**, A. Khakifirooz**, Q. Liu****, S. Ponoth**, C. Radens*** and M. Vinet****, *IBM SRDC, **IBM Albany, ***IBM East Fishkill, ****STMicroelectronics, *****LETI, USA

T206

JJ2-2 - 14:45

A 20nm 0.6V 2.1 μ W/MHz 128kb SRAM with No Half Select Issue by Interleave Wordline and Hierarchical Bitline Scheme, H. Fujiwara, M. Yabuuchi, M. Morimoto, K. Tanaka, M. Tanaka, N. Maeda, Y. Tsukamoto and K. Nii, Renesas Electronics Corp., Japan

C118**JJ2-3 - 15:10**

FDSOI Process/Design Full Solutions for Ultra Low Leakage, High Speed and Low Voltage SRAMs, R. Ranica*, N. Planes*, O. Weber**, O. Thomas**, S. Haendler*, D. Noblet*, D. Croain*, C. Gardin* and F. Arnaud*, *STMicroelectronics and **CEA, LETI, MINATEC, France

T210**JJ2-4 - 15:35**

Ultralow-Voltage Operation of Silicon-on-Thin-BOX (SOTB) 2Mbit SRAM Down to 0.37 V Utilizing Adaptive Back Bias, Y. Yamamoto*, H. Makiyama*, H. Shinohara*, T. Iwamatsu*, H. Oda*, S. Kamohara*, N. Sugii*, Y. Yamaguchi*, T. Mizutani** and T. Hiramoto**, *Low-power Electronics Association & Project (LEAP) and **The Univ. of Tokyo, Japan

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Chairpersons: H. Yamauchi, Fukuoka Institute of Technology
J. Cheek, Freescale

JJ2-5- 16:15**(Invited)**

Enhancing SRAM Performance by Advanced FinFET Device and Circuit Technology Collaboration for 14nm Node and Beyond, K. Endo, S. O'uchi, T. Matsukawa, Y. Liu, K. Sakamoto, W. Mizubayashi, S. Migita, Y. Morita, H. Ota, E. Suzuki and M. Masahara, Nanoelectronics Research Institute, National Institute of Advanced Industrial Sci. and Tech., Japan

T214**JJ2-6 - 16:40**

Dual-V_{cc} 8T-Bitcell SRAM Array in 22nm Tri-Gate CMOS for Energy-Efficient Operation across Wide Dynamic Voltage Range, J. Kulkarni, M. Khellah, J. Tschanz, B. Geuskens, R. Jain, S. Kim and V. De, Intel Corp., USA

C126**JJ2-7 - 17:05**

A 10 nm Si-Based Bulk FinFETs 6T SRAM with Multiple Fin Heights Technology for 25% Better Static Noise Margin, M.-C. Chen*, C.-H. Lin*, Y.-F. Hou*, Y.-J. Chen*, C.-Y. Lin*, F.-K. Hsueh*, H.-L. Liu*, C.-T. Liu*, B.-W. Wang**, H.-C. Chen*, C.-C. Chen*, S.-H. Chen*, C.-T. Wu*, T.-Y. Lai*, M.-Y. Lee*, B.-W. Wu*, C.-S. Wu*, I. Yang*, Y.-P. Hsieh***, C.H. Ho*, T. Wang**, A.B. Sachid****, C. Hu**** and F.-L. Yang*, *National Nano Device Labs. (NDL), **National Chiao-Tung Univ., ***National Cheng Kung Univ., Taiwan and ****UC Berkeley, USA

T218**JJ2-8 - 17:30**

A 210mV 7.3MHz 8T SRAM with Dual Data-Aware Write-Assists and Negative Read Wordline for High Cell-Stability, Speed and Area-Efficiency, C.-F. Chen*, T.-H. Chang*, L.-F. Chen*, M.-F. Chang* and H. Yamauchi**, *National Tsing Hua Univ., Taiwan and **Fukuoka Institute of Technology, Japan

C130**JJ2-9 - 17:55**

A 22nm 2.5MB Slice On-Die L3 Cache for the Next Generation Xeon® Processor, W. Chen, S.-L. Chen, S. Chiu, R. Ganesan, V. Lukka, W.W. Mar and S. Rusu, Intel Corp., USA

C132**SESSION 10 - PLL Building Blocks [Suzaku I]**

Thursday, June 13, 14:20-16:00

Chairpersons: S.H. Cho, KAIST
P. Hanumolu, Oregon State Univ.

10-1 - 14:20

A 9b, 1.12ps Resolution 2.5b/Stage Pipelined Time-to-Digital Converter in 65nm CMOS Using Time-Register, K.S. Kim, W.S. Yu and S.H. Cho, KAIST, Korea

C136**10-2 - 14:45**

A 0.11mm², 5.7-to-6.7GHz, Parametrically Pumped Quadrature LC-VCO with Digital Outputs, K. Bhardwaj, S. Seth, B. Murmann and T.H. Lee, Stanford Univ., USA

C138**10-3 - 15:10**

A 720 μ W 873MHz-1.008GHz Injection-Locked Frequency Multiplier with 0.3V Supply Voltage in 90nm CMOS, L. Liu, K. Ishikawa and T. Kuroda, Keio Univ., Japan

C140**10-4 - 15:35**

93% Power Reduction by Automatic Self Power Gating (ASPG) and Multistage Inverter for Negative Resistance (MINR) in 0.7V, 9.2 μ W, 39MHz Crystal Oscillator, S. Iguchi*, A. Saito**, Y. Zheng*, K. Watanabe**, T. Sakurai* and M. Takamiya*, *Univ. of Tokyo and **Semiconductor Technology Academic Research Center (STARC), Japan

C142**SESSION 11 - Low Power Wireless [Suzaku III]**

Thursday, June 13, 14:20-16:00

Chairpersons: H. Ishikuro, Keio Univ.
B. Nauta, Univ. of Twente

11-1 - 14:20

A 0.9V Low-Power 0.4-6GHz Linear SDR Receiver in 28nm CMOS, J. Borremans*, B. van Liempd*, E. Martens*, S. Cha** and J. Craninckx*, *imec, Belgium and **Renesas Electronics Corp., Japan

C146**11-2 - 14:45**

An Ultra Low Power, Reconfigurable, Multi-Standard Transceiver Using Fully Digital PLL, S. Chakraborty*, V. Parikh*, S. Sankaran*, T. Motos*, O. Fikstvedt*, J.-T. Marienborg*, D. Griffith*, I. Prathapan*, K. Nagaraj*, F. Zhang**, R. Smith*, W. Budziak*, S. Sundar* and P. Cruise*, *Texas Instruments Inc. and **NVIDIA Inc., USA

C148**11-3 - 15:10**

Intermittent Transmitter Circuit with Novel Feedback Source Follower Amplifier for Solar Powered 5-mm-Cubic Wireless Sensor Nodes with 1/20 λ Dipole Antenna, S. Oshima, K. Matsunaga, H. Morimura and M. Harada, NTT Microsystem Integration Labs., Japan

C150**11-4 - 15:35**

A -90dBm Sensitivity Wireless Transceiver Using VCO-PA-LNA-Switch-Modulator Co-Design for Low Power Insect- Based Wireless Sensor Networks, S. Sayilir*, W.-F. Loke*, J. Lee*, B. Epstein**, D.L. Rhodes** and B. Jung*, *Purdue Univ. and **OpCoast LLC, USA

C152**SESSION 12 - Clock and Frequency Generation [Suzaku I]**

Thursday, June 13, 16:15-17:55

Chairpersons: J. Lee, National Taiwan Univ.
N. Kurd, Intel Corp.

12-1 - 16:15

A 2.5GHz 5.4mW 1-to-2048 Digital Clock Multiplier Using a Scrambling TDC, R.K. Nandwana, S.Saxena, A. Elshazly, K. Mayaram and P.K. Hanumolu, Oregon State Univ., USA

C156

12-2 - 16:40

A 1.3-mW, 1.6-GHz Digital Delay-Locked Loop with Two-Cycle Locking Time and Dither-Free Tracking, K. Kim, S. Son, S. Ryu, H. Yeo, Y. Choi and J. Kim, Seoul National Univ., Korea

C158

12-3 - 17:05

A 288fs RMS Jitter Versatile 8-12.4GHz Wide-Band Fractional-N Synthesizer for SONET and SerDes Communication Standards in 40nm CMOS, M.R. Ahmadi, D. Pi, B. Çatlı, U. Singh, B. Zhang, Z. Huang, A. Momtaz and J. Cao, Broadcom Corp., USA

C160

12-4 - 17:30

A 32nm, 0.9V Supply-Noise Sensitivity Tracking PLL for Improved Clock Data Compensation Featuring a Deep Trench Capacitor Based Loop Filter, B. Kim, W. Xu and C. H. Kim, Univ. of Minnesota, USA

C162

SESSION 13 - Linear Regulators and DC-DC Converters [Suzaku III]

Thursday, June 13, 16:15-18:20

Chairpersons: H. Nakamoto, Fujitsu Labs., Ltd.
J.L. Nilles, Texas Instruments

13-1 - 16:15

A 0.6V Resistance-Locked Loop Embedded Digital Low-Dropout Regulator in 40nm CMOS with 77% Power Supply Rejection Improvement, C.-C. Chiu*, P.-H. Huang*, M. Lin*, K.-H. Chen*, Y.-H. Lin**, T.-Y. Tsai**, C.-C. Huang** and C.-C. Lee**, *National Chiao Tung Univ. and **Realtek Semiconductor Corp., Taiwan

C166

13-2 - 16:40

High-Gain Wide-Bandwidth Capacitor-Less Low-Dropout Regulator with Zero Insertion Utilizing Frequency Response of Inner Loops, S.-W. Hong, S. Jung, C. Park, T.-H. Kong, M.-Y. Jung, S.-T. Ryu and G.-H. Cho, KAIST, Korea

C168

13-3 - 17:05

A Pseudo-Noise Coded Constant-Off-Time (PNC-COT) Control Switching Converter with Maximum 18.7 dBm Peak Spur Reduction and 92% Efficiency in 40 nm CMOS, Y.-P. Su*, Y.-H. Lee*, W.-C. Chen*, K.-H. Chen*, Y.-H. Lin**, T.-Y. Tsai**, C.-C. Huang** and C.-C. Lee**, *National Chiao Tung Univ. and **Realtek Semiconductor Corp., Taiwan

C170

13-4 - 17:30

A 10V Fully-Integrated Bidirectional SC Ladder Converter in 0.13µm CMOS Using Nested-Bootstrapped Switch Cells, C.M. Dougherty*, L. Xue*, J. Pulskamp**, S. Bedair**, R. Polcawich**, B. Morgan** and R. Bashirullah*, *Univ. of Florida and **U.S. Army Research Laboratory, USA

C172

13-5 - 17:55

A 0.45-1V Fully Integrated Reconfigurable Switched Capacitor Step-Down DC-DC Converter with High Density MIM Capacitor in 22nm Tri-Gate CMOS, R. Jain, B. Geuskens, M. Khellah, S. Kim, J. Kulkarni, J. Tschanz and V. De, Intel Corp., USA

C174

RUMP SESSIONS [Suzaku I, II, III]

Thursday, June 13, 20:00-22:00

R-1: The Best Logic and Memory Interface Technology for 2D/2.5D/3D ICs [Suzaku I, II]

Organizers: N. Lu, Etron Technology, Inc.
J. Zerbe, Rambus Inc.

C178

Moderators: N. Lu, Etron Technology, Inc.
K. Chang, Xilinx, Inc.

R-2: Analog Designer's Play-Ground Beyond 20nm, Is it Circuit Physics or Auto Place & Route? [Suzaku III]

Organizers/Moderators: C.-M. Hung, MStar Semiconductor, Inc.
A. Cathelin, STMicroelectronics

C178

Technology / Circuits Joint Rump Session

Tuesday, June 11, 20:00-22:00

J-R: SOC vs. 3D IC in the More-than-Moore Era [Suzaku I, II]

Organizers: Technology
N. Sugii, LEAP
C.-P. Chang, Applied Materials, Inc.

C179

Circuits

H. Noda, Elpida Memory, Inc.
J. Debrosse, IBM Research

Moderators: S. Ramaswami, Applied Materials, Inc.
S. Natarajan, TSMC

SESSION 14 - Image Processing [Suzaku I]

Friday, June 14, 8:30-10:10

Chairpersons: M. Igarashi, Sony LSI Design, Inc.
T. Burd, AMD

14-1 - 8:30

A 100,000 fps Vision Sensor with Embedded 535GOPS/W 256x256 SIMD Processor Array, S.J. Carey, A. Lopich, D.R.W. Barr, B. Wang and P. Dudek, The Univ. of Manchester, UK

C182

14-2 - 8:55

A 125,582 Vector/s Throughput and 95.1% Accuracy ANN Searching Processor with Neuro-Fuzzy Vision Cache for Real-Time Object Recognition, I. Hong, J. Park, G. Kim, J. Oh and H.-J. Yoo, KAIST, Korea

C184

14-3 - 9:20

A 240x180 10mW 12us Latency Sparse-Output Vision Sensor for Mobile Applications, R. Berner, C. Brandli, M. Yang, S.-C. Liu and T. Delbruck, Univ. of Zurich and ETH Zurich, Switzerland

C186

14-4 - 9:45

A 1062Mpixels/s 8192x4320p High Efficiency Video Coding (H.265) Encoder Chip, S.-F. Tsai, C.-T. Li, H.-H. Chen, P.-K. Tsung, K.-Y. Chen and L.-G. Chen, National Taiwan Univ., Taiwan

C188

SESSION 15 - All Digital Phase-Locked Loops [Suzaku II]

Friday, June 14, 8:30-10:10

Chairpersons: K. Nose, Renesas Electronics Corp.
K. Chang, Xilinx, Inc.

15-1 - 8:30

An 8.5 mW, 0.07 mm² ADPLL in 28 nm CMOS with Sub-ps Resolution TDC and < 230 fs RMS Jitter, B. Shen, G. Unruh, M. Lughart, C.-H. Lee and M. Chambers, Broadcom Corp., USA

C192

15-2 - 8:55

A 12GHz 210fs 6mW Digital PLL with Sub-Sampling Binary Phase Detector and Voltage-Time Modulated DCO, Z. Ru***, P. Geraedts****, E. Klumperink*, X. He**** and B. Nauta*, *Univ. of Twente, The Netherlands, **MediaTek, USA, ***Axiom IC and ****NXP Semiconductors, The Netherlands

C194

15-3 - 9:20

A 25GHz 100ns Lock Time Digital LC PLL with an 8-Phase Output Clock, R. Navid, M. Hekmat, F. Aryanfar, J. Wei and V. Gadde, Rambus Inc, USA

C196

15-4 - 9:45**A 28GHz Hybrid PLL in 32nm SOI CMOS**

M. Ferriss, A. Rylyakov, H. Ainspan, J. Tierno and D. Friedman, IBM T. J. Watson Research Center, USA

C198**SESSION 16 - Embedded Non-Volatile Memory [Suzaku III]**

Friday, June 14, 8:30-10:10

Chairpersons: M. Yamaoka, Hitachi, Ltd.
C. Dry, Intel Mobile Communications

16-1 - 8:30

A MCU Platform with Embedded FRAM Achieving 350nA Current Consumption in Real-Time Clock Mode with Full State Retention and 6.5µs System Wakeup Time, A. Baumann, M. Jung, K. Huber, M. Arnold, C. Sichert, S. Schauer and R. Brederlow, Texas Instruments Deutschland GmbH, Germany

C202**16-2 - 8:55**

A 0.6V 8 pJ/write Non-Volatile CBRAM Macro Embedded in a Body Sensor Node for Ultra Low Energy Applications, N. Gilbert*, Y. Zhang**, J. Dinh*, B. Calhoun** and S. Hollmer*, *ADESTO Technologies and **Univ. of Virginia, USA

C204**16-3 - 9:20**

A 38% Access Time Improvement in 40nm CMOS Technology with Triple-Wire-Program-Cell Scheme for High Density MROM, T. Dozaka*, T. Hojo*, T. Yabe*, T. Fukuda*, T. Midorikawa*, K. Kohara*, K. Hashimoto**, I. Wakiyama**, Y. Uchino* and N. Otsuka*, *Toshiba Corp. and **Toshiba Microelectronics Corp., Japan

C206**16-4 - 9:45**

A 28nm ROM with Two-Step Decoding Scheme and OD-Space-Effect Minimization to Achieve 30% Speed and 190mV Vmin Improvement, C.-W. Wu, K.-T. Chen, R. Lee, W.-S. Kao, H.-J. Liao, J. Chang and S. Natarajan, TSMC, Taiwan

C208**SESSION 17 - Sensors [Suzaku I]**

Friday, June 14, 10:30-12:35

Chairpersons: Y. Kato, Panasonic Corp.
B. Nikolić, Univ. of California, Berkeley

17-1 - 10:30

A Fully Self-Powered Hybrid System Based on CMOS ICs and Large-Area Electronics for Large-Scale Strain Monitoring, Y. Hu, L. Huang, J.S. Robinson, W. Rieutort-Louis, S. Wagner, J.C. Sturm and N. Verma, Princeton Univ., USA

C212**17-2 - 10:55**

A ±0.4°C Accurate High-Speed Remote Junction Temperature Sensor with Digital Beta Correction and Series-Resistance Cancellation in 65nm CMOS, X. Pu, M. Ash, K. Nagaraj, J. Park, S. Vu, P. Kimelman and S. De La Haye, Texas Instruments, USA

C214**17-3 - 11:20**

A 70dB SNR Capacitive Touch Screen Panel Readout IC Using Capacitor-Less Trans-Impedance Amplifier and Coded Orthogonal Frequency-Division Multiple Sensing Scheme, S. Ko*, H. Shin*, H. Jang*, I. Yun** and K. Lee*, *KAIST and **Zinitix, Korea

C216**17-4 - 11:45**

An Integrated Pulse Wave Velocity Sensor Using Bio-Impedance and Noise-Shaped Body Channel Communication, W. Lee and S.H. Cho, KAIST, Korea

C218**17-5 - 12:10**

Integrated CMOS Quantitative Polymerase Chain Reaction Lab-on-Chip, H. Norian, I. Kymissis and K.L. Shepard, Columbia Univ., USA

C220**SESSION 18 - Power Management Techniques [Suzaku II]**

Friday, June 14, 10:30-12:35

Chairpersons: C. Yoo, Hanyang Univ.
H.J. Bergveld, NXP Semiconductors

18-1 - 10:30

An RF Energy Harvester with 35.7% PCE at P_{IN} of -15 dBm, P.-H. Hsieh* and T. Chiang**, *National Tsing Hua Univ. and **National Taiwan Univ., Taiwan

C224**18-2 - 10:55**

A Self-Calibrating RF Energy Harvester Generating 1V at -26.3 dBm, M. Stoopman*, S. Keyrouz****, H.J. Visser****, K. Philips** and W.A. Serdijn*, *Delft Univ. of Technology, **imec-NL and ***Eindhoven Univ. of Technology, The Netherlands

C226**18-3 - 11:20**

A Ripple Voltage Sensing MPPT Circuit for Ultra-Low Power Microsystems, I. Lee, S. Bang, D. Yoon, M. Choi, S. Jeong, D. Sylvester and D. Blaauw, Univ. of Michigan, USA

C228**18-4 - 11:45**

A 6.0-W Bi-Directional DC-DC Converter for Wireless Power Transceiver in 0.35-µm BCDMOS, Y.-J. Moon*, D.-Z. Kim**, S.-W. Kwon**, Y.-S. Roh* and C. Yoo*, *Hanyang Univ. and **Samsung Electronics Co., Korea

C230**18-5 - 12:10**

A Stackable, 6-Cell, Li-Ion, Battery Management IC for Electric Vehicles with 13, 12-bit ΣΔ ADCs, Cell Balancing, and Direct-Connect Current-Mode Communications, K. Kadirvel*, J. Carpenter*, R. Shoemaker*, J. Ross***, P. Huynh*** and B. Lum-Shue-Chan*, *Texas Instruments and **Formerly with Texas Instruments, USA

C232**SESSION 19 - Clocking and Memory Interface [Suzaku III]**

Friday, June 14, 10:30-12:35

Chairpersons: J.-Y. Sim, POSTECH
I. Fujimori, Broadcom Corp.

19-1 - 10:30

A 12Gb/s 0.92mW/Gb/s Forwarded Clock Receiver Based on ILO with 60MHz Jitter Tracking Bandwidth Variation Using Duty Cycle Adjuster in 65nm CMOS, Y.-J. Kim and L.-S. Kim, KAIST, Korea

C236**19-2 - 10:55**

An 8-to-16GHz 28nm CMOS Clock Distribution Circuit Based on Mutual-Injection-Locked Ring Oscillators, Y. Tomita*, K. Suzuki*, T. Matsumoto*, T. Yamamoto**, H. Yamaguchi* and H. Tamura*, *Fujitsu Labs., Ltd., Japan and **Fujitsu Labs. of America, USA

C238**19-3 - 11:20**

A Sub-1.0V 20nm 5Gb/s/pin Post-LPDDR3 I/O Interface with Low Voltage-Swing Terminated Logic and Adaptive Calibration Scheme for Mobile Application, Y.-C. Cho, Y.-C. Bae, B.-M. Moon, Y.-J. Eom, M.-S. Ahn, W.-Y. Lee, C.-R. Cho, M.-H. Park, Y.-J. Jeon, J.-O. Ahn, B.-K. Choi, D.-K. Kang, S.-H. Yoon, Y.-S. Yang, K.-I. Park, J.-H. Choi, J.-B. Lee and J.-S. Choi, Samsung Electronics Co., Korea

C240**19-4 - 11:45**

A Heterogeneous Dual DLL and Quantization Error Minimized ZQ Calibration for 30nm 1.2V 4Gb 3.2Gb/s/pin DDR4 SDRAM, T. Na, Y. Shim, I. Song, J.-K. Kim, S. Hyun, J.-B. Kim, J.-H. Choi, C.-W. Kim, J.-B. Lee and J.S. Choi, Samsung Electronics Co., Korea

C242

19-5 - 12:10

A 400MHz - 1.6GHz Fast Lock, Jitter Filtering ADDLL Based Burst Mode Memory Interface, M. Hossain*, F. Aquil*, P. Chau*, B. Tsang*, P. Le*, J. Wei*, T. Stone*, B. Daly*, T. Chanh*, J. Eble*, K. Knorpp* and J. Zerbe*, *Rambus Inc, USA and **Univ. of Alberta, Canada

C244

SESSION 20 - Medical Processing [Suzaku I]

Friday, June 14, 13:55-16:00

Chairpersons: B. Sheu, TSMC
E. Yeo, Marvell Semiconductor

20-1 - 13:55

A Self-Powered CMOS Reconfigurable Multi-Sensor SoC for Biomedical Applications, Y.-J. Huang, T.-W. Lin, T.-H. Tzeng, C.-W. Huang, P.-W. Yen, C.-T. Lin and S.-S. Lu, National Taiwan Univ., Taiwan

C248

20-2 - 14:20

A Low-Power Microprocessor for Data-Driven Analysis of Analytically-Intractable Physiological Signals in Advanced Medical Sensors, K.H. Lee and N. Verma, Princeton Univ., USA

C250

20-3 - 14:45

A 48.6-to-105.2µW Machine-Learning Assisted Cardiac Sensor SoC for Mobile Healthcare Monitoring, S.-Y. Hsu*, Y. Ho*, P.-Y. Chang*, P.-Y. Hsu*, C.-Y. Yu*, Y. Tseng*, T.-Z. Yang*, T.-F. Yang**, R.-J. Chen***, C. Su* and C.-Y. Lee*, *National Chiao Tung Univ., **Taipei Medical Univ. Hospital and ***Wan Fang Hospital, Taiwan

C252

20-4 - 15:10

A 0.36V, 33.3µW 18-Band ANSI S1.11 1/3-Octave Filter Bank for Digital Hearing Aids in 40nm CMOS, J.-S. Wang, K.-J. Chang, T.-J. Lin, R.W. Prasojo and C. Yeh, National Chung Cheng Univ., Taiwan

C254

20-5 - 15:35

A 401GFlops/W 16-Cores Signal Reconstruction Platform with a 4G Entries/s Matrix Generation Engine for Compressed Sensing and Sparse Representation, Y.-M. Tsai, T.-J. Yang and L.-G. Chen, National Taiwan Univ., Taiwan

C256

SESSION 21 - Nyquist Converters [Suzaku II]

Friday, June 14, 13:55-16:00

Chairpersons: M. Yoshioka, Fujitsu Labs., Ltd.
M. Flynn, Univ. of Michigan

21-1 - 13:55

A 35mW 8 b 8.8 GS/s SAR ADC with Low-Power Capacitive Reference Buffers in 32 nm Digital SOI CMOS, L. Kull***, T. Toifl*, M. Schmatz*, P.A. Francese*, C. Menolfi*, M. Braendli*, M. Kossel*, T. Morf*, T.M. Andersen* and Y. Leblebici**, *IBM Research - Zurich and **EPFL, Switzerland

C260

21-2 - 14:20

A 13-Bit 9GS/s RF DAC-Based Broadband Transmitter in 28nm CMOS, J. Xiao, B. Chen, T.Y. Kim, N.-Y. Wang, X. Chen, T.-H. Chih, K. Raviprakash, H.-F. Chen, R. Gomez and J.Y.C. Chang, Broadcom Corp., USA

C262

21-3 - 14:45

An 8.5mW 5GS/s 6b Flash ADC with Dynamic Offset Calibration in 32nm CMOS SOI, V.H.-C. Chen and L. Pileggi, Carnegie Mellon Univ., USA

C264

21-4 - 15:10

A 0.0058mm² 7.0 ENOB 24MS/s 17fJ/conv. Threshold Configuring SAR ADC with Source Voltage Shifting and Interpolation Technique, K. Yoshioka, A. Shikata, R. Sekimoto, T. Kuroda and H. Ishikuro, Keio Univ., Japan

C266

21-5 - 15:35

A 2.1 mW 11b 410 MS/s Dynamic Pipelined SAR ADC with Background Calibration in 28nm Digital CMOS, B. Verbruggen*, M. Iriguchi**, M. de la Guia Solaz*, G. Glorieux*, K. Deguchi**, B. Malki*** and J. Craninckx*, *imec, Belgium, **Renesas Electronics, Japan and ***Vrije Universiteit Brussel, Belgium

C268

SESSION 22 - Wireline Transceivers [Suzaku III]

Friday, June 14, 13:55-16:00

Chairpersons: K. Sunaga, Automotive Energy Supply Corp.
T. Chan Carusone, Univ. of Toronto

22-1 - 13:55

A 10 Gb/s 2-IIR-Tap DFE Receiver with 35 dB Loss Compensation in 65-nm CMOS, O. Elhadidy and S. Palermo, Texas A&M Univ., USA

C272

22-2 - 14:20

A 6b 10GS/s TI-SAR ADC with Embedded 2-Tap FFE/1-Tap DFE in 65nm CMOS, E.Z. Tabasy, A. Shafik, K. Lee, S. Hoyos and S. Palermo, Texas A&M Univ., USA

C274

22-3 - 14:45

A 2.8 mW/Gb/s Quad-Channel 8.5-11.4 Gb/s Quasi-Digital Transceiver in 28 nm CMOS, A. Nazemi, H. Maarefi, B. Çatli, M.R. Ahmadi, S. Fallahi, T. Ali, M. Abdul-Latif, Y. Liu, J. Kim, A. Momtaz and N. Kocaman, Broadcom Corp., USA

C276

22-4 - 15:10

A 5Gb/s 2.6mW/Gb/s Reference-Less Half-Rate PRPLL-Based Digital CDR, G. Shu, S. Saxena, W.-S. Choi, M. Talegaonkar, R. Inti, A. Elshazly, B. Young and P.K. Hanumolu, Oregon State Univ., USA

C278

22-5 - 15:35

A Fast Power-On 2.2Gb/s Burst-Mode Digital CDR with Programmable Input Jitter Filtering, W.-S. Choi, T. Anand, G. Shu and P.K. Hanumolu, Oregon State Univ., USA

C280

SESSION 23 - Embedded Processing [Suzaku I]

Friday, June 14, 16:15-17:55

Chairpersons: M. Hariyama, Tohoku Univ.
L. Cheng, Oracle

23-1 - 16:15

A 1Gbps LTE-Advanced Turbo-Decoder ASIC in 65nm CMOS, S. Belfanti, C. Roth, M. Gautschi, C. Benkeser and Q. Huang, ETH Zurich, Switzerland

C284

23-2 - 16:40

A 1.59Gpixel/s Motion Estimation Processor with -211-to-211 Search Range for UHDTV Video Encoder, J. Zhou, D. Zhou, G. He and S. Goto, Waseda Univ., Japan

C286

23-3 - 17:05

A 96.5% Energy-Reduced Lookup Engine with an Unused-Rules-Exception Scheme for Greening Networks, N. Miura*, R. Honda**, S. Shigematsu*, N. Tanaka*, S. Hatta*, M. Nakanishi*, Y. Matsuda** and M. Urano*, *NTT Microsystem Integration Labs. and **Kanazawa Univ., Japan

C288

23-4 - 17:30

Shortstop: An On-Chip Fast Supply Boosting Technique, N. Pinckney, M. Fojtik, B. Giridhar, D. Sylvester and D. Blaauw, Univ. of Michigan, USA

C290

SESSION 24 - Millimeter Wave Transceivers and Systems [Suzaku II]

Friday, June 14, 16:15-17:55

Chairpersons: C.-M. Hung, MStar Semiconductor, Inc.
A. Cathelin, STMicroelectronics

24-1 - 16:15

A Fully-Integrated 77GHz Phase-Array Radar System with 1TX/4RX Frontend and Digital Beamforming Technique, S.-J. Huang, Y.-L. Chen, H.-Y. Chu, P.-N. Chen, H.-Y. Chang, C.-Y. Kuo, C. Kao and J. Lee, National Taiwan Univ., Taiwan **C294**

24-2 - 16:40

A 4-Element 60-GHz CMOS Phased-Array Receiver with Transformer-Based Hybrid-Mode Mixing and Closed-Loop Beam-Forming Calibration, L. Wu*, H.F. Leung*, A. Li*, Z. Hong**, Y. Qin** and H.C. Luong*, *Hong Kong Univ. of Sci. and Tech. and **Fudan Univ., China **C296**

24-3 - 17:05

160GHz Pulsed Transmitter with Packaged Antenna Array in 65nm CMOS, V. Rentala, E. Seok, B. Ginsburg, S. Sankaran, S. Ramaswamy and B. Haroun, Texas Instruments, USA **C298**

24-4 - 17:30

A Low-Power 60-GHz CMOS Transceiver for WiGig Applications, B. Razavi*, Z. Soe**, A. Tham**, J. Chen**, D. Dai**, M. Lu**, A. Khalil**, H. Ma**, I. Lakkis** and H. Law**, *Univ. of California and **Tensorcom, Inc., USA **C300**

Technology SESSION 2 - Highlight [Shunju I, II]

Tuesday, June 11, 10:30-12:10

Chairpersons: S. Chung, National Chiao Tung Univ.
M. Khare, IBM Corp.

2-1 - 10:30

A 22nm High Performance Embedded DRAM SoC Technology Featuring Tri-Gate Transistors and MIMCAP COB, R. Brain, A. Baran, N. Bisnik, H.-P. Chen, S.-J. Choi, A. Chugh, M. Fradkin, T. Glassman, F. Hamzaoglu, E. Hoggan, R. Jahan, M. Jamil, C.-H. Jan, J. Jopling, H. Kan, R. Kasim, S. Kirby, S. Lahiri, B.-C. Lee, D. Lenski, J. Limb, N. Lindert, M. Musorrafiti, J. Neulinger, L. Rockford, J. Park, K. Singh, C. Staus, J. Steigerwald, B. Turkot, P. Vandervoorn, R. Venkatesan, S. Wu, J.-Y. Yeh, Y. Wang, Z. Zhang and K. Zhang, Intel Corp., USA **T16**

2-2 - 10:55

High-Performance Si_{1-x}Ge_x Channel on Insulator Trigate PFETs Featuring an Implant-Free Process and Aggressively- Scaled Fin and Gate Dimensions, P. Hashemi*, M. Kobayashi*, A. Majumdar*, L.A. Yang**, A. Baraskar**, K. Balakrishnan*, W. Kim*, K. Chan*, S.U. Engelmann*, J.A. Ott*, S.W. Bedell*, C.E. Murray*, S. Liang**, R.H. Dennard*, J.W. Sleight*, E. Leobandung* and D.-G. Park*, *IBM Research and **GLOBALFOUNDRIES, USA **T18**

2-3 - 11:20

First Demonstration of Strained Ge-in-STI IFQW pFETs Featuring Raised SiGe75% S/D, Replacement Metal Gate and Germanided Local Interconnects, J. Mitard*, L. Witters*, B. Vincent*, J. Franco*, P. Favia*, A. Hikavy*, G. Eneman*, R. Loo*, D.P. Brunco**, N. Kabir***, H. Bender*, F. Sebaai*, R. Vos*, P. Mertens*, A. Milenin*, E. Vecchio*, L.-Å. Ragnarsson*, N. Collaert* and A. Thean*, *imec, **GLOBALFOUNDRIES and ***assignee at imec, Belgium **T20**

2-4 - 11:45

Thin Organic Photoconductive Film Image Sensors with Extremely High Saturation of 8500 electrons/ μm^2 , M. Mori*, Y. Hirose*, M. Segawa*, I. Miyanaga*, R. Miyagawa*, T. Ueda*, H. Nara*, H. Masuda*, S. Kishimura*, T. Sasaki*, Y. Kato*, Y. Imada**, H. Asano**, H. Inomata**, H. Koguchi**, M. Ihama** and Y. Mishima**, *Panasonic Corp. and **FUJIFILM Corp., Japan