

2013 26th Symposium on Integrated Circuits and Systems Design

(SBCCI 2013)

**Curitiba, Brazil
2 – 6 September 2013**



**IEEE Catalog Number: CFP13237-POD
ISBN: 978-1-4799-1130-1**

SBCCI 2013

26th Symposium on Integrated Circuits and Systems Design



Sessions
Sessions

Session I - SoC, NoC, Embedded I



An Evolutive Approach for Designing Thermal and Performance-Aware Heterogeneous 3D-NoCs
Martha Johanna Sepulveda, Guy Gogniat, Ricardo Pires, Marius Strum and Wang Chau 1

Efficient Memory Access in 2D Mesh NoC Architectures using High Bandwidth Routers
Jan Heisswolf, Simon Bischof, Michael Rueckauer and Juergen Becker 7

Lasio 3D NoC Vertical Links Serialization: Evaluation of Latency and Buffer Occupancy
Yan Ghidini, Matheus Moreira, Lucas Brahm, Thais Webber, Ney Calazans, César Marcon 13

Security-Enhanced 3D Communication Structure for Dynamic 3D-MPSoCs Protection
Martha Johanna Sepulveda, Guy Gogniat, Ricardo Pires, Wang Jiang Chau and Marius Strum 19

H2A: A Hardened Asynchronous Network on Chip
Julian Pontes, Ney Calazans and Pascal Vivet 25

Session II - Analog & RF & Mixed Signal I



A 433/915-MHz Class A/B Power Amplifier Based on Multiresonant Circuits
Fabricio Silva, Robson Lima and Raimundo Freire 31

An RF-Powered Temperature Sensor Designed for Biomedical Applications
Gustavo Campos Martins and Fernando Rangel de Sousa 37

Low-Power/Low-Voltage Analog Front-End for LF passive RFID tag systems
Fernando Paixão Cortes, Guilherme Freitas, Henrique Pimentel, Juan Pablo Brito and Fernando Chavez 43

A 400 MHz Reconfigurable Injection-locking based RC Oscillator for ASK/FSK Modulation
Karoline Brito, Victor Ariel Sobral, Robson Nunes Lima, Fernando Rangel de Sousa and Raimundo Carlos Silvério Freire 49

Session III - Digital, Reconfigurable & Applications I



Real-Time Digital Modulation Classification Based on Support Vector Machines
Edson Sorato, Eduardo P. Fronza, Paulo R.F.M.M. Barbosa, José Luís Guntzel, Adalberto R. Castro and Aldebaro Klautau 53

Power Consumption Analysis in CMOS Static Gates
Alberto Wiltgen Junior, Kim A. Escobar, Andre I. Reis and Renato P. Ribas 59

Combination of Radix-2m Multiplier Blocks and Adder Compressors for the Design of Efficient 2's Complement 64-bit Array Multipliers
Leandro Z. Pieper, Eduardo A. C. da Costa and José C. Monteiro 65

An efficient FPGA implementation in quantum-dot cellular automata
Abner Marciano, André Oliveira, José Augusto M. Nacif and Omar Vilela Neto 71

Design of Crest Factor Reduction techniques based on clipping and filtering for wireless communications systems
Pedro Furtado G. da Silva and Eduardo Gonçalves de Lima 77

Session IV - CAD, Verification & Test I

Improving the Methodology to Build Non-Series-Parallel Transistor Arrangements
Vinicius Possani, Vinicius Callegaro, André I. Reis, Renato P. Ribas, Felipe Marques and Leomar da Rosa Junior 82

Reducing TMR overhead by Combining Approximate Circuit, Transistor Topology and Input Permutations Approaches
Iuri Gomes and Fernanda Kastensmidt 88

Delay Model for Static CMOS Complex Gates
Felipe Marranghelo, Renato P. Ribas and André I. Reis 94

Session V - Analog & RF & Mixed Signal II

A 14b Threshold Configurable Dynamically Latched Comparator for SAR ADCs
Tony Forzley and Ralph Mason 100

A Methodology for the Automatic Design of Operational Amplifiers Including Yield Optimization
Lucas Severo and Alessandro Girardi 105

Temporal Noise Analysis and Measurements of CMOS Active Pixel Sensors Operating in Time Domain
Fernando de Souza Campos, José Alfredo Convolan Ulson, Jacobus W. Swart, Ognian Marinov, M. Jamal Deen and Dib Karam 111

A Resistorless Switched Bandgap Voltage Reference
Hamilton Klimach, Arthur Costa, Moacir Monteiro and Sergio Bampi 116

A CMOS Bandgap Reference Circuit with a Temperature Coefficient Adjustment Block
Eder Ishibe and João Navarro 121

Session VI - Digital, Reconfigurable & Applications II

Gray Encoded Fixed-Point LMS Adaptive Filter Architecture for the Harmonics Power Line Interference Cancelling
Eduardo da Costa, Sérgio Almeida and Mônica Matzenauer 127

A Multiplierless and Low Latency Hardware Design for the 32x32 IDCT of the HEVC Emerging Video Coding Standard
Ruhan Conceição, José Cláudio Souza, Ricardo Jeske, Marcelo Porto, Julio Mattos and Luciano Agostini 133

Energy-speed Exploration for Very-Wide Range of Dynamic V-F Scaling
Kleber Stangherlin and Sergio Bampi 139

Parallel Prefix Adder Design Using Quantum-dot Cellular Automata
Kim Aragon Escobar and Renato P. Ribas 145

Session VII - CAD, Verification & Test II

Analytical Logical Effort Formulation for Minimum Active Area under Delay Constraints
Caio Alegretti, Vinicius Dal Bem, Renato P. Ribas and André I. Reis 151

Synthesis of a Narrow-band Low Noise Amplifier in 180 nm CMOS Technology using Simulated Annealing with Crossovers Operator
Tiago Oliveira Weber, Sergio Chaparro and Wilhelmus A. M. Van Noije 157

Read-Polarity-Once Boolean Functions
Vinicius Callegaro, Mayler G. A. Martins, Renato P. Ribas and André I. Reis 162

Global Routing Congestion Reduction with Cost Allocation Look-ahead
Leandro Nunes and Ricardo Reis 168

Session VIII - Analog & RF & Mixed Signal III



Voltage Regulation System for UHF RFID Tags

Gregorio Zamora Mejía, Jaime Martínez Castillo, Alejandro Díaz Sánchez and José Luis García Gervacio 173

CMOS Smart Temperature Sensors for RFID Applications

Juan Pablo Martinez Brito and Alain Rabaeijns 179

PTAT CMOS Current Sources Mismatch over Temperature

Andre Luiz Aita and Cesar Ramos Rodrigues 185

Session IX - SoC, NoC, Embedded II



A New Code Compression Algorithm and its Decompressor in FPGA-Based Hardware

Wanderson Roger Azevedo Dias, Edward David Moreno and Isaac Nattan Palmeira 189

On the Impacts of Pel Decimation and High-Vt/Low-Vdd on SAD Calculation

Ismael Seidel, Bruno George Moraes, André Beims Bräschler and José Luís A. Güntzel 195

A novel system on chip for software-defined high-speed OFDM signal processing

Joachim Meyer, Michael Dreschmann, Djorn Karnick, Philipp Schindler, Wolfgang Freude, Juerg Leuthold and Jürgen Becker 201

Hybrid Filter for High-Power Converter Systems

Guilherme H. K. Martini and João A. Fabro 207

Implementation of Split-Radix FFT pruning for the reduction of computational complexity in OFDM based cognitive radio system

Myoungseob Lim, Yihu Xu and SungHa Jung 213

Session X - CAD, Verification & Test III



A SystemC Modeling and Simulation Methodology for Fast and Accurate Parallel MPSoC Simulation

Christoph Roth, Harald Bucher, Simon Reder, Florian Buciuman, Oliver Sander and Juergen Becker 218

A Methodology to Evaluate the Aging Impact on Flip-Flops Performance

Cícero Nunes, Paulo Butzen, André I. Reis and Renato P. Ribas 224

Spin Diode Network Synthesis using Functional Composition

Mayler Martins, Felipe Marranghelo, Joseph Friedman, Renato P. Ribas and André I. Reis 230

A new customized concurrent functional testing technique in Digital Microfluidic Biochips

Pranab Roy, Hafizur Rahaman and Parthasarathi Dasgupta N/A

Synthesis of Threshold Logic Gates to Nanoelectronics

Augusto Neutzling, Mayler Martins, Renato P. Ribas and André I. Reis 236

Chip in Curitiba

2013

