

# **2013 International Conference On Simulation Of Semiconductor Processes And Devices**

**(SISPAD 2013)**

**Glasgow, United Kingdom  
3-5 September 2013**



**IEEE Catalog Number: CFP13SSD-POD  
ISBN: 978-1-4673-5735-7**

# Table of Contents and Programme

## Tuesday 3<sup>rd</sup> September

- 08:00      **Registration/Coffee**
- 08:45      **Welcome - Asen Asenov (University of Glasgow/GSS)**
- 08:50      **Keynote - Gary Patton (IBM)**

### Session 1 - Reliability 1

- 09:40      **(Extended) A Detailed Evaluation of Model Defects as**      1  
S1-1      **Candidates for the Bias Temperature Instability**  
*Franz Schanovsky, Oskar Baumgartner, Wolfgang Goes, and Tibor Grasser (TU Wien)*
- 10:10      **3D TCAD Statistical Analysis of Transient Charging in BTI**      5  
S1-2      **Degradation of Nanoscale MOSFETs**  
*Salvatore Maria Amoroso and Louis Gerrer (Device Modelling Group, University of Glasgow), and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)*

### Session 2 - Process Simulation 1

- 09:40      **(Extended) A new kinetic lattice Monte Carlo modeling**      9  
S2-1      **framework for the source-drain selective epitaxial growth process**  
*Renyu Chen and Woosung Choi (Device Laboratory, Samsung Semiconductor Inc.) and Alexander Schmidt, Keun-Ho Lee, and Youngkwan Park (Semiconductor R&D center, Samsung Electronics)*
- 10:10      **A Numerical Model using Phase Field Method for Stress**      13  
S2-2      **Induced Voiding in a Metal Line during Thermal Bake**  
*Yong-Seog Oh (Synopsys, Inc.), Sora Park, Jongsung Jeon, Dong-Cheon Baek, Jin-Seok Kim, and Windu Sari (Samsung Electronics Co.), and Hyerim Lee and Ibrahim Avci (Synopsys Inc.)*

### 10:30      **Coffee Break**

### Session 3 - Reliability 2

- 10:50      **Direct Tunneling and Gate Current Fluctuations**      17  
S3-1      *Oskar Baumgartner, Markus Bina, Wolfgang Goes, Franz Schanovsky, Hans Kosina, and Tibor Grasser (Institute for Microelectronics, TU Wien) and Maria Toledano-Luque and Ben Kaczer (imec)*

11:10 S3-2	<b>Assessment of the Statistical Impedance Field Method for the Analysis of the RTN Amplitude in Nanoscale MOS Devices</b> <i>Giulio Torrente and Niccolo' Castellani (Politecnico di Milano), Andrea Ghetti (Micron Technology), Christian Monzio Compagnoni, Andrea Leonardo Lacaita, and Alessandro Sottocornola Spinelli (Politecnico di Milano), and Augusto Benvenuti (Micron Technology)</i>	21
11:30 S3-3	<b>Quantum Insights in Gate Oxide Charge-Trapping Dynamics in Nanoscale MOSFETs</b> <i>Salvatore Maria Amoroso (Device Modelling Group, University of Glasgow), Jean Michel Sellier (IICT, Bulgarian Academy of Sciences), Mihail Nedjalkov (Institute for Microelectronics, TU Wien), Louis Gerrer (Device Modelling Group, University of Glasgow), Ivan Dimov (IICT, Bulgarian Academy of Sciences), Siegfried Selberherr (Institute for Microelectronics, TU Wien), and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)</i>	25
11:50 S3-4	<b>A Physics-Based Statistical Model for Reliability of STT-MRAM Considering Oxide Variability</b> <i>Chih-Hsiang Ho, Soo Youn Kim, Yusung Kim, Dongsoo Lee, Georgios D. Panagopoulos, and Kaushik Roy (Purdue University)</i>	29

#### Session 4 - Process Simulation 2

10:50 S4-1	<b>Dopant dynamics and defects evolution in implanted silicon under laser irradiations: a coupled continuum and Kinetic Monte Carlo approach</b> <i>G. Fiscaro (CNR IMM), L. Pelaz, M. Aboy, and P. Lopez (Department of Electronics, University of Valladolid), M. Italia (CNR IMM), K. Huet (Excico), F. Cristiano (LAAS CNRS), Z. Essa (LAAS CNRS/STMicroelectronics), Q. Yang and E. Bedel-Pereira (LAAS CNRS), M. Hackenberg (Fraunhofer Institute for Integrated Systems and Device Technology), P. Pichler (Fraunhofer Institute for Integrated Systems and Device Technology/ University of Erlangen-Nuremberg), M. Quillec and N. Taleb (Probion), and A. La Magna (CNR IMM)</i>	33
11:10 S4-2	<b>Donor deactivation at high doping limit: donor pair and impurity band model</b> <i>Chihak Ahn and Woosung Choi (Samsung Semiconductor Inc.), Hiroyuki Kubotera and Yasuyuki Kayama (Samsung R&amp;D Institute of Japan), Alexander Schmidt, Keunho Lee, and Youngkwan Park (Samsung Semiconductor R&amp;D center), and Nick E. B. Cowern (Newcastle University)</i>	37

11:30 S4-3	<b>Atomistic Study of Sulfur Diffusion and S<sub>2</sub> Formation in Silicon during Low-temperature Rapid Thermal Annealing</b> <i>Takahisa Kanemura (Center for Semiconductor Research and Development, Semiconductor &amp; Storage Products Company, Toshiba Corporation), Koichi Kato (Advanced LSI Technology Laboratory, Corporate Research and Development Center, Toshiba Corporation), and Hiroyoshi Tanimoto, Nobutoshi Aoki, and Yoshiaki Toyoshima (Center for Semiconductor Research and Development, Semiconductor &amp; Storage Products Company, Toshiba Corporation)</i>	41
11:50 S4-4	<b>Epitaxial Volmer-Weber Growth Modelling</b> <i>Raffaele A. Coppeta (Institut für Mikroelektronik an der TU Wien), Hajdin Ceric (Christian Doppler Laboratory for Reliability Issues in Microelectronics at the Institute for Microelectronics), Tibor Grasser (Institut für Mikroelektronik an der TU Wien), and Bala Karunamurthy (KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH)</i>	45
12:10	<b>Lunch</b>	
13:30	<b>Plenary - Chenming Hu (University of California, Berkley)</b> <b>Compact Modeling for the Changing Transistor</b> <i>Chenming Hu (University of California, Berkeley)</i>	49
<b>Session 5 - Compact Models</b>		
14:10 S5-1	<b>Recent Enhancements in BSIM6 Bulk MOSFET Model</b> <i>H. Agarwal (IIT Kanpur), S. Venugopalany (University of California Berkeley), M.-A. Chalkiadakia (Ecole Polytechnique Federale de Lausanne), N. Paydavosi and J. P. Duarte (University of California Berkeley), S. Agnihotri, C. Yadav, P. Kushwaha and Y. S. Chauhan (IIT Kanpur), C. Enz (Ecole Polytechnique Federale de Lausanne), A. Niknejd, and C. Hu (University of California Berkeley)</i>	53
14:30 S5-2	<b>An Accurate Compact Modelling Approach for Statistical Ageing and Reliability</b> <i>Jie Ding (Device Modelling Group, University of Glasgow), Dave Reid and Campbell Millar (GSS), and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)</i>	57
14:50 S5-3	<b>Compact Modeling for Application-Specific High-Sigma Worst Case</b> <i>Hsuan-Han Wang, Yi-Ling Chen, Chang-Chieh Yang, Chung-Kai Lin, and Min-Chie Jeng (Taiwan Semiconductor Manufacturing Company)</i>	61

## Session 6 - Interconnects & Contacts

<b>14:10</b>	<b>Stress Estimation in Open Tungsten TSV</b>	65
S6-1	<i>Anderson Singulani, Hajdin Ceric, and Siegfried Selberherr (TU Wien)</i>	
<b>14:30</b>	<b>Limits of specific contact resistivity to Si, Ge, and III-V semiconductors using interfacial layers</b>	69
S6-2	<i>Gautam Shine and Krishna C. Saraswat (Stanford University)</i>	
<b>14:50</b>	<b>Impact of Intermetallic Compound on Solder Bump Electromigration Reliability</b>	73
S6-3	<i>Hajdin Ceric, Anderson Pires Singulani, Roberto Lacerda de Orio, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)</i>	
<b>15:10</b>	<b>Coffee Break</b>	

## Session 7 - Nanowires

<b>15:30</b>	<b>A Tight-binding Study of Channel Modulation in Atomic-scale Si:P Nanowires</b>	77
S7-1	<i>Hoon Ryu (Korea Institute of Science and Technology Information), Sunhee Lee (Samsung Advanced Institute of Technology), Bent Weber, Suddhasatta Mahapatra, and Michelle Y. Simmons (Centre for Quantum Computer Technology, University of New South Wales), Lloyd C. L. Hollenberg (Centre for Quantum Computer Technology, University of Melbourne), and Gerhard Klimeck (Network for Computational Nanotechnology, Purdue University)</i>	
<b>15:50</b>	<b>Full band calculations of low-field mobility in p-type Silicon nanowire MOSFETs</b>	81
S7-2	<i>Neophytos Neophytou, Zlatan Stanojevic, and Hans Kosina (Institute for Microelectronics, Technical University of Vienna)</i>	
<b>16:10</b>	<b>Electrostatics and Ballistic Transport Studies in Junctionless Nanowire Transistors</b>	85
S7-3	<i>Tsung-Hsing Yu, Ethan Hsu, C-W Liu, J.P. Colinge, Y-M Sheu, Jeff Wu, and C.H. Diaz (TSMC)</i>	
<b>16:30</b>	<b>Strain effects on transport properties of Si nanowire devices</b>	89
S7-4	<i>Viet-Hung Nguyen (L_Sim, SP2M, UMR-E CEA/UJF-Grenoble 1), François Triozon (CEA, LETI, MINATEC Campus), and Yann-Michel Niquet (L_Sim, SP2M, UMR-E CEA/UJF-Grenoble 1)</i>	
<b>16:50</b>	<b>Impact of Band Non-parabolicity on the Onset Voltage in a Cylindrical Tunnel Field-effect Transistor</b>	93
S7-5	<i>H. Carrillo-Nuñez (IM2NP), Wim Magnus (Departement Fysica, Universiteit Antwerpen/imec), William G. Vandenberghe (University of Texas at Dallas, Department of Materials Science and Engineering) Bart Sorée (Departement Fysica, Universiteit Antwerpen/imec) and François M. Peeters (Departement Fysica, Universiteit Antwerpen)</i>	

## Session 8 - Technology

15:30 S8-1	<b>22nm Technology Yield Optimization Using Multivariate 3D Virtual Fabrication</b> <i>Benjamin R. Cipriany (IBM), David M. Fried (Coventor), Basanth Jagannathan and Gregory Costrini (IBM), Ken Greiner (Coventor), Ahmed Nayaz Noemaun, Katsunori Onishi, Shreesh Narasimha, Bidan Zhang, Christopher D. Sheraw, and Jason E. Meiring (IBM), Daniel Faken (Coventor), Mahender Kumar, Karen A. Nummy, and Ning Zhan (IBM), Stephen R. Breit (Coventor), and James P. Norum, Stephen S. Furkay, Rajeev Malik, Paul D. Agnello, and Haraprasad Nanjundappa (IBM)</i>	97
15:50 S8-2	<b>Mechanism of Super Steep Subthreshold Slope Characteristics with Body-Tied SOI MOSFET</b> <i>Takayuki Mori and Jiro Ida (Kanazawa Institute of Technology)</i>	101
16:10 S8-3	<b>Double Patterning: Simulating a Variability Challenge for Advanced Transistors</b> <i>Peter Evanschitzky, Alex Burenkov, and Jürgen Lorenz (Fraunhofer IISB)</i>	105
16:30 S8-4	<b>Fin Bending due to Stress and its Simulation</b> <i>Alp H. Gencer, Dimitrios Tsamados, and Victor Moroz (Synopsys)</i>	109
16:50 S8-5	<b>Understanding Workfunction Tuning in HKMG by Lanthanum Diffusion Combining Simulations and Measurements</b> <i>Alessio Spessot and Christian Caillat (Micron Technology), Romain Ritzenthaler and Tom Schram (imec), and Pierre Fazan (Micron Technology Belgium)</i>	113
17:10	<b>Technical Programme Ends</b>	
18:30	<b>Whisky Tasting</b>	

## Wednesday 4<sup>th</sup> September

09:00	<b>Plenary - Cory Weber (Intel)</b>	
	<b>Technology CAD challenges of modeling multi-gate transistors</b>	117
	<i>Cory Weber, Dipanjan Basu, Roza Kotlyar, and Saurabh Morarka (Process Technology Modeling, Intel Corporation)</i>	

### Session 9 - Variability

09:40 S9-1	<b>(Extended) Effects of Phonon Scattering on Discrete-Impurity-Induced Current Fluctuation in Silicon Nanowire Transistors</b>	119
	<i>Nobuya Mori (Osaka University), Masashi Uematsu (Keio University), Gennady Mil'nikov and Hideki Minari (Osaka University), and Kohei M. Itoh (Keio University)</i>	
10:10 S9-2	<b>Simulation of Correlated Line-Edge Roughness in Multi-Gate Devices</b>	123
	<i>Xiaobo Jiang, Runsheng Wang, Jiang Chen, and Ru Huang (Peking University)</i>	

### Session 10 - Novel Materials & Devices 1

09:40 S10-1	<b>(Extended) Fast Simulation of Spin Transfer Torque Devices in a General Purpose TCAD Device Simulator</b>	127
	<i>Frederik Ole Heinz (Synopsys Switzerland) and Lee Smith (Synopsys Inc.)</i>	
10:10 S10-2	<b>Change of the Electronic Conductivity of Graphene Nanoribbons and Carbon Nanotubes Caused by a Local Deformation</b>	131
	<i>Masato Ohnishi, Ken Suzuki, and Hideo Miura (Tohoku University)</i>	
10:30	<b>Coffee Break</b>	

### Session 11 - FinFETs

10:50 S11-1	<b>Unified FinFET Compact Model: Modelling Trapezoidal Triple-Gate FinFETs</b>	135
	<i>Juan Pablo Duarte, Navid Paydavosi, Sriramkumar Venugopalan, Angada Sachid, and Chenming Hu (University of California, Berkeley)</i>	
11:10 S11-2	<b>Unified Compact Modelling Strategies for Process and Statistical Variability in 14-nm node DG FinFETs</b>	139
	<i>X. Wang and B. Cheng (Device Modelling Group, University of Glasgow), A. R. Brown, C. Millar, C. Alexander, and D. Reid (GSS), J. B. Kuang and S. Nassif (IBM Austin Research Lab) and A. Asenov (Device Modelling Group, University of Glasgow/GSS)</i>	

11:30 S11-3	<b>Performance Advantage and Energy Saving of Triangular-Shaped FinFETs</b> <i>Kehuey Wu (National Nano Device Laboratories) and Wei-Wen Ding and Meng-Hsueh Chiang (Department of Electronic Engineering, National Ilan University)</i>	143
11:50 S11-4	<b>A Comparative Study of Fin-Last and Fin-First SOI FinFETs</b> <i>Darsen Lu, Josephine Chang, Michael A. Guillorn, Chung-Hsun Lin, Jeffrey Johnson, Phil Oldiges, Ken Rim, Mukesh Khare, and Wilfried Haensch (IBM Research)</i>	147

**Session 12 - Novel Materials & Devices 2**

10:50 S12-1	<b>Ab-initio and Continuum Simulation of High-Field Chemistry of Diphenylgermane and Diphenylsilane for Scanning Probe Direct Write</b> <i>Wenjun Jiang (Department of Physics, University of Washington), Marco Rolandi (Department of Materials Science &amp; Engineering, University of Washington), Haoyu Lai (Department of Electrical Engineering, University of Washington) and Scott T. Dunham (Department of Electrical Engineering, University of Washington)</i>	149
11:10 S12-2	<b>A Modified Top-of-the-Barrier Solver for Graphene and Its Application to Predict RF Linearity</b> <i>Ahsan U. Alam, Kyle D. Holland, and Sabbir Ahmed (Department of Electrical and Computer Engineering, University of Alberta), Diego Kienle (Theoretische Physik I, Universitat Bayreuth), and Mani Vaidyanathan (Department of Electrical and Computer Engineering, University of Alberta)</i>	155
11:30 S12-3	<b>Impact of near-contact barriers on the subthreshold slope of short-channel CNTFETs</b> <i>Martin Claus (Technische Universität Dresden, Germany), Stefan Blawid (Universidade de Brasília, Brazil), and Michael Schröter (UC San Diego, USA)</i>	159
11:50 S12-4	<b>Performance Analysis and Comparison of Two 1T/1MTJ-based Logic Gates</b> <i>Hiwa Mahmoudi, Thomas Windbacher, Viktor Sverdlov, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)</i>	163
12:10	<b>Lunch</b>	
13:30	<b>Plenary - Jeff Wu (TSMC)</b> <b>Expanding Role of Predictive TCAD in Advanced Technology Development</b> <i>Jeff Wu and C. H. Diaz (TSMC)</i>	167



### Session 13 - Monte Carlo Transport

14:10 S13-1	<b>Efficient 3D Monte Carlo Simulation of Orientation and Stress Effects in FinFETs</b> <i>Fabian Bufler and Frederik Ole Heinz (Synopsys Schweiz GmbH) and Lee Smith (Synopsys Inc.)</i>	172
14:30 S13-2	<b>Toward computationally efficient Multi-Subband Monte Carlo Simulations of Nanoscale MOSFETs</b> <i>Patrik Osgnach, Alberto Revelant, Daniel Lizzit, Pierpaolo Palestri, David Esseni, and Luca Selmi (DIEGM, University of Udine)</i>	176
14:50 S13-3	<b>Density Functional and Monte Carlo-based Electron Transport Simulation in 4H-SiC(0001)/SiO<sub>2</sub> DMOSFET Transition Region</b> <i>S. Salemi, D. P. Ettisserry, A. Akturk, and N. Goldsman (University of Maryland) and A. Lelis (US Army Research Lab)</i>	180

### Session 14 - TCAD

14:10 S14-1	<b>Density Gradient calibration for 2D quantum confinement : Tri-Gate SOI transistor application</b> <i>Nicolas Pons, François Triozon, and Marie-Anne Jaud (CEA-LETI), Remi Coquand (CEA-LETI/STMicroelectronics), Sébastien Martinie (CEA-LETI), Yann-Michel Niquet and V.-H Nguyen (CEA-INAC), and Anouar Idrissi-El Oudrhiri and Sylvain Barraud (CEA-LETI)</i>	184
14:30 S14-2	<b>Impact of Back-end-of-line on Thermal Impedance in SiGe HBTs</b> <i>Amit Kumar Sahoo, Sébastien Fregonese, Mario Weiß, C. Maneux, Nathalie Malbert, and Thomas Zimmer (Laboratoire IMS, CNRS - UMR 5218, Université de Bordeaux 1)</i>	188
14:50 S14-3	<b>Quantum Confinement Point of View for Mobility and Stress Responses on (100) and (110) Single-Gate and Double-Gate nMOSFETs</b> <i>Anson C-C Wang, Edward Chen, Tzer-Min Shen, Jeff Wu, and Carlos H. Diaz (TSMC)</i>	192

## Poster Session

15:10

- P1 **3-D Simulation of Silicon Oxidation: Challenges, Progress and Results** 196  
*Damrong Guoy, Alp H. Gencer, Zhiqiang Tan, Satish Chalasani, Mark Johnson, Luis Villablanca, and Simeon Simeonov (Synopsys)*
- P2 **TCAD Modeling and Simulation of Non-Resonant Plasmonic THz Detector Based on Asymmetric Silicon MOSFETs** 200  
*Min Woo Ryu, Jeong Seop Lee, and Kibog Park (Ulsan National Institute Science and Technology), Wook-Ki Park and Seong-Tae Han (Korea Electrotechnology Research Institute), and Kyung Rok Kim (Ulsan National Institute Science and Technology)*
- P3 **Circuit-level modeling of FinFet sub-threshold slope and DIBL mismatch beyond 22nm** 204  
*Pablo Royer (Universidad Politécnica de Madrid), Paul Zuber (IMEC), and Binjie Cheng and Asen Asenov (University of Glasgow) and Marisa López-Vallejo (Universidad Politécnica de Madrid)*
- P4 **Modeling the Growth of Thin SnO<sub>2</sub> Films using Spray Pyrolysis Deposition** 208  
*Lado Filipovic and Siegfried Selberherr (Institute for Microelectronics, TU Wien), Giorgio Cataldo Mutinati, Elise Brunet, Stephan Steinhauer, and Anton Koeck (Molecular Diagnostics, Health & Environment, AIT GmbH), Jordi Teva, Jochen Kraft, Joerg Siebert, and Franz Schrank (ams AG), and Christian Gspan and Werner Grogger (Institute for Electron Microscopy and Fine Structure Research, Graz University of Technology and Centre for Electron Microscopy Graz)*
- P5 **Modeling Direct Band-to-Band Tunneling using QTBM** 212  
*Lidija Filipovic, Oskar Baumgartner, and Hans Kosina (TU Wien, Institute for Microelectronics)*
- P6 **Nonlinear PCA for Source Optimization in Optical Lithography** 216  
*Pardeep Kumar (Research Scholar) and Babji Srivasan and Nihar R. Mohapatra (Assistant Professor)*
- P7 **PDK development of 10nm III-V/Ge IFQW CMOS technology including statistical variability** 220  
*Si-Yu Liao, Ewan A. Towie, Daniel Balaz, and Craig Riddet (Device Modelling Group, University of Glasgow) and Binjie Cheng and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)*
- P8 **Fast 3D Electro-Thermal Device/Circuit Simulation Based on Automated Interaction of SDevice and HSpice Simulators** 224  
*Aleš Chvála, Daniel Donoval, Juraj Marek, Patrik Príbytný, and Marián Molnár (Institute of Electronics and Photonics, Slovak University of Technology in Bratislava)*

P9	<b>A new time-dependent analytic compact model for radiation-induced photocurrent in epitaxial structures</b> <i>Jason C. Verley, Eric R. Keiter, and Charles E. Hembree (Sandia National Laboratories), Carl L. Axness (Sandia National Laboratories (ret.)), and Bert Kerr (New Mexico Institute of Mining and Technology)</i>	228
P10	<b>Influence of Temperature on the Standard Deviation of Electromigration Lifetimes</b> <i>Roberto Lacerda de Orio, Hajdin Ceric, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)</i>	232
P11	<b>Evaluation of Spin Lifetime in Strained UT2B Silicon-On-Insulator MOSFETs</b> <i>Dmitri Osintsev, Viktor Sverdlov, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)</i>	236
P12	<b>Impurity scattering in p-type silicon nanowire FET: k.p approach</b> <i>Nima Dehdashti Akhavan, Gregory Jolley, Gilberto Umana-Membreno, Jarek Antoszewski, and Lorenzo Faraone (University of Western Australia)</i>	PDE
P13	<b>Electromigration Analyses of Open TSVs</b> <i>W. H. Zisser and H. Ceric (Christian Doppler Laboratory for Reliability Issues in Microelectronics at the Institute for Microelectronics) and R. L. de Orio and S. Selberherr (Institute for Microelectronics, TU Wien)</i>	244
P14	<b>Modeling and Simulation of Dopant Segregation at NiSi/Si Interface Using Chemical Potential Approach</b> <i>Ashish kumar and Mark E. Law (University of Florida)</i>	PDE
P15	<b>TCAD study of Single Photon Avalanche Diode on 0.35<math>\mu</math>m High Voltage Technology</b> <i>Frederic Roger, Jordi Teva, Ewald Wachmann, Jong Mun Park, and Rainer Minixhofer (ams AG)</i>	252
P16	<b>3-D Modeling of Fringing Gate Capacitance in Gate-all-Around Cylindrical Silicon Nanowire MOSFETs</b> <i>TaeYoon An and SoYoung Kim (College of Information and Communication Engineering, Sungkyunkwan University, Korea)</i>	256
P17	<b>Simulation of Terahertz Plasmons in Graphene with Grating-Gate Structures</b> <i>A. Satou and V. Ryzhii (Tohoku University), F. T. Vasko and V. V. Mitin (University at Buffalo), and T. Otsuji (Tohoku University)</i>	260
P18	<b>Microtexture Dependence of Stress-induced Migration of Electroplated Copper Thin Film Interconnections Used for 3D Integration</b> <i>Ken Suzuki, Osamu Asai, Ryosuke Furuya, Jaeuk Sung, Naokazu Murata, and Hideo Miura (Tohoku University)</i>	264

P19	<b>Compact Physical Models for Gate Charge and Gate Capacitances of AlGaIn/GaN HEMTs</b> <i>Fetene Mulugeta Yigletu and Benjamin Iñiguez (Dept. of Electrical Electronics and Automation Engineering, Universitat Rovira i Virgili) and Sourabh Khandelwal and Tor Fjeldly (Dept. of Electronics and Telecommunication, Norwegian University of Science and Technology)</i>	268
P20	<b>Efficient Wigner Function Simulation for Nanowire MOSFETs and Comparison to Quantum Drift-Diffusion</b> <i>O. Badami, D.Saha, and S. Ganguly (Indian Institute of Technology, Bombay)</i>	272
P21	<b>Improving subthreshold MSB-EMC simulations by dynamic particle weighting</b> <i>Carlos Sampedro, Francisco Gámiz, and Andrés Godoy (University of Granada), Raul Valin (University of Swansea), and Antonio Garcia-Loureiro (University of Santiago de Compostela)</i>	276
P22	<b>Bridging Design to Manufacturability by Layout Enhanced Analyses Process Simulations</b> <i>Mark Lu, Cong-Shu Zhou, Yi Tian, Chang Liu, Yuan-Wei Zheng, Guo-Zhong You, Qing Yang, Shyue-Fong Quek, Soo-Muay Goh, Hein-Mun Lam, Jian Zhang, Peter Benyon, and Christine P. Tan (GLOBALFOUNDRIES Singapore)</i>	PDE
P23	<b>Compact Modeling of SOI MOSFETs with Ultra Thin Silicon and BOX Layers for Ultra Low Power Applications</b> <i>Yukiya Fukunaga, Mitiko Miura-Mattausch, Uwe Feldmann, and Hideyuki Kikuchihara (Hiroshima University), Tadashi Nakagawa (AIST), and Masataka Miyake and Hans Juergen Mattausch (Hiroshima University)</i>	284
P24	<b>Impact of Back biasing in Ultra Short Channel UTBB SOI nMOSFETs</b> <i>Kai Zhao (Institute of Microelectronics, Peking University), Tiao Lu (School of Mathematical Sciences, LMAM and CAPT, Peking University), and Gang Du, Xiao-yan Liu, and Xing Zhang (Institute of Microelectronics, Peking University)</i>	288
P25	<b>Simulation on Endurance Characteristic of Charge Trapping Memory</b> <i>Zhiyuan Lun, Taihuan Wang, Lang Zeng, Kai Zhao, Xiaoyan Liu, Yi Wang, Jinfeng Kang and Gang Du (Peking University)</i>	292
P26	<b>Analysis of the Latchup Process in High-Voltage Trench-IGBT Cell Arrays</b> <i>Christopher Toechterle (Munich University of Technology), Frank Pfirsch and C. Sandow (Infineon Technologies AG), and Gerhard Wachutka (Munich University of Technology)</i>	296
P27	<b>Globally hyperbolic moment method for solving BTE including phonon scattering</b> <i>Wenqi Yao, Ruo Li, and Tiao Lu (School of Mathematical Science, Peking University) and Xiaoyan Liu, Gang Du, and Kai Zhao (Institute of Microelectronics, Peking University)</i>	300

P28	<b>Influence of the back-gate bias on the electron mobility of trigate MOSFETs</b> <i>Francisco G. Ruiz, Enrique G. Marín, Isabel M. Tienda-Luna, Andrés Godoy, Celso Martínez Blanco, and Francisco Gámiz (University of Granada)</i>	304
P29	<b>Quasi Self-consistent Monte Carlo Particle Simulations of Local Heating Properties in Nano-scale Gallium Nitride FETs</b> <i>Taichi Misawa, Shusuke Oki, and Yuji Awano (Keio University)</i>	308
P30	<b>Performance Evaluation of p-channel FinFETs using 3D Ensemble Monte Carlo Simulation</b> <i>Craig Riddet and Ewan A. Towie (Device Modelling Group, University of Glasgow) and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)</i>	312
P31	<b>Novel Design of Multiple Negative-Differential Resistance (NDR) Device in a 32nm CMOS Technology using TCAD</b> <i>Sunhae Shin and Kyung Rok Kim (UNIST)</i>	316
P32	<b>Analytical Modelling of Current-Voltage Characteristics of Ballistic Graphene Nanoribbon Field-Effect Transistors</b> <i>George S. Kliros (Hellenic Air-Force Academy)</i>	320
P33	<b>Simulating Ion Transport and its Effects in Silicon Carbide Power MOSFET Gate Oxides</b> <i>Daniel B. Habersat and Aivars J. Lelis (U.S. Army Research Laboratory) and Neil Goldsman (Dept. of Electrical and Computer Engineering, University of Maryland)</i>	324
P34	<b>Simulated effect of epitaxial growth variations on THz emission of SiGe/Ge quantum cascade structures</b> <i>Pavlo Ivanov, Alexander Valavanis, Zoran Ikonc, and Robert Kelsall (School of Electronic and Electrical Engineering, University of Leeds)</i>	328
17:00	<b>Technical Programme Ends</b>	
19:00	<b>Conference Dinner</b>	

## Thursday 5<sup>th</sup> September

09:00 Plenary – *Jo Finders (ASML)*

### Session 15 - Circuits

09:40 **(Extended) Evaluating the Accuracy of SRAM Margin** 332  
S15-1 **Simulation Through Large Scale Monte-Carlo Simulations with Accurate Compact Models**

*Plamen Asenov and David New (ARM), Dave Reid and Campbell Millar (GSS), and Scott Roy (University of Glasgow) and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)*

10:10 **Accelerated Variation Simulation through Parameter** 336  
S15-2 **Reduction**

*William "Paul" Griffin II and Kaushik Roy (Purdue University)*

### Session 16 - Memories 1

09:40 **(Extended) Simulation of CBRAM devices with the level set** 340  
S16-1 **method**

*P.Dorion (CEA-LETI & UPMC Univ J.-L Lions Laboratory), O.Cueto, M.Reyboz, E.Vianello, and J.C. Barbé (CEA-LETI), A.Grigoriu (Univ. Paris Diderot,), and Y.Maday (UPMC Univ J.-L Lions Laboratory)*

10:10 **A Unified Model of Metallic Filament Growth Dynamics for** 344  
S16-2 **Conductive-Bridge Random Access Memory**

*Shengjun Qin, Jinyu Zhang, and Zhiping Yu (Institute of Microelectronics, Tsinghua University)*

10:30 **Coffee Break**

### Session 17 - Transport

10:50 **Coupled Drift-Diffusion (DD) and Multi-Subband Boltzmann** 348  
S17-1 **Transport Equation (MSBTE) Solver for 3D Multi-Gate Transistors**

*Seonghoon Jin (Samsung Semiconductor), Sung-Min Hong (GIST), Woosung Choi (Samsung Semiconductor), and Keun-Ho Lee and Youngkwan Park (Samsung Electronics)*

11:10 **Surface-Roughness-Scattering in Non-Planar Channels -- the** 352  
S17-2 **Role of Band Anisotropy**

*Zlatan Stanojevic and Hans Kosina (TU Wien, Institute for Microelectronics)*

11:30 S17-3	<b>A self-consistent solution of the Poisson, Schrödinger and Boltzmann equations by a full Newton-Raphson approach for nanoscale semiconductor devices</b> <i>Dino Ruic and Christoph Jungemann (ITHE RWTH Aachen University)</i>	356
11:50 S17-4	<b>Spherical Harmonics Solver for a Coupled Hot-Electron-Hot-Phonon System</b> <i>Mindaugas Ramonas (RWTH Aachen University/Center for Physical Sciences and Technology, SPI) and Christoph Jungemann (RWTH Aachen University)</i>	360

## Session 18 - Memories 2

10:50 S18-1	<b>An Analytical Model for Predicting Forming/Switching Time in Conductive-Bridge Resistive Memory (CBRAM)</b> <i>Shaoli Lv (CAD Institute, Hangzhou Dianzi University), He Wang and Jinyu Zhang (Institute of Microelectronics, Tsinghua University), Jun Liu and Lingling Sun (CAD Institute, Hangzhou Dianzi University) and Zhiping Yu (Institute of Microelectronics, Tsinghua University)</i>	364
11:10 S18-2	<b>Rigorous Simulation Study of a Novel Non-Volatile Magnetic Flip Flop</b> <i>Thomas Windbacher, Hiwa Mahmoudi, Viktor Sverdlov, and Siegfried Selberherr (Institute for Microelectronics, TU Wien)</i>	368
11:30 S18-3	<b>A hybrid spin-charge mixed-mode simulation framework for evaluating spin-transfer torque MRAM bit-cells utilizing multiferroic tunneling junctions</b> <i>Xuanyao Fong and Kaushik Roy (Purdue University)</i>	372
11:50 S18-4	<b>Addressing Key Challenges in 1T-DRAM: Retention Time, Scaling and Variability - Using a Novel Design with GaP Source-Drain</b> <i>Ashish Pal, Aneesh Nainani and Krishna Saraswat (Stanford University)</i>	376

12:10      **Lunch**

13:30      **Plenary – Gerhard Klimeck (Purdue University)**

## Session 19 - III-V Devices

14:10 S19-1	<b>Atomistic simulation of a III-V p-i-n junction</b> <i>Kurt Stokbro, Anders Blom, and Søren Smidstrup (QuantumWise)</i>	380
14:30 S19-2	<b>Comparison of Raised Source/Drain Implant-Free Quantum-Well and Tri-Gate MOSFETs using 3D Monte Carlo Simulation</b> <i>Ewan Towie and Craig Riddet (Device Modelling Group, University of Glasgow) and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)</i>	384

14:50 S19-3	<b>Calculation of the valence band structures in strained In<sub>0.7</sub>Ga<sub>0.3</sub>As devices with different surface orientation</b> <i>Pengying Chang, Lang Zeng, Xiaoyan Liu, Wei Kangliang, Jiayu Qin, Kai Zhao, Gang Du, and Xing Zhang (Peking University)</i>	388
----------------	---	-----

## Session 20 - Models & Methodologies 1

14:10 S20-1	<b>First-principle investigation of Ti wetting layer influence on metal-graphene contact</b> <i>Xiang Ji, Yan Wang, and Zhiping Yu (Tsinghua University)</i>	392
----------------	---	-----

14:30 S20-2	<b>Identification and Quantification of 4H-SiC (0001)/SiO<sub>2</sub> Interface Defects by Combining Density Functional and Device Simulations</b> <i>D.P. Ettisserry, S. Salemi, N. Goldsman, S. Potbhare, and A. Akturk (Dept. of ECE, University of Maryland) and A. Lelis (U.S. Army Research Laboratory)</i>	396
----------------	--	-----

14:50 S20-3	<b>Quantitative Full 3D Blooming Analysis on 1.4um BSI CMOS Image Sensor</b> <i>Mitsuhiro Sengoku (Technology CAD Group, Toshiba I.S. Corp.) and Hisao Yoshimura, Yuki Sugiura, Sakiko Shimizu, Ryoji Hasumi, and Makoto Monoi (Analog &amp; Imaging IC Div. Toshiba Corp. S&amp;S Products Company)</i>	400
----------------	---	-----

15:10 **Coffee Break**

## Session 21 - Quantum Transport

15:30 S21-1	<b>Two-dimensional Transient Wigner Particle Model</b> <i>Jean Michel Sellier (IICT, Bulgarian Academy of Sciences), Mihail Nedjalkov (Institute for Microelectronics, TU Wien), Ivan Dimov (IICT, Bulgarian Academy of Sciences), and Siegfried Selberherr (Institute for Microelectronics, TU Wien)</i>	404
----------------	--	-----

15:50 S21-2	<b>Comparison of Ballistic Transport Characteristics of Monolayer Transition Metal Dichalcogenides (TMDs) MX<sub>2</sub> (M = Mo, W; X = S, Se, Te) n-MOSFETs</b> <i>Jiwon Chang, Leonard F. Register, and Sanjay K. Banerjee (The University of Texas at Austin)</i>	408
----------------	--	-----

16:10 S21-3	<b>One-shot current conserving approach of phonon scattering treatment in nano-transistors</b> <i>M. Bescond, E. Dib, C. Li, H. Mera, N. Cavassilas, F. Michelini, and M. Lannoo (IM2NP - CNRS)</i>	412
----------------	--	-----

16:30 S21-4	<b>Interactions Between Precisely Placed Dopants and Interface Roughness in Silicon Nanowire Transistors: Full 3-D NEGF Simulation Study</b> <i>Vihar P. Georgiev and Ewan A. Towie (Device Modelling Group, University of Glasgow) and Asen Asenov (Device Modelling Group, University of Glasgow/GSS)</i>	416
----------------	--	-----



16:50 S21-5	<b>Quantum Transport Simulation of Bilayer Pseudospin Field-Effect Transistor (BisFET) on Tight-binding Hartree-Fock Model</b> <i>Xuehao Mou, Leonard F. Register, and Sanjay K. Banerjee (The University of Texas at Austin, United States)</i>	420
----------------	---	-----

## Session 22 - Models & Methodologies 2

15:30 S22-1	<b>The Novel Stress Simulation Method for Contemporary DRAM Capacitor Arrays</b> <i>Kyu-Baik Chang, Yun Young Kim, Jiwoong Sue, Hojoon Lee, Won-Young Chung, Keun-Ho Lee, Young-Kwan Park and EunSeung Jung (Semiconductor R&amp;D Center, Samsung Electronics), and Ilsub Chung (Sungkyunkwan University)</i>	424
15:50 S22-2	<b>Microscopic Description of the Inter-Trap Transitions in a-Chalcogenides</b> <i>Massimo Rudan, Fabio Giovanardi, and Fabrizio Buscemi (ARCES and DEI - University of Bologna), Rossella Brunetti (FIM - University of Modena and Reggio Emilia), and Giuliano Marcolini (ARCES and DEI - University of Bologna)</i>	428
16:10 S22-3	<b>Modeling of Reliability Issues in RF MEMS Switches</b> <i>Gabriele Schrag, Thomas Kuenzig, and Gerhard Wachutka (Munich University of Technology)</i>	432
16:30 S22-4	<b>3D-nHD: A hydrodynamic model for trap-limited conduction in a 3D network</b> <i>Andrea Cappelli (FIM Department - University of Modena and Reggio Emilia), Enrico Piccinini (ARCES - University of Bologna), Feng Xiong and Ashkan Behnam (MNTL - University of Illinois at Urbana-Champaign), Rossella Brunetti (FIM Department - University of Modena and Reggio Emilia), Eric Pop (MNTL - University of Illinois at Urbana-Champaign), and Carlo Jacoboni (FIM Department - University of Modena and Reggio Emilia)</i>	436
16:50 S22-5	<b>A Process/Device/Circuit/System Compatible Simulation Framework for Poly-Si TFT Based SRAM Design</b> <i>Chen-Wei Lin (NCTU, Taiwan), Chih-Hsiang Ho and Chao Lu (Purdue University), Mango C.-T. Chao (NCTU, Taiwan), and Kaushik Roy (Purdue University)</i>	440
17:10	<b>Technical Programme Ends</b>	

## Appendix – Workshop Papers

### MORDRED Workshop

**Experimental characterization of BTI defects** 444

*B. Kaczer (imec), V. V. Afanas'ev (KUL), K. Rott (Infineon), F. Cerbu (KUL), J. Franco (imec), W. Goes and T. Grasser (TUW), O. Madia, A.P.D. Nguyen, and A. Stesmans (KUL), H. Reisinger (Infineon), and M. Toledano-Luque and P. Weckx (imec)*

**Advanced Modeling of charge trapping in oxide defects** 451

*Franz Schanovsky, Wolfgang Gös, and Tibor Grasser (Institute for Microelectronics, TU Wien, Austria)*

**Author Index** 459