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*Monday, September 23 – Wednesday, September 25*

## Educational Sessions

*Tuesday, September 24 and Wednesday, September 25*

## Session 1 – Plenary Session

Monday, 9/23/2013, 8:15 am
Oak Ballroom
8:15 am
Welcome and Opening Remarks
Awards Presentations
Keynote Speaker Introduction
Aurangzeb Khan, Altia Systems

**Keynote Presentation**
**Digital Analog Design**
**Mark Horowitz, Stanford University**

The past 30 years have seen an enormous growth in the power and sophistication of digital design tools, while progress in analog tools has been much more modest. Digital tools use many abstractions to allow them to validate implementations match the functional models, and the composition of cells matches the composition of the functional models. While there are many reasons why this is more difficult for analog circuits, it can be done. To prove this point, this talk presents how to leverage the fact that the result surface of analog designs are smooth to create ways to formally validate analog models to instances, define analog fault models, and even efficiently explore the effect of process variations.

## Session 2 -- Microsystems for Biomedical and Sensing Applications

Monday, 9/23, 10:00 am
Oak Ballroom
**Session Chair:** Christophe Antoine, Analog Devices
**Session Co-Chair:** Stephen O'Driscoll, University of California, Davis

10:00 am **Introduction**

Biomedical and sensing applications present new challenges for IC and system designers. In this session, five papers representing advances in these areas are presented.



This paper describes a broadband biosensor interface IC as part of a miniaturized measurement platform for MHz-to-GHz dielectric spectroscopy. Developed in 0.35μm 2P/4M RF CMOS, the IC measures the frequency-dependent S21 magnitude and phase of a

microfabricated microfluidic dielectric sensor, when the sensor is loaded with a solution-under-test (SUT).

10:30 am 2-2 **Capacitive Proximity Communication with Distributed Alignment Sensing for Origami Biomedical Implants,** *M. Loh, A. Emami-Neyestanak, California Institute of Technology* **5**

Origami implant design is a 3D integration technique which addresses size and cost constraints in biomedical implants. A capacitive proximity interconnect that enables this technique is presented. It embeds an alignment sensor that measures link quality directly and simplifies adaptation to alignment. The sensor and transceiver share functional blocks, saving power and area. Data rates 10-60 Mbps are achieved over 4-12µm parylene-C, with efficiencies up to0.180 pJ/bit.

10:55 am 2-3 **An Active Rectifier/Regulator Combo Circuit for Powering Biomedical Implants,** *E. Lee, Alfred Mann Foundation* **9**

A circuit that combines an active rectifier and a linear regulator, which will be referred to as a rectulator, is proposed in this paper. The main transistor in the rectulator is used for both the rectification of the AC input (VAC) and the regulation of the DC output (VO) to reduce the overall voltage drop between VAC and VO. The rectulator has a high power efficiency (nP) and very good amplitude modulation (am) rejection on VAC against AC field strength variations. A full-wave rectulator implemented in a 0.18µm CMOS process showed an AM rejection > 45dB for an AM frequency < 2kHz. A nP of 90.7% was measured for an input frequency of 5MHz, VO = 2.5V and an output power of 10.5mW.

11:20 am 2-4 **65nW CMOS Temperature Sensor for Ultra-Low Power Microsystems,** *Seokhyeon Jeong, Jae-yoon Sim*, David Blaauw, Dennis Sylvester, University of Michigan, *Pohang University of Science and Technology* **13**

A temperature sensor using a novel process-invariant temperature sensing element and voltage to current converter is proposed for battery-operated ultra-low power micro systems. Measurements from a 180nm CMOS test chip show power consumption of 65nW with an inaccuracy of +1.3℃/-1.4℃ over a temperature range of 0℃ to 100℃ after 2-point calibration.

11:45 am 2-5 **Design and Characterization of Electronic Sensing System for a 13 x 13 Biomechanical Ground Reaction Sensor Array,** *Q. Guo, M. A. Suster*, R. Surapaneni, C. H. Mastrangelo and D. J. Young, The University of Utah, *Case Western Reserve University* **17**

This paper presents the design and characterization of an electronic sensing system interfaced with a high-density flexible biomechanical ground reaction sensor array. The prototype system can measure real-time ground force, shear strain and sole deformation associated with a human bipedal locomotion, thus providing zero-velocity correction to an inertial measurement unit to improve navigation accuracy.

## Session 3 -- High-Speed Wireline Timing Recovery and PLLs

Monday, 9/23, 10:00 am
Fir Ballroom
**Session Chair:** Samuel Palermo, Texas A&M University
**Session Co-Chair:** Kimo Tam, Analog Devices

10:00 am **Introduction**

This session presents various design techniques for ADC-based and burst-made timing recovery systems and PLLs with peaking-free transfer functions and low-area utilization.

10:05 am 3-1 **Design Metrics for Blind ADC-Based Wireline Receivers (Invited),** *Ali Sheikholeslami and Hirotaka Tamura*, University of Toronto and *Fujitsu Labs* **21**

This paper compares blind ADC-based receivers against binary and phase-tracking ADC-based receivers in terms of their design complexity and cost, and derives equations that relate the required ADC resolution (ENOB) to channel loss and to the characteristics of the FFE/DFE that follow the ADC.

10:55 am 3-2 **A 10Gbps, 1.24pJ/bit, Burst-Mode Clock and Data Recovery with Jitter Suppression,** *Ming-Chiuan Su, Wei-Zen Chen, Pei-Si Wu*, Yu-Hsian Chen*, Chao-Cheng Lee*, Shyh-Jye Jou, National Chiao Tung University, *Realtek Corp.* **29**

A 10Gbps, 1/5 rate burst mode CDR is reconfigurable between data gating and phase tracking modes to achieve instantaneous phase-locking with low jitter suppression. Incorporated with 1:5 demultiplexer, it achieves a high energy efficiency of 1.24pJ/bit. The prototype chip is fabricated in UMC 55nm CMOS technology.

11:20 am 3-3 **A 9.2-GHz Digital Phase-Locked Loop with Peaking-Free Transfer Function,** *Sigang Ryu, Hwanseok Yeo, Yoontaek Lee, Seuk Son, Jaeha Kim, Seoul National University* **33**

This paper describes a digital phase-locked loop (PLL) that realizes a peaking-free jitter transfer. That is, the PLL's second-order transfer function does not have a closed-loop zero. Such a PLL does not exhibit overshoots in the phase step response and achieves fast settling. Unlike the previously-reported peaking-free PLLs, the proposed PLL implements the peaking-free loop filter directly in digital domain without requiring additional components. A time-to-digital converter (TDC) is implemented as, a set of three binary phase-frequency detectors that over sample the timing error with time-varying offsets, achieving a linear TDC gain and PLL bandwidth insensitive to the jitter condition. And a 9.2-GHz digitally-controlled LC oscillator (DCO) with transformer-based tuning realizes a predictable DCO gain set by a ratio between two digitally-controlled currents. The prototype 9.2-GHz-output digital PLL fabricated in a 65nm CMOS demonstrates a fast settling time of 1.58-μs with 700-kHz bandwidth. The PLL has a 3.477-psrms divided clock jitter and -120dBc/Hz phase noise at 10-MHz offset while dissipating 63.9-mW at a 1.2-V supply.

11:45 am 3-4 **A Sub-200 fs RMS Jitter Capacitor Multiplier Loop Filter-Based PLL in 28 nm CMOS for High-Speed Serial Communication Applications,** *Burak Çatl, Ali Nazemi, Tamer Ali, Siavash Fallahi, Yang Liu, Jaehyup Kim, Mohammed Abdul−Latif, Mahmoud Reza Ahmadi, Hassan Maarefi, Afshin Momtaz, and Namik Kocaman, Broadcom Corporation* **37**

An 8.0 GHz to 12.2 GHz PLL with a capacitor multiplier-based active loop filter is designed in a 28 nm digital CMOS process. A passive loop filter-based version of the PLL is also implemented for comparison. While the PLL area is comparable to that of digital PLLs, the PLL performance is as good as that of an analog PLL that employs a passive loop filter. The capacitor multiplier-based active loop filter PLL has a jitter performance of 198 fs(rms), while its passive loop filter-based counterpart shows a jitter performance of 195 fs (rms). The PLL occupies 0.093 $mm^2$ and consumes 15.5 mA at 1.0V.

## Session 4 -- RF Building Blocks

Monday, 9/23, 10:00 am
Pine Ballroom
**Session Chair:** Andrea Mazzanti, University of Padova
**Session Co-Chair:** Earl McCune

10:00 am **Introduction**

Moving beyond traditional technologies this session presents digital PLL nonlinearity cancellation, integrated tunable duplexer, smartphone T/R switch, and a programmable broadband integrated phase shifter.

10:05 am 4-1 **Nonlinearity Cancellation in Digital PLLs (Invited),** *S. Levantino, C. Samori, Politecnico di Milano* **41**

The spur level in digital fractional-N PLLs is often bounded by TDC resolution and linearity. Methods for mitigating TDC nonlinearity tend to increase phase-noise level. By contrast, PLL architectures based on digital-to-time converters enable nonlinearity cancellation and spur reduction with no added noise at lower design complexity and power consumption.

10:55 am 4-2 **Hybrid Transformer-Based Tunable Integrated Duplexer with Antenna Impedance Tracking Loop,** *S. Abdelhalem, P. Gudem*, L. Larson**, University of California at San Diego, *Qualcomm Inc., **Brown University* **49**

Electrical balance between the antenna and the balance network impedances is crucial for achieving high isolation in a hybrid transformer duplexer. In this paper, an auto calibration loop for tuning a novel integrated balance network to track the antenna impedance variations is introduced. It achieves an isolation of more than 50 dB in the transmit and receive bands, with an antenna VSWR within 2:1, and between 1.7 and 2.2 GHz. The duplexer, along with a cascaded direct-conversion receiver, achieves a noise figure of 5.3 dB, a conversion gain of 45 dB and consumes 34 mA. The insertion loss in the transmit path was less than 3.8 dB. Implemented in a 65-nm CMOS process, the chip occupies an active area of 2.2 $mm^2$.

11:20 am 4-3 **A Smartphone SP10T T/R Switch in 180nm SOI CMOS with 8kV ESD Protection by Co-Design,** *X.S. Wang, X. Wang*, F. Lu**, L. Wang**, R. Ma**, Z. Dong**, L. Sun, A. Wang**, C.P. Yue, D. Wang***, A. Joseph***, University of California, Santa Barbara., *OmniVision Technologies., **University of California, Riverside., ***IBM Microelectronics* **53**

This paper reports the first 8kV+ ESD-protected SP10T transmit/receive (T/R)antenna switch for quad-band (0.85/0.9/1.8/1.9GHz) GSM and multiple WCDMA smartphones fabricated in an 180nm SOI CMOS. A novel physics-based switch-ESD co-design methodology is applied to ensure full-chip optimization for a SP10T test chip and its ESD protection circuit simultaneously.

11:45 am 4-4 **A Lumped Component Programmable Delay Element for Ultra-Wideband Beamforming,** *Naga Rajesh, Shanthi Pavan, Indian Institute of Technology Madras* **57**

We introduce a ladder filter based programmable time delay element for beamforming in Ultra-Wideband (UWB) systems. When compared to conventional methods based on the tapped delay line architecture, our technique achieves lower power dissipation, better area efficiency, and finer delay and gain resolution more efficiently. The proposed architecture is more scalable, has better parasitic absorption capability and highly programmable with delay

and gain resolution dependent only on transconductor resolution. A prototype delay line designed for the 3.1-10.6 GHz UWB range achieves a delay range of 80 ps with 0.5 ps resolution and a gain range of -30 dB to +10 dB with 0.15 dB step. Fabricated in a 0.25 µm SiGe BiCMOS process, the delay element occupies an active area of 1 $mm^2$ and consumes 47 mW from a 2.5 V supply. A four antenna beamforming system using the delay element can achieve scanning range of +/-51deg with resolution of 0.86 deg for antenna spacing of 10 mm.

## Session 5 -- Beyond 14nm Technology Circuit Interaction

Monday, 9/23, 10:00 am
Cedar Ballroom
**Session Chair**: Rajiv Joshi, IBM TJ Watson Research Center
**Session Co-Chair:** Ramnath Venkatraman, LSI Corp.

10:00 am **Introduction**

This session covers technology-circuit interaction needs beyond 14nm including advanced device and lithographic considerations. Multiple patterning and FinFETs add significant complexity. This session further covers efficient methodology and solutions needed for product metrics applied to a myriad of design-technology choices.

10:05 am 5-1 **The Past, Present, and Future of Design-Technology Co-Optimization (Invited),** *G. Yeric, B. Cline, S. Sinha, D. Pietromonaco, V. Chandra, and R. Aitken, ARM* **61**

Design-Technology Co-Optimization (DTCO) has evolved into a multi-faceted, multi-lateral co-optimization below 20nm, where double patterning and FinFETs create significant complexities. Effective DTCO now involves end product metrics applied to a myriad of technology choices. A future of even more complex lithography, devices, and reliability will drive continued evolution in DTCO.

10:55 am 5-2 **From 2D-Planar to 3D-Non_Planar Device Architecture: A Scalable Path Forward? (Invited),** *G. Shahidi, IBM T.J. Watson Research Center* **69**

11:45 am 5-3 **Foundations for Scaling to 7nm and Beyond (Invited),** *R. Schenker, V. Singh, Intel Corporation* **77**

## Session 6 – Forum Session: 20 nm Design Challenges

Monday, 9/23, 1:30 pm
Oak Ballroom
**Organizers** – Pavan Hanumolu, Kimo Tam, Manoj Sachdev
**Moderator** – Manoj Sachdev

1:30 **Introduction**

1:35 pm 6-1 **Analog/wireline design in an increasingly digital process,** *Matt Straayar, Maxim*

Analog design in mostly digital process is a challenge. What are issues of embedding sensitive analog circuits surrounded by noisy digital transistors in 20 nm? **N/A**

2:00 pm **Tools/rules driving designers vs. designers driving tools?,** *Ravi Subramanian, Berkeley*

6-2 *Design Automation* **N/A**

Design automation is the key to enhance designer productivity. Are we relying too heavily on tools in scaled geometries? Are design rules & tools are too restrictive in 20 nm?

2:25 pm 6-3 **DFM Issues for 20 nm Analog,** *Stacy Ho, Mediatek* **N/A**

The emergence of finFETs is an important evolutionary step for transistor scaling? How one can exploit its benefits for analog circuits while ensuring yield and reliability? What for the Design For Manufacturing (DFM) challenges that we should be mindful of?

2:50 pm 6-4 **Analog design in 20 nm - putting it all together,** *Madhukar Reddy, Maxilinear* **N/A**

Successful implementation of analog circuit in Systems on Chip (SoC) requires experience, expertise. How one should execute design, exploit tools while ensuring good yield and reliability in 20 nm?

## Session 7 -- Power Management

Monday, 9/23, 1:30 pm
Fir Ballroom
**Session Chair:** Christoph Sandner, Infineon
**Session Co-Chair:** Raj Amirtharajah, UC Davis

1:30 pm **Introduction**

Effective power management requires innovative techniques to minimize system cost while maximizing efficiency. This session covers a wide array of advances in power management spanning battery interfaces, high voltage converters, LED lighting, digital control, and energy harvesting.

1:35 pm 7-1 **BIF–Battery Interface Standard for Mobile Devices (Invited),** *W. Furtner, S. Schaecher, M. Littow*, L. Cimaz*, and P. Leinonen**, Infineon Technologies AG, *ST-Ericsson and **Nokia* **81**

The MIPI® Alliance Battery Interface (BIF) is the first comprehensive battery communication interface standard for mobile devices. MIPI BIF is a robust, scalable and cost-effective single-wire communication interface between the mobile terminal and smart or low cost batteries. It is suited for removable batteries as well as for embedded batteries.

2:00 pm 7-2 **A 40V 10W 93%-Efficiency Current-Accuracy-Enhanced Dimmable LED Driver with Adaptive Timing Difference Compensation for Solid-State Lighting Applications,** *D. Park and H. Lee, University of Texas at Dallas* **89**

This paper describes a floating buck dimmable LED driver for solid-state lighting applications. Adaptive timing difference compensation is proposed to enable the driver to achieve high accuracy of the average LED current, fast settling time, and high-frequency operation over a wide range of input voltages and number of LED loads. The power efficiency of the proposed LED driver is benefited from the capabilities of using synchronous rectification and having no sensing resistor in the power stage. The synchronous rectification under high input supply voltage is enabled by a proposed high-speed and low-power gate driver with pseudo-digital level shifters. Implemented in a 0.35μm 50V CMOS process, the proposed 40V LED driver can operate at 1MHz and achieve 93% peak power efficiency when driving up to 10 series-

connected LEDs. It has only 2.8% current error from the average LED current of 345mA and settles within 8.5μs under different line and load variations. The performances of the proposed driver significantly outperform all state-of-the-art counterparts.

2:25 pm 7-3 **A Stackable Switched-Capacitor DC/DC Converter IC for LED Drivers with 90% Efficiency,** *Chengrui Le, Mitchell Kline*, Daniel L. Gerber*, Seth R. Sanders*, Peter R. Kinget, Columbia University, *University of California, Berkeley* **93**

A stackable switched-capacitor DC-DC converter IC for a hybrid-SC-resonant LED driver is presented. The IC can handle a range of input voltages through chip-stacking in the voltage domain. The tested driver delivers 17.6W with 90% peak efficiency and maintains >85% efficiency over a rectified voltage range from 160VDC to 180VDC.

2:50 pm 7-4 **A 100V Gate Driver with Sub-Nanosecond-Delay Capacitive-Coupled Level Shifting and Dynamic Timing Control for ZVS-Based Synchronous Power Converters,** *Z. Liu and H. Lee, The University of Texas at Dallas* **97**

A high-voltage high-speed gate driver to enable synchronous rectifiers with zero-voltage-switching (ZVS) operation is presented in this paper. A capacitive-coupled level-shifter (CCLS) is developed to achieve negligible propagation delay and static current consumption. With only 1 off-chip capacitor, the proposed gate driver possesses strong driving capability and requires no external floating supply for the high-side driving. A dynamic timing control is also proposed not only to enable ZVS operation in the converter for minimizing the capacitive switching loss, but also to eliminate the converter short-circuit power loss. Implemented in a 0.5μm HV CMOS process, the proposed CCLS of the gate driver can shift up a 5V signal to the 100V DC rail with sub-nanosecond delay, improving the FoM by at least 29 times compared with that of state-of-the-art counterparts. The dynamic dead-time control properly enables ZVS operation in a synchronous buck converter under different input voltages (30V to 100V). The power losses of the high-voltage buck converter are thus greatly reduced under different load currents, achieving a maximum power efficiency improvement of 11.5%.

3:15 pm **BREAK**

3:30 pm 7-5 **A Compact 120-MHz 1.8V/1.2V Dual-Output DC-DC Converter With Digital Control,** *S. Arora, D.K. Su, B. A. Wooley, Stanford University* **101**

A dual-output cascaded dc-dc converter for embedded applications uses a programmable switching frequency up to 120 MHz, output stage segmentation, and cascoding to achieve high power efficiency with small output inductors. A fast digital constant-off-time controller provides the suppression of cross-regulation among multiple output voltages.

3:55 pm 7-6 **A Monolithic Digitally Controlled Ripple-Based DC-DC Converter with Digital Inductor Current Sensor,** *Man Pun Chan, Philip K.T. Mok, The Hong Kong University of Science and Technology* **105**

A ripple-based digital controller is presented which has incorporated a digital inductor current sensor that does not require extra ADCs and occupies a small chip. Both the digital sensor and controller are fully synthesizable with the total chip area of 0.048 $mm^2$ in 0.13-μm digital CMOS process.

4:20 pm **A Fully Integrated Battery-Connected Switched-Capacitor 4:1 Voltage Regulator with 70% Peak Efficiency Using Bottom-Plate Charge Recycling,** *T. Tong, X. Zhang,*

7-7 *W. Kim, D. Brooks, G.-Y. Wei, Harvard University* **109**

This work presents a switched-capacitor (SC) DC-DC voltage regulator that converts a 3.7V battery voltage down to ~0.8V in order to power the 'brain' SoC of a flapping-wing microrobotic bee. A cascade of two 2:1 SC converters offers high efficiency for a 4:1 conversion ratio. A charge recycling technique reduces the flying capacitor's bottom-plate parasitic loss by 50% and overall conversion efficiency reaches 70%. The output droop is less than 10% of the nominal output voltage for a worst-case 47mA load step.

4:45 pm 7-8 **A 110nA Synchronous Boost Regulator With Autonomous Bias Gating for Energy Harvesting,** *Khondker Z. Ahmed and Saibal Mukhopadhyay, Georgia Institute of Technology* **113**

An autonomously bias gated synchronous boost regulator consuming 110nA at 1V is demonstrated in 130nm CMOS. The IC generates regulated 1V output from 30mV input, starts up autonomously (battery-less) at 265mV, and regulates output ranging from 0.78V-3.3V. The peak efficiency is 83% with 10µA and 85% with 10mA load.

5:10 pm 7-9 **A Power Sensor with 80ns Response Time for Power Management in Microprocessors,** *S. Bhagavatula, B. Jung, Purdue University* **117**

A real-time, on-chip power sensor that estimates load currents and on-chip temperatures concurrently is presented. It occupies an area of 0.11mm X 0.09mm in 130n mCMOS technology. With a simplified 1-point calibration and a response time of 80ns, it shows improvements in input dynamic range by 10 X, response time by 6 X and sensitivity by 3 X over previous such sensors. A current reference with a measured temperature coefficient 91ppm/C (-20Cto 120C) is presented. This reference is used for online calibration of the power sensor to enable greater tolerance to PVT variations and aging effects.

## Session 8 -- AMS Verification in Advanced Technologies

Monday, 9/23, 1:30 pm
Pine Ballroom
**Session Chair:** Hidetoshi Onodera, Kyoto University
**Session Co-Chair:** Yu (Kevin) Cao, Arizona State University

1:30 pm **Introduction**

Verification of AMS circuits is increasingly challenging. This session presents novel AMS simulation and emulation techniques, and advanced reliability and performance issues with technology scaling.

1:35 pm 8-1 **Discretization and Discrimination Methods for Design, Verification, and Testing of Analog/Mixed-Signal Circuits (Invited),** *J. Kim, J. Lee, D.-G. Song, T. Kim, K.-H. Kim, S. Jung, S. Youn, Seoul National University* **121**

This paper describes how the difficult problems of designing, verifying, and testing analog circuits in presence of variability can be converted to easier ones by discretizing the search spaces or discriminating one case from another. For instance, discretizing the continuous design space of analog circuits enables the use of an efficient, predictive global circuit optimizer. Also, discretizing the initial condition space of a circuit enables one to establish its global convergence property over the entire space by exploring only a small number of samples. Lastly, discriminating the test responses of the circuit with and without a fault in consideration of the underlying statistical distribution provides a formal guide on how to

quantify the fault coverage of analog/mixed-signal circuit tests. It is noteworthy that it is variability that introduces the cross-correlations in the performance metrics, convergence behaviors, and test responses between two nearby candidates in consideration and therefore enables the use of discretization and discrimination methods listed in this paper. The proposed methods are demonstrated on the practical examples of sizing an operational amplifier, verifying the correct start-up of a coupled ring oscillator, and composing a test suite for screening faults in a digitally-controlled phase interpolator circuit.

2:25 pm 8-2 **Indirect Performance Sensing for On-Chip Analog Self-Healing via Bayesian Model Fusion,** *S. Sun, F. Wang, S. Yaldiz, X. Li, L. Pileggi, A. Natarajan*, M. Ferriss*, J. Plouchart*, B. Sadhu*, B. Parker*, A. Valdes-Garcia*, M. Sanduleanu*, J. Tierno*, D. Friedman*, Carnegie Mellon University, *IBM T.J. Watson Research Center* **129**

On-chip analog self-healing requires low-cost sensors to accurately measure performance metrics. In this paper, we propose a novel approach of indirect performance sensing based upon Bayesian model fusion to facilitate inexpensive-yet-accurate on-chip measurement. A 25GHz differential Colpitts VCO is used to validate the proposed indirect performance sensing and self-healing methodology.

2:50 pm 8-3 **Fast FPGA Emulation of Background-Calibrated SAR ADC with Internal Redundancy Dithering,** *G. Wang, Y. Chiu, University of Texas at Dallas* **133**

A custom FPGA emulation platform for the verification of a slowly adapted, background calibration technique for successive-approximation-register (SAR) analog-to-digital converter (ADC) is demonstrated in an Altera DE4 board. The internal redundancy of a sub-binary SAR is exploited for the identification of ten leading bit weights in a 14.5-bit SAR ADC using pseudorandom bit sequence (PRBS) injection with background correlation. Experimental results reveal that the FPGA emulation achieves a 3000× speedup for the same simulation executed on a general-purpose microprocessor.

3:15 pm **BREAK**

3:30 pm 8-4 **Circuit Reliability Simulation Using TMI$^2$ (Invited),** *Min-Chie Jeng, Cheng Hsiao, Ke-Wei Su, Chung-Kai Lin, Taiwan Semiconductor Manufacturing Company* **137**

This paper reviews existing circuit aging simulation approaches with focus on TMI$^2$.

4:20 pm 8-5 **Scalable Behavior Modeling for 3D Field-Programmable ESD Protection Structures,** *L. Wang, X. Wang*, Z. T. Shi**, R. Ma, C. Zhang, Z. Dong, F. Lu, H. Zhao** and A. Wang, University of California, Riverside, *Omnivision Technologies, **Marvell Semiconductor* **144**

This paper reports new accurate and scalable behavioral modeling for novel 3D field-programmable ESD protection circuits, which enables post-Si on-chip ESD protection design simulation. New field-programmable ESD protection devices were fabricated in CMOS-compatible processes. The behavior models were developed from ESD testing results and verified in SPICE circuit simulation.

4:45 pm 8-6 **Quasi-3D method: Time-efficient TCAD and Mixed-Mode Simulations on finFET Technologies,** *G. Hellings, S-H Chen, D. Linten, M. Scholz, G. Groeseneken, imec,* **148**

The Quasi-3D allows to drastically speed up TCAD and mixed-mode simulations of finFET technologies, by solving on well-chosen 2D finFET cross sections. The method accurately

reproduces important transistor metrics requiring only 1/20th of the simulation time.

5:10 pm 8-7 **Gate Stack Resistance and Limits to CMOS Logic Performance,** *R. A. Wachnik, S. Lee, L. H. Pan, N. Lu, H. Li, R. Bingert **, M. Randall, S. Springer, C. Putnam, IBM Corporation, **ST Microelectronics* **152**

Measured data from five generations of CMOS technology including polysilicon and High-K metal gate stacks shows a trend of increasing gate resistance. The data are analyzed to determine horizontal and vertical components in terms of scalable model parameters. Gate resistance affects performance of a 20nmreplacement gate technology.

## Session 9 -- Wireless Transceivers

Monday, 9/23, 1:30 pm
Cedar Ballroom
**Session Chair:** Julian Tham, Broadcom
**Session Co-Chair:** Jonathan Borremans, imec

1:30 pm **Introduction**

This session presents papers on advances in wide-band receiver designs and a calibrated software-defined radio. It also presents WLAN, GPS and ultra low-power receivers and transceivers.

1:35 pm 9-1 **IIP2 and HR Calibration for an 8-Phase Harmonic Recombination Receiver in 28nm,** *B. van Liempd, J. Borremans, S. Cha*, E. Martens, H. Suys, J. Craninckx, imec vzw, *Renesas Electronics Corporation* **156**

Fully integrated CMOS receivers achieve high linearity and low noise due to harmonic recombination, but suffer from limited IIP2 and harmonic rejection due to mismatch and inaccuracies. This paper presents an 8-phase harmonic recombination receiver with independent IIP2, HR3 and HR5 calibration techniques. Calibrated >80dBm IIP2, >70dB HR3 and >75dB HR5 are measured.

2:00 pm 9-2 **Advances in the Design of Wideband Receivers (Invited),** *D. Murphy, M. Mikhemar, A. Mirzaei, H. Darabi, Broadcom Corporation* **160**

To be practical, wideband receivers must tolerate large out-of-band blockers, which can desensitize the receiver through gain compression or reciprocal mixing with LO phase noise. This paper reviews how a new noise-cancelling receiver architecture – that utilizes 3 important circuit innovations – mitigates gain compression without compromising noise figure. While the architecture is still susceptible to reciprocal mixing, it is shown how a recently proposed reciprocal mixing cancelling technique (if incorporated into the receiver) can eliminate the need for a dramatic rise in LOGEN current.

2:50 pm 9-3 **An Asymmetric Dual-Channel Reconfigurable Receiver for GNSS in 180nm CMOS,** *Nan Qi, Baoyong Chi, Yang Xu, Zhou Chen, Jun Xie, Yang Xu, Zheng Song, Zhihua Wang, Tsinghua University* **168**

A fully integrated dual-channel reconfigurable receiver supporting all the GNSS signals is presented. The two channels share the frequency synthesizer and RF front-end circuits, but employ separate asymmetric IF strips to support simultaneous dual-constellation reception. The 2nd IF strip can be configured to a dual-conversion mode to lower the sampling rate.

3:15 pm **BREAK**

3:30 pm 9-4 **A 5-GHz 11.6-mW CMOS Receiver for IEEE 802.11a Applications,** *A. Homayoun, B. Razavi, University of California, Los Angeles* **172**

A direct-conversion receiver employs a 1-to-6 transformer as a low-noise amplifier along with passive mixers and noninvasive baseband filters. Realized in 65-nm CMOS technology, the receiver provides an average noise figure of 5.3dB and a sensitivity of -70 dBm at a data rate of 54 Mb/s. The prototype draws 11.6 mW from a 1-V supply and occupies an active area of 0.18 $mm^2$.

3:55 pm 9-5 **An Adaptive Predistorter for Wireless LAN RFSoC with embedded PA and T/R switch in 55nm CMOS,** *K. Muhammad, M.-C. Chen, K.-H. Wang, K.-P. Ma, Y.-L. Hiseh, W.-S. Hsu, Y.-Y. Fu, M.-C. Lee, S.-Y. Hsiao, C.-M. Hung, MStar Semiconductor Inc.* **176**

We present an adaptive predistortion system for a WLAN transceiver in 55nm CMOS. The forward DSP path utilizes complex gain predistortion while the APD module in the feedback path computes AMAM and AMPM coefficients by comparing ideal transmit signal with the distorted signal from the receiver. This module operates with various calibration signals generated on-chip in addition to TX data. Measurement results show improvement of EVM by 1dB with the proposed approach. Improvement of P1dB of more than 3dB was obtained using fully automatic processing. The total solution utilizes 120k gates.

4:20 pm 9-6 **A 116nW Multi-Band Wake-Up Receiver with 31-bit Correlator and Interference Rejection,** *S. Oh, N. Roberts*, D. Wentzloff*, Samsung, *University of Michigan* **180**

This paper presents a 116nW wake-up radio complete with crystal reference, interference compensation, and baseband processing, such that a selectable 31-bit code is required to toggle a wake-up signal. The baseband processor detects interferers and dynamically adjusts the receiver's sensitivity, mitigating the jamming problem to previous energy-detection wake-up radios.

4:45 pm 9-7 **A 11μW Sub-pJ/bit Reconfigurable Transceiver for mm-Sized Wireless Implants,** *A. Yakovlev, J. Jang, D. Pivonka, A. Poon, Stanford University* **184**

A wirelessly powered 11μW transceiver for mm-sized wireless implants supporting TDMA has been designed and demonstrated through 35mm of porcine heart. The communication links have configurability for operation in diverse biological environments. The forward link achieves 4-20Mbps at 0.3pJ/bit, and the reverse link achieves 0.7-2Mbps at 0.7pJ/bit.

## Session 10 – Panel Session

"Can biomedical electronic startups make money??"

Monday, 9/23, 3:30 pm
Oak Ballroom
**Session Chair:** Pedram Mohseni, Case Western Reserve University
**Moderator:** John McNeill, Worcester Polytechnic Institute

-Straight semiconductor startups are marginally viable
-Green/solar startups took the money and ran
-Will bioelectronics fare any better?

Panelists Arjang Hassibi, UT Austin & Insilixa

Patrick Chiang, Fudan University

Chris Raanes, Viewray

## Monday Poster Session

Monday, 9/23, 5:00 pm – 7:00 pm
Donner/ Siskiyou/ Cascade Ballrooms

M-1 **An All-Digital Time Difference Hold-and-Replication Circuit utilizing a Dual Pulse Ring Oscillator,** *Tetsuya Iizuka, Teruki Someya, Toru Nakura, Kunihiro Asada, University of Tokyo* **188**

This paper presents a time-domain analog signal hold-and-replication circuit which holds an input time interval of two signal transitions and replicates it any number of times.65nm CMOS implementation accepts 100ps to 1.2ns time interval while occupying40x60μm$^2$ area. A TDC resolution enhancement application is also demonstrated in this paper.

M-2 **A 15-Bit Binary-Weighted Current-Steering DAC with Ordered Element Matching,** *T. Zeng, K. Townsend, J. Duan*, D. Chen, Iowa State University, *Broadcom Corporation* **192**

This paper introduces a 15-bit binary-weighted current-steering DAC in a 130nm CMOS technology. The core area is less than 0.42mm$^2$, among which the MSB area is well within 0.021mm$^2$. Measurement results have shown that the DNL and INL can be reduced from 9.85LSB and 17.41LSB to 0.34LSB and 0.77LSB, respectively.

M-3 **A 500 MS/s 76dB SNDR Continuous Time Delta Sigma Modulator with 10MHz Signal Bandwidth in 0.18μm CMOS,** *Rune Kaald, Bjørnar Hernes*, Christian Holdø*, Frode Telstø*, Ivar Løkken*, Norwegian University of Science and Technology, *Hittite Microwave Norway* **196**

A 5th order continuous-time delta sigma modulator is designed in 0.18um CMOS. At a sampling rate of 500MHz it achieves 76dB SNDR over a 10MHz bandwidth consuming 58mW. 5th order noise shaping is realized with 4 op amp based RC integrators and a VCO realizing an integrator and a 4 bit quantizer. A THD of-82.3dBc is achieved without calibration of feedback DACs. We address two problems related to VCO quantizers which have local feedback to also work as integrators with a high-speed excess loop delay compensation using capacitive summation and a method for reducing the switching activity of the output codes.

M-4 **A 0.1-3GHz Cell-Based Fractional-N All Digital Phase-Locked Loop Using ΔΣ Noise-Shaped Phase Detector,** *Yao-Chia Liu, Wei-Zen Chen, , Mao-Hsuan Chou*, Tsung-Hsien Tsai*, Yen-Wei Lee, Min-Shueh Yuan, National Chiao Tung University and *TSMC* **200**

A 0.1-3 GHz, cell-based, fractional-N ADPLL with ΔΣ noise-shaped phase detector is presented. By dithering the reference phase and quantization phase error through an additional feedback path, linear phase detection and zero stabilization are accomplished without resort to sophisticated time to digital converter (TDC). The measured rms jitter from a 3GHz carrier is 1.9 ps with a multiplication factor of 60. Implemented in TSMC 40nm general purpose superb CMOS technology, the chip size is 280μm x 240μm. Keywords: TDC, ΔΣ phase detector, fractional-N ADPLL

M-5 **A Direct-Battery Hookup, Fully Integrated Stereo Headphone Module with 82 mW Output Power and 110 dB PSRR,** *Khaled Abdelfattah, Sherif Galal, Iuri Mehr, Alex Jianzhong Chen, Ahmet Tekin*, Xicheng Jiang, Todd L. Brooks, Broadcom Corp.,*Semtech* **204**

A complete stereo ground-referenced headphone module that supports direct battery hookup is integrated on a 40 nm mobile baseband SoC. Several techniques were employed to guarantee the reliability of the module circuitry under high output swing and limited safe operating regions in this low-voltage technology. Additional techniques to reduce area and enable low-cost integration were also employed. The module delivers 3.24 Vpp to a 16Ω load (82 mW) and achieves 100 dB dynamic range (DR), 110 dB PSRR, and 84 dB THD+N with an area of 0.675mm$^2$ on the SoC.

M-6 **A Fast-Locking Digital DLL with a High Resolution Time-to-Digital Converter,** *Dandan Zhang, Hai-gang Yang, Zhujia Chen, Wei Li, Zhihong Huang, Lijiang Gao, Wenrui Zhu, Institute of Electronics, Chinese Academy of Sciences* **208**

A fast-locking DLL is presented in this paper. By adopting a novel high resolution TDC, the total locking time is reduced to 8 clock cycles and shortened by 80% to 94.6% compared to previous closed-loop architectures .The measured RMS and p-p jitters are 2.3ps and 10ps respectively.

M-7 **A Stochastic Sampling Time-to-Digital Converter with Tunable 180-770fs Resolution, INL less than 0.6LSB, and Selectable Dynamic Range Offset,** *J. Tandon, T. Yamagichi, S. Komatsu, K. Asada, VDEC-D2T, University of Tokyo* **212**

We introduce a stochastic time-to-digital converter (TDC) that has 180-770fs tunable resolution, less than 0.6LSB INL, and selectable dynamic range offset .Previous arbiter-based TDCs have fine resolution but small dynamic range which is difficult to calibrate. Our approach uses comparators as decision elements to precisely control dynamic range offset.

M-8 **A 50 μW/Ch Artifacts-Insensitive Neural Recorder Using Frequency-Shaping Technique,** *J. Xu, Z. Yang, National University of Singapore* **216**

This paper presents a frequency-shaping (FS) neural recording interface that can inherently reject electrode offset, 5-10 times increase input impedance,4.5-bit extend system dynamic range, and provide much more tolerance to motion artifacts and 50/60 Hz power noise interferences. It is supposed to be more suitable for long-term brain-machine-interface (BMI) experiments.

M-9 **A Bipolar >40-V Driver in 45-nm SOI CMOS Technology,** *Yousr Ismail, Chang-Jin Kim, Chih-Kong Ken Yang, University of California, Los Angeles* **220**

A novel, switched-capacitor output driver combining both voltage-conversion and pulse-drive is introduced. The driver is implemented in 45-nm SOI CMOS technology and uses only

process-compliant devices. It achieves a maximum output drive of 44 V and has a 36 KΩ output resistance while consuming 28 mA from a 1.5-V supply.

M-10 **High-Sensitivity Photodetection Sensor Front-End, Detecting Organophosphourous Compounds for Food Safety,** *L. Wan, Y. Qin, P. Chiang*, G. Chen, R. Liu, Z. Hong, Fudan University and *Oregon State University* **224**

A high-sensitivity, high-dynamic range photo detection sensor front-end is presented, suitable for low-cost hand-held food safety systems. This sensor-on-a-chip for detecting organophosphorus compounds incorporates a non-chip deep N-well photo detector, pulse width modulation, and a folded reference. Measurement results show an input optical power dynamic range of 71dB, a sensitivity of 3.6nW/cm$^2$.

M-11 **A 16-Channel, 359 µW, Parallel Neural Recording System Using Walsh-Hadamard Coding,** *Vahid Majidzadeh, Alexandre Schmid and Yusuf Leblebici, Swiss Institute of Technology (EPFL)* **228**

Application of an algebraic coding to a multichannel parallel neural recording system is presented. The Walsh-Hadamard coding enables back-end hardware sharing between recording channels, using a linear and orthogonal superposition of the analog inputs. Moreover, this technique preserves the temporal information of the channels in contrast to the conventional architectures which use time-multiplexed ADC. In the proposed architecture a single ADC operates on a superposed signal, thereby the dynamic range of the ADC is effectively shared between channels benefiting from the sparsity characteristics of the channels. A 16-channel parallel recording system is implemented as a proof of concept. The system is implemented in a 0.18 µm CMOS technology and occupies 1.99 mm$^2$ of silicon area. The input-referred noise of a single channel integrated from 10 Hz to 100 kHz equals to 4.1 µV$_{rms}$, and the effective power consumption of each channel is measured at 22.4 µW from a 1.2 V power supply, which results in a system level NEF of 5.6.

M-12 **Analysis of Deviation from Pelgrom Scaling Law in $V_{th}$ Variability of Pocket-implanted MOSFET,** *K. Sakakibara, Y. Miura, T. Kumamoto, S. Tanimoto, Renesas Electronics Corporation* **232**

Deviation from Pelgrom scaling law in threshold voltage variability of pocket-implanted MOSFET is attributed to an increasing behavior of offset-voltage variability in weak and moderate inversion regions. This increasing behavior can be completely removed by using both-side ring gate structure. This means that the deviation is caused by subthreshold hump.

M-13 **Low Power ARM® Cortex™-M0 CPU and SRAM Using Deeply Depleted Channel (DDC) Transistors with VDD Scaling and Body Bias,** *V. Agrawal, N. Kepler, D. Kidd, G. Krishnan, S. Leshner, T. Bakishev, D. Zhao, P. Ranade, R. Roy, M. Wojko, L. Clark, R. Rogenmoser, M. Hori*, T. Ema*, S. Moriwaki*, T. Tsuruta*, T. Yamada*, J. Mitani*, and S. Wakayama*, SuVolta Inc. and *Fujitsu Semiconductor Ltd.* **236**

130-D Knowles Drive, Deeply Depleted Channel™ (DDC) technology demonstrates more than 50% power reduction for ARM® Cortex™-M0 CPU cores and SRAMs at matched performance via VDD scaling and body biasing. DDC technology also demonstrates 35% speed improvement at matched power, improved SNM, 150mV 8Mb SRAM VDDmin improvement, and 5x SRAM retention leakage reduction.

A new Error Correcting Code (ECC) solution to improve the reliability of NAND is proposed. Implemented in SSD controller IC, it is confirmed that more than1/10000 lower error rate, and 1.7x longer endurance of SSD can be achieved. This solution consists of a Message-Passing ECC architecture and a Parity Area Combined ECC scheme.

M-20 **45pW ESD Clamp Circuit for Ultra-Low Power Applications,** *Yen-Po Chen, Yoonmyung Lee, Jae-Yoon Sim*, Massimo Alioto**, David Blaauw, and Dennis Sylvester, University of Michigan, *Pohang University of Science and Technology, **University of Siena* **263**

Novel ultralow-leakage ESD power clamp designs are proposed and implemented in 0.18μm CMOS. Limiting both subthreshold leakage and GIDL, the proposed designs consume 43pW at 25°C and 119nW at 125°C with 4500V HBM level and 400V MM level protection, marking an 18-139× leakage reduction over conventional ESD clamps.

M-21 **A 1.14mW 750kb/s FM-UWB Transmitter with 8-FSK Subcarrier Modulation,** *F. Chen, Y. Li, D. Lin, H. Zhuo, W. Rhee, J. Kim*, D. Kim*, and Z. Wang, Tsinghua University and *Samsung Advanced Institute of Technology* **267**

A noninvasive energy-efficient FM-UWB transmitter is implemented in 65nm CMOS for stereo hearing aid. 8-FSK subcarrier modulation is employed to triple data rate by a fast-settling PLL. The FM-UWB signal is generated by an FLL-assisted ring VCO and a class AB PA. The 3.5-4GHz 750kb/s transmitter consumes 1.14mW,achieving 1.5nJ/bit.

M-22 **A 2.4 GHz Energy-Efficient 18-Mbps FSK Transmitter in 0.18 μm CMOS,** *Jingjing Chen, Weiyang Liu, Peng Feng, Haiyong Wang, and Nanjian Wu, Institute of Semiconductors, Chinese Academy of Sciences* **271**

This paper presents a 2.4 GHz energy-efficient phase locked loop (PLL)-based transmitter (TX) integrated in 0.18-μm CMOS technology. By using Twin-VCO transmission scheme, the data rate of the transmitter is free of loop bandwidth of PLL with stable carrier frequency. Measured results show that The TX achieves an energy efficiency less than 0.64 nJ/bit at a data rate of 18 Mbps.

M-23 **A 60GHz, Linear, Direct Down-Conversion Mixer with mm-Wave Tunability in 32nm CMOS SOI,** *M.A.T. Sanduleanu, A. Valdes-Garcia, Y. Liu, B. Parker, S. Shlafman*, B. Sheinman*, D. Elad*, S. Reynolds, D. Friedman, IBM T.J. Watson Research Center and *IBM Haifa R&D* **275**

The gain/linearity trade-off is exploited to achieve the best linearity performance of a mm-Wave down-conversion system. The achieved linearity (IIP3) for the whole down-conversion chain is better than 11.06dBm for 5.8dB gain at 60GHz. The down-converter occupies 1.38mm$^2$ in 32nm CMOS SOI and consumes 19.2mW from 1V supply.

M-24 **A Fully Integrated Highly Linear Receiver with Automatic IP$_2$ Calibration Schemes for Multi-Standard Applications,** *A. Borna, Y. Wang*, C. Hull*, H. Wang**, A. Niknejad, UC Berkeley, *Intel Corp., ** Georgia Institute of Technology* **279**

This paper presents an entire receiver chain with fully integrated self-calibration circuitries for suppressing the 2nd-order intermodulation distortions in Homodyne receivers for multi-standard applications. All the potential sources for IM2 generation are identified and tackled independently by architectural and calibration techniques, which results in a robust IP$_2$

enhancement.

## Session 11 -- Power and Heterogeneous Technology Circuit

Tuesday, 9/24, 9:00 am
Oak Ballroom
**Session Chair**: Takamaro Kikkawa, Hiroshima University
**Session Co-Chair**: Philippe Jansen, Texas Instruments

9:00 am **Introduction**

This session focuses on technology circuit interactions for heterogeneous 3D stacked-silicon FPGA, advanced high-voltage GaN electronics and future generation nanowire transistors.

9:05 am 11-1 **40V MESFETs Fabricated on 32nm SOI CMOS,** *W. Lepkowski, S. Wilk, J. Kam, T. Thornton, Arizona State University* **283**

40V N-channel MESFETs fabricated at a commercial 32nm SOI CMOS foundry without changing any of the process flow or including additional mask steps. Current drives of 110mA/mm with peak cut-off frequency of 30.5GHz and maximum oscillation frequency of 34.5GHz were observed.

9:30 am 11-2 **Recent Advances in GaN Power Electronics (Invited),** *Karim Boutros, Rongming Chu, Brian Hughes,HRL Laboratories, LLC* **287**

Gallium Nitride power devices are poised to replace silicon-based MOSFETs in power switching applications having weight and volume constraints, while simultaneously needing a high overall efficiency. With its projected 100x performance advantage over silicon, GaN is a game changing technology for energy-efficient power electronics. This paper reviews the advantages of GaN material and devices, the performance of these devices in power circuits, and the potential applications for this technology.

9:55 am 11-3 **Prospective for Nanowire Transistors (Invited),** *J.P. Colinge, S. Dhong, Taiwan Semiconductor Manufacturing Company* **291**

The multigate nanowire FET architecture allows for ultimate short-channel control and push Moore's law down to sub-5nm gate lengths. This paper reviews nanowire transistor device physics as well as circuit prospects in the fields of CMOS logic, memory, analog, RF and integrated sensor applications.

10:45 am **BREAK**

11:05 am 11-4 **Interconnect and Package design of a Heterogeneous Stacked-Silicon FPGA (Invited),** *E. Wu, K. Abugharbieh, B. Banijamali, S. Ramalingam, P. Wu, C. Wyland, Xilinx, Inc.* **299**

## Session 12 -- Wireline Transmitter and Receiver Design Techniques

Tuesday, 9/24, 9:00 am
Fir Ballroom
**Session Chair**: Dennis Fischette, AMD
**Session Co-Chair**: Jaeha Kim, Seoul National University

9:00am **Introduction**

This session presents state of the art wireline transmitter and receiver circuits, including advanced low-power equalization and impedance-matching techniques.

9:05 am 12-1 **A 5Gb/s 3.2mW/Gb/s 28dB Loss-compensating Pulse-Width Modulated Voltage-Mode Transmitter,** *S. Saxena, R. K. Nandwana, and P. K. Hanumolu, Oregon State University* **307**

A voltage mode transmitter employs pulse width modulation (PWM) based equalization of NRZ input data at 5Gb/s and compensates 28dB channel loss at 2.5GHz. Fabricated in a 90nm CMOS process, the proposed transmitter achieves a horizontal eye opening of 0.3UI with BER<10^{-12} and consumes only 16mW power of which 2.5mW is consumed by the digital PLL.

9:30 am 12-2 **Current-Steering Pre-Emphasis Transmitter with Continuously Tuned Line Terminations for Optimum Impedance Match and Maximum Signal Drive Range,** *Gerrit W. den Besten, Harold G. Hanson, Ranjeet K. Gupta, NXP Semiconductors* **311**

A configurable 24-segment current-steering transmitter with linear continuously-tuned active line terminations is presented. A linearized resistor-MOSFET termination topology is proposed for accurate output levels (σ=1%) and good impedance matching (σ=2%) enabling larger drive levels by better supply utilization. The concept is implemented in 0.16 μm CMOS for 1-6Gbps.

9:55 am 12-3 **Design Techniques for CMOS Backplane Transceivers Approaching 30-Gb/s Data Rates (Invited),** *J. Bulzacchelli, IBM T.J. Watson Research Center* **315**

This paper highlights design techniques for extending backplane transceiver data rates by describing a 28-Gb/s prototype implemented in 32-nm SOI CMOS and featuring a source-series terminated driver with 4-tap FFE, a two-stage peaking amplifier with active feedback, and a 15-tap DFE. Equalization is demonstrated over a 35-dB loss channel.

10:45 am **BREAK**

11:05 am 12-4 **Design Considerations for Low-Power Receiver Front-End in High-Speed Data Links (Invited),** *S. Shekhar, J. E. Jaussi, F. O'Mahony, M. Mansuri, B. Casper, Intel Corporation* **323**

This paper presents different design considerations for the receiver front-end (RXFE) in low-power, high-speed data links. Specifications for the RXFE are defined and explained in detail, including their impact on the overall link performance. Based on these specifications, low-power RXFE topologies are then analyzed to illustrate the design and performance tradeoffs. Techniques to properly characterize and measure the RXFE specifications are also provided, supplemented with measurement results from three different low-power links operating at 10Gb/s, 16Gb/s and 20Gb/s.

11:55 am 12-5 **An 8mW Frequency Detector for 10Gb/s Half-Rate CDR using Clock Phase Selection,** *M.S. Jalali, R. Shivnaraine, A. Sheikholeslami, M. Kibune*, H. Tamura*, University of Toronto, *Fujitsu Laboratories Limited* **331**

A half-rate single-loop CDR with a new frequency detection scheme is introduced. The proposed frequency detector selects between the clock phases (I and Q) to reduce cycle

slipping, hence improving lock time and capture range. This frequency detector, implemented within a 10Gb/s CDR in Fujitsu 65nm CMOS, consumes only 8mW, but improves the capture range by up to 3.6 . The measured capture range with the FD is from 8.675Gb/s to 11Gb/s.

## Session 13 -- mm-Wave Circuits and Systems

Tuesday, 9/24, 9:00 am
Pine Ballroom
**Session Chair**: John Rogers, Carleton University
**Session Co-Chair:** Howard Luong, Hong Kong University of Science & Tech.

9:00 am **Introduction**

This session will present the latest advances in mm-Wave (>30 GHz) circuits and systems, including transceivers, power amplifiers, synthesizers, VCOs and dividers.

9:05 am 13-1 **A 60 GHz Linear Wideband Power Amplifier using Cascode Neutralization in 28 nm CMOS,** *Siva V Thyagarajan, Ali M Niknejad, Christopher D Hull*, University of California Berkeley, *Intel Corporation* **335**

This paper presents the design of a 60GHz linear wideband power amplifier (PA) in deeply scaled 28nm CMOS technology. The PA utilizes cascode drain-source neutralization to improve stability and low-k transformer techniques to achieve high bandwidth. The PA delivers a saturated output power of 16.5dBm with a peak PAE of 12.6% and achieves a bandwidth of 11GHz with a peak gain of 24.4dB.

9:30 am 13-2 **Compact High-Power 60 GHz Power Amplifier in 65 nm CMOS,** *Payam M. Farahabadi, Kambiz Moez, University of Alberta* **339**

This paper presents a compact 60 GHz power amplifier utilizing a novel 4-waymulti-conductor power combiner. Fabricated in 65 nm CMOS process, the measured gain of the 0.19 $mm^2$ power amplifier is 18.8 dB at 60 GHz. A maximum saturated output power of 18.3 dBm is measured with the 15.9% peak power added efficiency.

9:55 am 13-3 **CMOS Low-Power Transceivers for 60GHz Multi Gbit/s Communications (Invited),** *V. Vidojkovic, V. Szortyka, K. Khalaf,G. Mangraviti, B. Parvais, K. Vaesen, S. Brebels, A. Spagnolo, M. Libois, J. Long*, K. Raczkowski, P. Raghavan, A. Bourdoux, L. Min, C. Soens, V. Giannini, P. Wambacq, imec, *Delft University of Technology* **343**

The availability of 9GHz bandwidth around 60GHz in combination with simple modulations schemes, low-cost radio ICs and small antenna size allows for multi Gbit/s wireless communications. In this article the potential of 60GHz wireless communications is evaluated from system, application and user point of view. Further, design challenges for 60GHz CMOS transceivers are identified. State-of-the-art designs show that short-range high-data rate radio links based on CMOS ICs can be made, potentially helped with beamforming.

10:45 am **BREAK**

11:05 am 13-4 **A CMOS 21-48GHz Fractional-N Synthesizer Employing Ultra-Wideband Injection-Locked Frequency Multipliers,** *A. Li, S. Zheng, J. Yin, X. Luo*, H. Luong, The Hong Kong University of Science and Technology, *Huawei Technologies Co. Ltd.* **351**

Higher-order LC tanks are proposed to widen the locking range of mm-Wave injection-locked frequency multipliers. Employing a chain of such multipliers, a wideband fractional-N frequency synthesizer is demonstrated in 65nm CMOS. An output tuning range from 20.6-48.2GHz (80.2%) is measured with phase noise<-107dBc/Hz at 1MHz offset while consuming 148mW.

11:30 am 13-5 **A 75.7GHz to 102GHz Rotary-traveling-wave VCO by Tunable Composite Right /Left Hand T-line,** *Shunli Ma, Wei Fei*, Hao Yu*, Junyan Ren, Fudan University, *Nanyang Technological University* **355**

With the use of tunable composite-right/left-hand transmission line, this paper provides a wide frequency-tuning-range mechanism for Mobius-ring rotary-traveling-wave VCO in millimeter-wave region. Measurement results show 29.5% tuning range with center frequency at 89.3GHz, and phase noise from-100.08dBc/Hz to -98.7dBc/Hz with 10MHz offset, demonstrating state-of-art FOMT of -177.78dBc/Hz.

11:55 am 13-6 **Transformer-Based Dual-Band VCO and ILFD for Wide-Band mm-Wave LO Generation,** *Yue Chao, Howard C. Luong, Hong Kong University of Science and Technology* **359**

This paper presents wide-band transformer-based mm-wave dual-band VCO and ILFD. Based on two novel design techniques, the circuit is designed and fabricated in TSMC 65nm CMOS process and measures a state-of-art performance.

## Educational Session 1

Tuesday, 9/24, 9:00 am
Cedar Ballroom
**Session Chair**: Foster Dai, Auburn University
**Session Co-Chair:** Earl McCune, RF Communications Consulting

E-1 9:00 am – 10:30 am **Concurrent Design of ESD Protection and Integrated Circuits for Optimization and Prediction,** *Albert Wang, University of California, Riverside* **363**

As semiconductor technologies continuously advance into nano nodes, while integrated circuits (IC) become faster and more complex, on-chip ESD protection design quickly emerges as a huge IC design barrier nowadays. Major ESD design challenges include the followings: First, how to conduct simulation-based quantitative design to achieve ESD protection design optimization and prediction? Second, how to minimize ESD-induced parasitic effects that affect IC performance. Third, how to perform co-design of ESD protection and IC to achieve ESD protection and core circuit design optimization simultaneously. This lecture discusses critical aspects and techniques in practical ESD protection designs, including a mixed-mode ESD simulation-design method for design prediction, accurate RF ESD design characterization, complex ESD-IC interactions, ESD+IC co-design for whole-chip design optimization, etc. Real-world design examples will be presented.

10:30 am **BREAK**

## Educational Session 2

Tuesday, 9/24, 11:00 am
Cedar Ballroom

**Session Chair**: Eric Naviasky, Cadence
**Session Co-Chair:** Gerrit den Besten, NXP Semiconductors

E-2
11:00 am – 12:30 pm

**Characterization of Matching, Variability, and Low-Frequency Noise for Mixed-Signal Technologies,** *Hans Tuinhout, NXP* **397**

Parametric mismatches and low frequency noise are major performance limiters as well as notorious causes for redesigns of high performance mixed-signal (HPMS) circuits and systems. Consequently, it is extremely important to measure, analyze, interpret, model and document these effects for mixed-signal technologies.

Part one of this educational lecture discusses parametric mismatch benchmarks and variability characterization challenges for active and passive devices. Part two focuses on low frequency noise, in particular on the emerging challenge in this field, namely variability of 1/f noise and associated Random Telegraph Noise.

These topics will be exemplified with results from (Bi)CMOS technologies, ranging from the current HPMS cash cow technologies (140 to 250 nm minimum dimensions), up to more advanced 40 nm node devices which can be seen as the stepping stone to some of the ultimate challenges of sub 10 nm devices that will mark the end of the CMOS shrink roadmap.

## Luncheon Keynote

Tuesday, Sept. 24, 12:20 – 1:50 pm
Sierra Ballroom
Tickets for the luncheon are for sale at the Registration Desk

**Connecting with the Emerging Nervous System of Ubiquitous Sensing,** *presented by Joseph Paradiso, MIT Media Laboratory* **N/A**

Embedded sensors are touching every phase of our lives as they diffuse into the objects and environments around us. We'll exhibit a "phase change" within a few years, however, once this sensor information becomes networked and available to applications running outside of each device's domain that will be at least as profound as the web was to computers. Accordingly, this talk will overview the broad theme of interfacing humans to the ubiquitous electronic "nervous system" that sensor networks will soon extend across things, places, and people. I'll illustrate this through two avenues of research - one looking at a new kind of digital "omniscience" (e.g., building different kinds of browsers for sensor network data) and the other looking at buildings & tools as "prosthetic" extensions of humans (e.g., making HVAC systems an extension of your sense of comfort), drawing from many projects that are running in my group at the MIT Media Lab.

## Session 14 – Panel Session

"Do You Need to Plug In to Get Your Fill of Bits?"
Tuesday, 9/24, 2:00 pm
Oak Ballroom
**Moderator:** Sam Palermo, Texas A&M University

Applications such as video streaming and data sharing/backup are driving demand for increased device-to-device data transfer bandwidth for in/adjacent-room communication on the order of 10-20m. While the demand for higher data rates is growing, consumers are also becoming accustomed to and beginning to expect broadband wireless connectivity for their devices. To replace electrical cable-based links, wireless links will need to demonstrate competitive or superior data rates, energy efficiency, reliability,

cost, and in some applications, latency. On the other hand, optical interconnects offer the flexibility of traditional electrical cable-based systems at potentially higher data rates and lower power and latency. However, the reliability and cost of optical cable systems are open issues. This panel aims to answer the question: "Do You Need to Plug In to Get Your Fill of Bits?" In other words, can future wireless systems support the 10+Gb/s data rates that future systems will demand? If not, what is best approach? Traditional electrical or emerging optical cable solutions?

Panelists: Elad Alon, University of California - Berkeley
Marc Loinaz, Broadcom
Payam Heydari, University of California - Irvine
Tirdad Sowlati, Broadcom
Drew Alduino, Intel

## Session 15 - Forum Session: Electrical and Photonics I/O Test and Debug

Tuesday, 9/24, 2:00 pm
Fir Ballroom
**Session Chair:** Mike Li, Altera
**Session Co-Chair:** Takahiro Yamaguchi, Advantest Laboratories

2:00 pm **Introduction**

This session addresses test and debug challenges associated with multi-Gbits/s to more than 30 Gbits/s I/Os built with electrical and photonic ICs.

2:05 pm 15-1 **The Future of High Speed Electrical and Photonics IO Testing: Facing Complex Challenges,** *Salem Abdennadher, Intel Corporation* **N/A**

Where is High Speed IO manufacturing Test heading? As technology continues to scale to increase system bandwidth, decrease power dissipation, die area and system cost, the challenges associated with test seem to expand exponentially. There has been a rise in defect occurrences as Serial Electrical IO interfaces instances and test complexity rise. In addition, introduction of optical IO's in main stream products is introducing unprecedented challenges. Technology process variation and process uncertainty is also affecting the performance of these circuits.

Intel Test community wonder if the current technologies and strategies are adequate in the short term and what they should focus on now to deal with issues that are surfacing in the 2013-2015 timeframe. Current 22nm analog test coverage issues will persist to be an issue with 14nm process and beyond or even get worse. With Signal Headroom becoming too small to design analog circuit with sufficient signal integrity, HVM tests need to screen not only for manufacturing defects but also for design marginality and process uncertainty.

In this talk will present new HVM test techniques to meet the ever increasing test complexity challenges. Such as developing methodologies to test optical interfaces depending on their level of integration (Hybrid or Full). Providing new innovative approaches in areas such as: Complete No Touch Testing (NTT) methodology and systematic defect capture in Electrical High Speed IO circuits.

2:40 pm 15-2 **Testability Improvement for 12.8 GB/s Wide IO DRAM Controller by Small Area Pre-bonding TSV Tests and a 1 GHz Sampled Fully Digital Noise Monitor,** *T. Nomura, R. Mori, M. Ito*, K. Takayanagi, T. Ochiai, K. Fukuoka, K. Otsuga, K. Nii, S. Morita, T.*

*Hashimoto, T. Kida, J. Yamada, H. Tanaka, Renesas Electronics Corporation, *Renesas Micro Systems Corporation* **453**

A Wide IO DRAM controller chip was designed, and fabricated with Through Silicon Via (TSV) technology. The memory interface consists of 1200 TSVs including 512 bit data signals, which introduces new challenges in testability. To address these challenges, testing schemes by dedicated circuitry are proposed. TSV test circuitry is implemented in the micro-IOs placed in between the fine pitch TSV arrays, which can detect and reject TSV defects prior to stacking process. Another circuitry is for monitoring power noise, where we are aware of 512 bit Data simultaneously switching noise. We also introduced a impedance optimization scheme associated with the noise monitoring circuitry, where Vmin was improved for 30mV by appropriate optimization. We achieved 12.8GB/s operation, while IO power was reduced by 89% compared to LPDDR3.

3:15 pm 15-3 **Design Verification and Testing of High Speed Silicon Photonics Links,** *Brian Welch, Luxtera, T. Nomura, R. Mori, M. Ito*, K. Takayanagi, T. Ochiai, K. Fukuoka, K. Otsuga, K. Nii, S. Morita, T. Hashimoto, T. Kida, J. Yamada, H. Tanaka, Renesas Electronics Corporation, *Renesas Micro Systems Corporation* **N/A**

This paper looks at the verification and test techniques that can be deployed in silicon photonics solutions, and how it mirrors those that are used in conventional CMOS design.

3:50 pm **BREAK**

4:05 pm 15-4 **CMOS Photonics: Product Test and Debug Challenges,** *David Piede, Cisco Systems* **N/A**

CMOS photonics is a new and exciting technology that offers potential improvements in cost, power, integration, and size over current photonic and electronic technologies. As with any new technology, there are new challenges associated with productization. We will focus on the test and debug challenges associated with known-good-die (KGD), and with the heterous integration of electronics and CMOS photonics in a package format.

4:40 pm **Panel Discussion and Q&A**

## Session 16 -- Nyquist Rate A/D Converters

Tuesday, 9/24, 2:00 pm
Pine Ballroom
**Session Chair**: Mohammad Ranjbar, Cirrus Logic
**Session Co-Chair**: John McNeill, Worcester Polytechnic Insittute

2:00 pm **Introduction**

A/D converters are key building blocks in many electronic systems. Their applications range from low-speed, low-power sensors to high-speed wireless or wireline communication systems. Papers in this session cover a range of speeds form 250 kSps to 12.8 GSps, and resolutions from 5 to 12 bits.

2:05 pm 16-1 **A 12.8GS/s Time-Interleaved SAR ADC with 25GHz 3dB ERBW and 4.6b ENOB,** *Y. Duan, E. Alon, UC Berkeley* **457**

This paper presents a 12.8GS/s 32-way hierarchically time-interleaved SAR ADC with 4.6-bit

ENOB in 65nm CMOS. The prototype utilizes multi-stage sampling and a cascode sampler circuit to enable greater than 25GHz 3dB effective resolution bandwidth (ERBW). We further employ a pseudo-differential SAR ADC to save power and area. The core circuit occupies only 0.23mm$^2$and consumes a total of 162mW from dual 1.2V/1.1V supplies.

2:30 pm 16-2 **A 10GS/s 6b Time-Interleaved ADC with Partially Active Flash sub-ADCs,** *Xiaochen Yang, Robert Payne*, Jin Liu, University of Texas at Dallas, *Texas Instruments* **461**

A 10GS/s 6b time-interleaved ADC in 65nm CMOS is presented. A partially-active flash sub-ADC is proposed to improve the power efficiency, a source-follower based boot-strap T&H circuit reduces input kickback and improve ADC bandwidth, and timing skew is corrected with duty-cycle calibration. The measurement shows a FOM of 197fJ/conv-step.

2:55 pm 16-3 **An 8-Bit 4-GS/s 120-mW CMOS ADC,** *Hegong Wei, Peng Zhang*, Bibhu Datta Sahoo**, and Behzad Razavi, University of California-Los Angeles, *Tsinghua University, **Amrita University* **465**

A four-channel time-interleaved pipelined ADC employs a new timing calibration technique to suppress mismatch-induced spurs and achieve a Nyquist-rate SNDR of 44.4 dB. Designed in 65-nm CMOS technology, the ADC draws 120 mW, providing an FOM of 219 fJ per conversion step.

3:20 pm 16-4 **A 7.1-mW 1-GS/s ADC with 48-dB SNDR at Nyquist Rate,** *S. Hashemi, B. Razavi, University of California, Los Angeles* **469**

A two-stage pipelined ADC employs a double-sampling residue amplifier, two interleaved precharged DACs, and a new calibration scheme to correct for residue gain error, offset, and nonlinearity. Realized in 65-nm CMOS technology and sampling at 1 GHz, the prototype exhibits an FOM of 25 fJ/conversion-step while drawing 7.1 mW from a 1-V supply.

3:45 pm **BREAK**

4:00 pm 16-5 **A 0.55 V 7-bit 160 MS/s Interpolated Pipeline ADC Using Dynamic Amplifiers,** *J. Lin, D. Paik, S. Lee, M. Miyahara, A. Matsuzawa, Tokyo Institute of Technology* **473**

This paper presents a 0.55 V, 7-bit, 160 MS/s pipeline ADC using dynamic amplifiers. In this ADC, dynamic amplifiers with a common-mode detection technique are used as residual amplifiers to increase its robustness against supply voltage lowering and to remove the unnecessary static power consumption achieving clock-scalability in power performance.

4:25 pm 16-6 **A 95-MS/s 11-bit 1.36-mW Asynchronous SAR ADC with Embedded Passive Gain in 65nm CMOS,** *Jae-Won Nam, David Chiong, Mike Shuo-Wei Chen, University of Southern California* **477**

An asynchronous SAR ADC with embedded passive gain is fabricated in 65nm CMOS. The prototype ADC demonstrates a peak SNDR of 63.1dB and SFDR of 75.2dB at 95MS/s. It dissipates 1.36mW at 1.1V supply and achieves the lowest FoM among the recently published ADCs with similar specification (>10 ENOB, >10MS/s).

4:50 pm 16-7 **A 24μW 12b 1MS/s 68.3dB SNDR SAR ADC with Two-Step Decision DAC Switching,** *Yung-Hui Chung, Meng-Hsuan Wu, Hung-Sung Li, MediaTek, Inc.* **481**

A 12-bit SAR ADC employs a new DAC switching technique for improving the ADC linearity and tolerating the DAC settling errors. At 1MS/s, it consumes 24uW from a 0.9V supply. At the Nyquist-rate input, measured SNDR and SFDR are 68.3dB and 82dB, respectively. It achieves a FoM of 11.7fJ/conversion-step.

5:15 pm 16-8 **A 3.3fJ/conversion-step 250kS/s 10b SAR ADC Using Optimized Vote Allocation,** *M. Ahmadi, W. Namgoong, University of Texas at Dallas* **485**

A 10b SAR ADC that supports a flexible differential input swing from 0.4V to 1V is presented. The proposed ADC employs a non-binary architecture along with a majority vote comparison using optimized vote allocation. The prototype achieves ENOB ranging from 7.1b to 9.1b and FOM from 3.3 to 6.8fJ/conversion step.

## Educational Session 3

Tuesday, 9/24, 2:00 pm
Cedar Ballroom
**Session Chair**: Christoph Sandner, Infineon Technologies Austria AG
**Session Co-Chair:** Hoi Lee, University of Texas at Dallas

E-3 2:00 pm – 3:30 pm **Single-Inductor-Multiple-Output DC-DC Converter Design,** *Philip Mok, Hong Kong University of Science and Technology* **489**

Multiple well-regulated power supplies are essential for reducing power consumption and isolating the coupling noise between different functional blocks in VLSI design. With the increasing number of functional blocks in SoC applications, the need for a cost and efficiency effective solution of multiple power supplies is growing. Single-Inductor-Multiple-Output (SIMO) switching regulator, which provides several output voltages with only one inductor, is one of promising solutions and becomes a hot topic in DC-DC converter design due to the cost and volume reduction. However, with one inductor shared by all the outputs to accumulate and transfer energy from the input, cross regulation easily appears at outputs when a change in the inductive energy is induced by a load transient at one output. These unwanted voltage variations affect the performance or even the function of the loading devices. This talk will discuss the operation principle of SIMO switching converters and their design issues. To minimize cross regulation of a SIMO regulator, several control techniques will be presented and their pros and cons will be discussed.

3:30 pm **BREAK**

## Educational Session 4

Tuesday, 9/24, 4:00 pm
Cedar Ballroom
**Session Chair**: Foster Dai, Auburn University
**Session Co-Chair:** Jonathan Borremans, IMEC

E-4 4:00 pm – 5:30 pm **Advanced Digital Phase-Locked Loops,** *Salvatore Levantino, Politecnico di Milano* **524**

This tutorial will introduce the fundamentals of digital phased-locked loops for wireless applications. After reviewing the basic architectures, the tutorial will analyze the mechanisms of generation of limit cycles, which manifest themselves as spurious tones in the output spectrum even when synthesizing integer-N channels. Then, loop-parameter settings and

design strategies for spur elimination and phase-noise optimization will be derived. Next, we will move to the fractional-N case, in which quantization and nonlinearity add new sources of spur tones, and we will review the different design techniques which helps mitigate such impairments. Finally, examples of state-of-the-art implementations of frequency synthesizers and direct-FM modulators based on digital PLLs will be discussed.

## Tuesday Poster Session

Tuesday, 9/24, 5:00 pm – 7:00 pm

T-1 **All-Digital 90º Phase-Shift DLL with a Dithering Jitter Suppression Scheme,** *D. H. Jung, K. Ryu, J. H. Park, W. Lee*, S. O. Jung, Yonsei University, *Samsung Electronics* **572**

We propose a 90º phase-shift digital delay-locked loop (DLL) with a new dithering jitter suppression scheme. Delay-line control code dithering is effectively suppressed by comparing the distribution of the input and the output clock jitter. And the phase shift and duty cycle correction accuracy are enhanced by MDLL based phase-shift structure.

T-2 **A 1Gb/s Reconfigurable Pulse Compression Radar Signal Processor in 90nm CMOS,** *Jun Li, Hirohito Mukai*, Mehmet Parlak, Michiaki Matsuo*, James F. Buckwalter, University of California San Diego and *Panasonic Corporation* **576**

This paper presents a reconfigurable analog signal processing circuit for pulse compression radar. Adapting bandwidth for the range of the target is proposed for radar systems. The baseband signal processor includes a high-speed correlator/integrator, a 4-bit flash analog-to-digital converter (ADC) and a multi-range delay lock loop (DLL). The DLL generates multi-phase clock to align the template signal with the received signal. The circuit is fabricated in90-nm CMOS and can be configured to work from 50Mb/s to 1Gb/s with Barker codes. An SNR of 8.5dB is demonstrated for 1Gb/s. The total power consumption is 33mW at 1Gb/s.

T-3 **A 5GS/s 4-bit Time-Based Single-Channel CMOS ADC for Radio Astronomy,** *A. Macpherson, J. Haslett, L. Belostotski, University of Calgary* **580**

A 4-bit 5GS/s 65nm time-based analog-to-digital converter (ADC) targeting the next-generation Square Kilometre Array (SKA) is presented. This ADC is composed of an analog voltage-to-time converter (VTC) front end and a digital time-to-digital converter (TDC) back end. The two components can be physically separated to minimize the impact of digital noise from the ADC on high-gain, high-sensitivity receiver chains common in radio telescopes.

T-4 **A 6b 800MS/s 3.62mW Nyquist AC-coupled VCO-Based ADC in 65nm CMOS,** *P. K. Sharma, M. S-W. Chen, University of Southern California* **584**

A 6-bit 800MS/s Nyquist VCO-Based ADC is proposed. The ADC utilizes an analog differentiator, replacing the conventional digital differentiator to avoid quantization noise shaping and achieve Nyquist operation with embedded DC rejection, first order anti-aliasing filtering and improved VCO linearity without calibration. The ADC achieves peak SNDR of 34dB with over 400MHz input bandwidth and occupies an active area of 0.015mm2 while consuming 3.65mW.

T-5 **A Fully-Digital Beat-Frequency Based ADC Achieving 39dB SNDR for a 1.6mV$_{pp}$**

We present the first published measurements of a complex digital integrated circuit fabricated in both standard and split-foundry processes. Our1.3-million-transistor asynchronous FPGA operates at over 300MHz in 130nm. We discuss the challenges inherent in split design and our automated layout tools that address them.

T-12 **A 40-nm 8T SRAM with Selective Source Line Control of Read Bitlines and Address Preset Structure,** *S. Yoshimoto, S. Miyano*, M. Takamiya**, H. Shinohara*, H. Kawaguchi*, and M. Yoshimoto, Kobe University, *Semiconductor Technology Academic Research Center, and **University of Tokyo* **612**

This paper presents a 40-nm 8T SRAM in which bit lines are partially discharged by a selective source line control (SSLC) for low-power operation. The proposed SSLC scheme reduces a read bit line voltage swing in an unselected column with af loating source line (SL) of dedicated read ports.

T-13 **AOT-Controlled Dual-Mode AVP Buck Reglator with AEAF Mechanism,** *Hsin-Lun Li, Chia-Cheng Pao, Bo-Ming Chen, Chien-Hung Tsai, National Cheng Kung University* **616**

A novel adaptive voltage positioning (AVP) buck regulator using adaptive on-time (AOT) control targeted for applications with low-ESR output capacitors is proposed. In this work, AOT control is adapted to keep the system's switching frequency quasi-fixed or independent of the input supply voltage and the AVP mechanism is realized without the need to use conventional error amplifier compensator or extra current-sensing circuit. For ensuring the system's switching frequency not entering the range of acoustic frequency at light load, an AEAF (avoid entering acoustic frequency) circuit is also proposed. For comparison purpose, the implemented buck regulator can be set to operate under AVP or non-AVP mode. This work has been fabricated and verified with a standard 0.18μm CMOS technology. Experimental results show excellent transient recovery time of 4μs (under AVP mode), ±0.11% switching frequency variation (for the specified input voltage range), and 91% peak conversion efficiency.

T-14 **Switched-Capacitor Filter based Type-III Compensation for switched-mode Buck Converters,** *G. Bawa, A.Q. Huang, North Carolina State University* **620**

A switched-capacitor filter based Type-III compensation for regulation of Buck converters is presented. Compared to the all-analog filter, the proposed compensator can be fully-integrated onto the die, resulting in reduced footprint and cost. The filter time-constants also scale linearly with the converter's switching time-period, resulting in increased programmability and ease-of-use.

T-15 **Estimation of Passive Mixer Output Bandwidth Using Switched-Capacitor Techniques,** *Essam S. Atalla, Frank Zhang*, Abdellatif Bellaouar*, Poras T, Balsara, The University of Texas at Dallas and *NVIDIA Corp.* **624**

Passive mixers have become an essential component of SAW-less receivers. It is well known that the passive mixer behaves as a switched-capacitor circuit (SC)but to the authors knowledge, there is no reported analysis of the mixer impedance that truly accounts for the SC behavior. In this paper, we present for the first time a closed form of the passive mixer output impedance based on SC techniques. We prove that the fundamental lower limit of the mixer impedance is proportional to the well-known switched capacitor resistor$1/\left(f_{LO}C\right)$ and different from the previously reported mixer switch ON resistance. We also explain that the equation is useful in estimating output bandwidth of

passive mixer based front-ends with general LNA load impedance. We finally show that our bandwidth estimation matches measured results of two receiver front-ends.

T-16 **How to Reduce Power in 3D IC Designs: A Case Study with OpenSPARC T2 Core,** *Moongon Jung, Taigon Song, Yang Wan, Young-Joon Lee, Debabrata Mohapatra*, Hong Wang*, Greg Taylor*, Devang Jariwala*, Vijay Pitchumani*, Patrick Morrow*, Clair Webb*, Paul Fischer*, and Sung Kyu Lim, Georgia Institute of Technology, *Intel Corporation* **628**

The power benefit of 3D ICs is demonstrated with an OpenSPARC T2 core. Four design techniques are explored to optimize power in 3D ICs: 3D floor planning, intra-block metal layer usage control, dual-Vth, and FUB folding. With aforementioned methods, the total power saving of 21.2% is achieved against the2D counterpart.

T-17 **A General-purpose Vision Processor with 160x80 Pixel-Parallel SIMD Processor Array,** *A. Lopich, P. Dudek, University of Manchester* **632**

In this paper we present a vision processor, which incorporates a 160×80 SIMD array of pixel-processors. The processor operates with a 100MHz clock and 1.8Vsupply. The device provides 640 GOPS (binary) and 23 GOPS (greyscale) consuming0.5 W. The chip occupies 50mm^2 and is fabricated in a standard 0.18 μm CMOS process. The I/O interface supports 200 M Pixels/s (greyscale), 1.6 G Pixels/s(binary) and 40 M Pixels/s (address-event readout) data rate, and PE-parallel image sensing mode for embedded high-speed vision applications. Experimental results indicate that the performance of the presented chip approaches the efficiency of recently reported application-specific vision processors, while providing full programmability and thus being adjustable to a wide range of applications.

T-18 **A Programmable Analog Frequency-Locked Loop for VCO Characterization and Test with 8 ppm Resolution,** *S. Aouini, J.F. Bousquet, N. Ben-Hamida, L. Jakober, J. Wolczanski, C. Kurowski, Ciena Corporation* **636**

We present a digitally controlled analog frequency-locked loop for VCO characterization and test. The scheme allows a frequency tuning better than 8ppm. The AFLL comprises a 17-bit frequency counter, a sigma-delta modulator used for dithering the correction signal, a charge-pump and capacitance used as integrator and a VCO.

T-19 **Detection of Early-Life Failures in High-K Metal-Gate Transistors and Ultra Low-K Inter-Metal Dielectrics,** *Y.M. Kim, J. Seomun*, H.-O. Kim*, K.-T. Do*, J.Y. Choi*, K.S. Kim*, M. Sauer**, B. Becker**, S. Mitra, Stanford University, *Samsung Electronics, **University of Freiburg* **640**

We derive signatures for early-life failures (ELF) in 28nm high-K/metal-gate transistors and ultra low-K inter-metal dielectrics. We also demonstrate that the derived ELF signatures can be successfully detected using a clock control technique, activated during periodic on-line self-test and diagnostics in robust systems, without requiring expensive concurrent error detection.

T-20 **A Fully Differential Ultra-Compact Broadband Transformer Based Quadrature Generation Scheme,** *Jong Seok Park, Shouhei Kousai*, and Hua Wang, Georgia Institute of Technology, *Toshiba Corporation* **644**

This paper presents a fully differential ultra-compact broadband transformer-based quadrature generation scheme implemented within only one inductor-footprint. A 5GHz

design in a 65nm CMOS only occupies 260µm-by-260µmarea and achieves 0.82dB insertion loss (5GHz) with 3.8° maximum phase error and ±0.5dB amplitude mismatch within 13% bandwidth (4.75GHz to 5.41GHz).

T-21 **A -173 dBc/Hz @ 1 MHz offset Colpitts Oscillator using AlN Contour-Mode MEMS Resonator,** *Jabeom Koo, Augusto Tazzoli*, Jeronimo Segovai-Fernandez*, Gianluca Piazza*, Brian Otis, University of Washington, *Carnegie Mellon University* **648**

A differential Colpitts oscillator using AlN MEMS CMR designed in 0.13 µm CMOS is presented in this work. The oscillator operates at 1.16 GHz, with a total power consumption of 4.2 mW at 1 V supply. It achieves a phase noise of -143.6dBc/Hz, -173.3 dBc/Hz at 100 kHz and 1 MHz offset frequency respectively with a figure of merit (FOM) of 228.3 dB. Current-based temperature compensation was employed to reduce oscillator drift across temperature.

T-22 **An Ultra-Broadband Compact Mm-Wave Butler Matrix in CMOS for Array-Based MIMO Systems,** *J. Park, T. Chi, H. Wang, Georgia Institute of Technology* **652**

This paper presents an ultra-broadband compact mm-wave Butler Matrix utilizing new transformer-based swapped-port couplers. It is implemented as a 4×4 Butler Matrix at 63GHz in a 65nm CMOS process with 0.335×0.215mm2, and it achieves9.8GHz bandwidth, 2.77dB insertion loss, and better-than 17dB array peak-to-null-ratio over 57GHz and 67GHz.

T-23 **A 1.2 pJ/b 6.4 Gb/s 8+1-Lane Forwarded-Clock Receiver with PVT-Variation-Tolerant All-Digital Clock and Data Recovery in 28nm CMOS,** *Shuai Chen, Hao Li*, Liqiong Yang, Zongren Yang, Weiwu Hu and Patrick Yin Chiang*, Chinese Academy of Science, *Oregon State University* **656**

This paper presents an energy/area-efficient forwarded-clock receiver fabricated in 28 nm CMOS process. The receiver consists of 8 data lanes plus one forwarded clock lane, and adopts a novel all-digital clock and data recovery (CDR) based on delay-locked loop (DLL). The proposed all-digital DLL-based CDR uses the calibration and the update techniques to achieves a robust PVT-variation tolerance as well as a low power/area consumption. The measurement results show that our receiver can work at a data rate of 6.4 Gb/s with BER<10e-12 and consume only 7.5 mW per lane under 0.85 V power supply. The receiver core merely occupies an area of 0.02 mm*mm per lane.

T-24 **A True 4-Cycle Lock Reference-Less All-Digital Burst-Mode CDR Utilizing Coarse-Fine Phase Generator with Embedded TDC,** *Tetsuya Iizuka, Satoshi Miura*, Yohei Ishizone*, Yoshimichi Murakami*, Kunihiro Asada, University of Tokyo, *THine Electronics, Inc.* **660**

This paper presents a reference-less all-digital burst-mode CDR using a coarse-fine phase generator with embedded TDC. It achieves true 4-cycle lock without warm-ups, and eliminates dynamic power consumption in a stand-by state. Fabricated in 65nm CMOS, this CDR operates from 1.40 to 2.06Gb/s and consumes9.6mW at 2.06Gb/s with 80x80µm$^2$.

## Session 17 -- Variation and Analog Modeling

Wednesday, 9/25, 9:00 am
Oak Ballroom
**Session Chair:** Trent McConaghy, Solido Design
**Session Co-Chair:** Brian Chen, Agilent

9:00 am **Introduction**

This session discusses modeling process variation in analog and SRAM circuits, as well as analog thermal noise and distortion modeling.

9:05 am 17-1 **Thermal Noise Modeling of Nano-scale MOSFETs for Mixed-signal and RF Applications (Invited),** *Chih-Hung Chen, David Chen, Ryan Lee, Peiming Lei, and Daniel Wan, United Microelectronics Corporation* **664**

This paper presents the thermal noise in nano-scale MOSFETs – from measurement, characterization, modeling, and potential technology enhancement for future low power, mixed-signal, and radio-frequency (RF) applications. Experimental data from five CMOS technology nodes, namely 180 nm, 130 nm, 90nm, 65 nm, and 40 nm nodes are presented and discussed.

9:55 am 17-2 **A Model-Agnostic Technique for Simulating Per-Element Distortion Contributions,** *Nagendra Krishnapura, Rakshitdatta K. S., Indian Institute of Technology* **672**

The nonlinearity of an element can be altered while maintaining the operating point and first-order terms by appropriately combining two instances of the nonlinear element with complementary scaling factors for incremental voltages above the operating points. Per-element distortion contributions in a circuit can then be determined by altering the nonlinear terms by known factors and simulating the output distortion in each case. This technique can be used in a standard circuit simulator with the appropriate nonlinear device models butr equires no knowledge of the device model details on the part of the circuit designer. The technique is demonstrated by applying it to a common source amplifier with a nonlinear load and a two stage fully differential opamp.

10:20 am 17-3 **Corner Models: Inaccurate at Best and it Only Gets Worst ...,** *Colin C. McAndrew, Ik-Sung Lim, Brandt Braswell, and Doug Garrity, Freescale Semiconductor* **676**

Corner (best- and worst-case) models have been a mainstay of integrated circuit design for decades. Obviously they can be effective, especially for digital CMOS design. However, there are significant inaccuracies that arise when digital CMOS corner models are used for analog circuits, or any types of circuits or measures of circuit performance they were not targeted for. This paper details what corner models can and cannot do, and shows their inadequacies for analog CMOS circuits.

10:45 am **BREAK**

11:05 am 17-4 **Energy Centric Model of SRAM Write Operation for Improved Energy and Error Rates,** *Swaroop Ghosh, University of South Florida* **680**

We propose an energy centric model of SRAM write operation. The model provides useful insight about energy and write error rate. We employ the proposed model for evaluating write assist mechanisms and their potential in reducing intrinsic memory error rates. We also employ it for optimizing energy of memories.

11:30 am 17-5 **SRAM Read Current Variability and its Dependence on Transistor Statistics,** *Sriramkumar Venugopalan, Vivek Joshi*, Luis Zamudio*, Matthias Goldbach*, Gert Burbach*, Ralf VanBentum*, Sriram Balasubramanian*, University of California, Berkeley, *GLOBALFOUNDRIES* **684**

Our study breaks down the dependence of SRAM read current (Iread) variability(σIread) into constituting pass-gate (PG) and pull down (PD) NMOS transistor variability. We report a bottoms-up model for σIread including feedback in stacked transistors and discuss its implications on SRAM performance.

11:55 am 17-6 **Mismatch Characterization of Small Metal Fringe Capacitors,** *V. Tripathi, B. Murmann, Stanford University* **688**

This paper describes a test structure and measurements results pertaining to the characterization of single-layer, lateral-field, 0.45-fF and 1.2-fF unit metal capacitors in a 32-nm SOI CMOS process. The measurement-inferred average standard deviations for these capacitances are 1.2% and 0.8%, respectively, confirming variance scaling according to Pelgrom's matching law.

## Session 18 -- Energy Efficient SoC Design

Wednesday, 9/25, 9:00 am
Fir Ballroom
**Session Chair:** Visvesh Sathe, Advanced Micro Devices
**Session Co-Chair:** Arif Rahman, Altera Corporation

9:00 am **Introduction**

Processors, accelerators and on-chip clocking implementations for energy-efficient SoC design.

9:05 am 18-1 **A 1GHz Hardware Loop-Accelerator with Razor-based Dynamic Adaptation for Energy-Efficient Operation,** *S. Das, G. Dasika, K. Shivashankar and D. Bull, ARM Ltd.* **692**

We describe the implementation and silicon measurement results from a Razor-based hardware loop-accelerator (RZLA), implementing the Sobeledge-detection algorithm. We demonstrate robust operation with a large Dynamic Voltage Scaling (DVS) range achieved using 50% of the clock-period for timing-speculation. At 1GHz operating frequency, Razor DVS enables34% energy saving on a per-device basis and 33% overall on the entire batch of devices.

9:30 am 18-2 **Energy Efficient Recognition and Mining Processor using Scalable Effort Design,** *Vinay Chippa, Hrishikesh Jayakumar, Debabrata Mohapatra, Kaushik Roy, Anand Raghunathan, Purdue University,* **696**

A Recognition and Mining(RM) processor, that exploits the inherent application resilience using scalable effort design is implemented in TSMC-65nm technology. Measurements demonstrate energy savings of 1.2-2.3X with no quality-loss, and2X-20X with modest quality reduction due to cross-layer optimization of algorithm, architecture and circuit level scaling mechanisms.

9:55 am 18-3 **An Energy-Efficient Coarse-Grained Dynamically Reconfigurable Fabric for Multiple-Standard Video Decoding Applications,** *L. Liu, C. Deng, D. Wang, M. Zhu, S. Yin, P. Cao*, S. Wei,Tsinghua University,*Southeast University* **700**

We introduce a coarse-grained dynamically reconfigurable fabric consisting of16x16 Processing Elements. Line-Switched Mesh Connect routing and Hierarchical Configuration Context organization scheme are proposed. Measured results show that the fabric has great

advantage in energy efficiency compared with the state-of-art designs when processing video decoding and some other computation-intensive applications.

10:20 am 18-4 **SURFEX: A 57fps 1080P resolution 220mW Silicon Implementation for Simplified Speeded-Up Robust Feature with 65nm Process,** *L. Liu, W. Zhang, C. Deng, S. Yin, S. Cai, S. Wei, Tsinghua University* **704**

Speeded-Up Robust Feature algorithm is optimized for silicon implementation and a 57fps 1080P 220mW ASIC is presented. Methods including orientation assignment& descriptor extraction reorganization, memory accesses improvement and etc. are introduced. Experimental results show proposed architecture has great advantages in performance and power consumption compared with the state-of-art designs.

10:45 am **BREAK**

11:05 am 18-5 **Supply-Noise Resilient Adaptive Clocking for Battery-Powered Aerial Microrobotic System-on-Chip in 40nm CMOS,** *Xuan Zhang, Tao Tong, David Brooks, Gu-Yeon Wei, Harvard University* **708**

A battery-powered aerial microrobotic System-on-Chip (SoC) has stringent weight and power budgets, which requires fully-integrated solutions for both clock generation and voltage regulation. Supply-noise resilience is important yet challenging for such SoC systems due to a non-constant battery discharge profile and load current variability. This paper proposes an adaptive-frequency clocking scheme that can tolerate supply noise and improve performance when implemented with an integrated voltage regulator (IVR). Measurements from a `brain' SoC, implemented in 40nm CMOS, demonstrate 2x performance improvement with adaptive-frequency clocking over conventional fixed-frequency clocking. Combining adaptive-frequency clocking with open-loop IVR extends error-free operation to a wider battery voltage range (2.8 to 3.8V) with higher average performance.

11:30 am 18-6 **Distributed clock generator for synchronous SoC using ADPLL network,** *E. Zianbetov, D. Galayko, F. Anceau, M. Javidan, C. Shan, O. Billoint**, A. Korniienko*, E. Colinet**, G. Scorletti*, J. M. Akre, J. Juillard***, UPMC LIP6 Lab, *Ampere lab, **CEA-LETI, ***Supelec* **712**

This paper presents a novel architecture of on-chip clock generation employing a network of oscillators synchronized by the distributed all-digital PLLs(ADPLLs). The implemented prototype has 16 clocking domains operating synchronously in a frequency range of 1.1-2.4 GHz. The synchronization error between the neighboring clock domains is less than 60 ps. The fully digital architecture of the generation offers flexibility and efficient synchronization control suitable for use in synchronous SoCs.

11:55 am 18-7 **A 920MHz Quad-core Cryptography Processor Accelerating Parallel Task Processing of Public-key Algorithms,** *Shuai Wang, Jun Han, Yang Li, Yifan Bo, Xiaoyang Zeng, Fudan University* **716**

The wireless access point (AP) devices of the next generation requires to implement the high-complexity public-key ciphers efficiently on programmable processors. Therefore, this paper presents a quad-core processor that accelerates public-key computations by enabling high-speed parallel task processing.

## Session 19 -- Analog Techniques I

Wednesday, 9/25, 9:00 am
Pine Ballroom
**Session Chair:** Don Thelen, ON Semiconductor
**Session Co-Chair:** Jerry (Xicheng) Jiang, Broadcom

9:00 am **Introduction**

This session showcases a collection of analog techniques that enable high-performance analog design.

9:05 am 19-1 **Parallel Gain Enhancement Technique for Switched-Capacitor Circuits,** *Hariprasath Venkatram, Benjamin Hershberg, Taehwan Oh, Manideep Gande, Kazuki Sobue*, Koichi Hamashita*, Un-Ku Moon, Oregon State University, *Asahi Kasei Microdevices* **720**

This paper presents a unified classification model for gain enhancement techniques used in the design of high performance amplifiers. A parallel gain enhancement technique is proposed for switched capacitor circuits which combine the best features of the existing gain enhancement techniques found in continuous-time and discrete-time amplifiers. This technique utilizes two dependent closed loop amplifiers to enhance the open loop DC gain of the main amplifier. This replicated parallel gain enhancement (RPGE) technique enables a very high DC gain amplifier with an improved harmonic distortion performance. A proof of concept pipeline ADC in a 0.18 µm CMOS process using RPGE technique achieves 75 dB SNDR, 91 dB SFDR, -87 dB THD at 20 MS/s. The measured 13 bit DNL and INL is +0.75/-0.36 and +0.88/-0.92 LSB respectively. The ADC operates from a supply voltage of 1.3 V, consumes 5.9 mW, occupies 3.06 sq. mm and achieves a figure of merit of 65 fJ/CS.

9:30 am 19-2 **Sampling Circuits That Break the kT/C Thermal Noise Limit (Invited),** *R. Kapusta, H. Zhu, C. Lyden, Analog Devices, Inc.* **724**

This paper presents techniques that prove the kT/C limit of sampled thermal noise is, in fact, not a limit at all. A first feedback technique is demonstrated to reduce thermal noise power by nearly 50%, and a second active noise cancellation technique achieves better than 70% noise power reduction.

10:20 am 19-3 **Blind Background Calibration of Harmonic Distortion Based on Selective Sampling,** *Manideep Gande, Ho-Young Lee, Hariprasath Venkatram, Jon Guerber, Un-Ku Moon, Oregon State University* **730**

This paper proposes a blind calibration algorithm for suppressing harmonic distortion in analog to digital converters (ADCs). The proposed algorithm does not need any external calibration signal and is first of its kind. The proposed algorithm relies on the properties of downsampling and orthogonality of sinusoidal signals to estimate the harmonic distortion coefficients. The algorithm can be operated in both foreground and background modes to remove even and odd harmonics simultaneously. The algorithm is demonstrated on a first-order ring oscillator based delta sigma ADC, whose performance is harmonic distortion limited. Built in 0.13 µm, the algorithm improves the SNDR of the ADC by 39dB while improving SFDR by 45 dB.

10:45 am **BREAK**

11:05 am 19-4 **CMOS Millimeter Wave Phase Shifter Based on Tunable Transmission Lines,** *Wayne H. Woods, Alberto Valdes-Garcia*, Hanyi Ding, Jay Rascoe, IBM Semiconductor Research and*

*Development, *IBM T.J. Watson Research Center* **734**

Design and measurements are presented of a new type of phase shifter, fabricated in a 32 nm SOI technology and operating at 60 GHz, which consists of novel tunable t-line sections that use FET switches to control L and C separately to minimize Z0 variation while changing delay.

11:30 am 19-5 **Charge Steering: A Low-Power Design Paradigm (Invited),** *Behzad Razavi, University of California, Los Angeles* **738**

Discrete-time charge-steering circuits consume less power than their continuous-time current-steering counterparts even at high speeds. This advantage can be exploited in the design of semi-analog circuits such as latches, demultiplexers, and CDR circuits as well as mixed-mode systems such as ADCs. Employing charge steering in 65-nm CMOS technology, a 25-Gb/sCDR/deserializer consumes 5 mW and a 10-bit 800-MHz pipelined ADC draws 19 mW.

## Educational Session 5

Wednesday, 9/25, 9:00 am
Cedar Ballroom
**Session Chair**: Gordon Roberts, McGill University
**Session Co-Chair:** Takamaro Kikkawa, Hiroshima University

E-5 9:00 am – 10:30 am **Design for Nanoscale Patterning,** *Puneet Gupta, UCLA* **746**

This tutorial explains how layout and circuit design interact with lithography choices. Lithography technology is rapidly evolving and has started to impose unusual restrictions on design layout. The tutorial will give a brief introduction to current and upcoming lithography technologies. We especially focus on multi-patterning technologies such as LELE double patterning and SADP. We will discuss design enablement of multi-patterning technologies, especially in context of cell-based digital designs. Models for electrical impact of lithography imperfections such as polysilicon/active rounding and overlay errors will be outlined. We will also briefly explore role of design in lithography technology development.

10:30 am **BREAK**

## Educational Session 6

Wednesday, 9/25, 11:00 am
Cedar Ballroom
**Session Chair**: Howard Luong, Hong Kong University of Science & Technology
**Session Co-Chair:** Earl McCune, RF Communications Consulting

E-6 11:00 am – 12:30 pm **Low Power Chip & System Design for Biomedical Applications,** *Brian Otis, Google, Inc.* **772**

Advances in chip and system design will help define the next generation of wireless sensors for biomedical applications. This talk will investigate system and circuit design techniques for body-worn systems, implantable chips, and wireless sensors. These areas present unique challenges at the interface between the IC and the body that cannot be solved by technology scaling alone. Traditional circuit blocks, architectures, and even assembly techniques need to be questioned. Several future applications will demand thin-film realization and biocompatibility of complex systems. RFID-like techniques are highly useful for many of

these emerging biomedical applications. High-Q RF resonators are useful for minimizing power and size of low power radios. We'll discuss a few examples of the above.

## Session 20 -- Advanced Memory Topics

Wednesday, 9/25, 1:30 pm
Oak Ballroom
**Session Chair**: Koji Nii, Renesas
**Session Co-Chair:** Toshiaki Kirihata, IBM

1:30 pm **Introduction**

This session covers scaling challenges, latest advances, and future trends on spin-torque, MRAM, NAND, and logic-compatible flash, TCAM, and 6T/8T SRAM.

1:30 pm **Introduction**

This session covers scaling challenges, latest advances, and future trends on spin-torque, MRAM, NAND, and logic-compatible flash, TCAM, and 6T/8T SRAM.

1:35 pm 20-1 **ST-MRAM Fundamentals, Challenges, and Applications (Invited),** *T. Andre, S.M. Alam, D. Gogl, C.K. Subramanian, H. Lin, W. Meadows, X. Zhang, N.D. Rizzo, J. Janesky, D. Houssameddine, J.M. Slaughter, Everspin Technologies* **799**

MRAM technology emerged from research and development into volume production within the last decade in the form of Toggle MRAM. Spin-Torque MRAM has reached the level of customer sampling, offering higher density and bandwidth. This paper describes the devices, fundamental circuit challenges, and applications of this evolving MTJ based memory.

2:25 pm 20-2 **Scaling Challenges of NAND Flash Memory and Hybrid Memory System with Storage Class Memory & NAND flash memory (Invited),** *Ken Takeuchi, Chuo University* **807**

SSDs and emerging storage class non-volatile memories such as PCRAM, ReRAM and MRAM have enabled innovations in various nano-scale VLSI memory systems for personal computers, smart phones, tablets and enterprise servers. This paper discusses the scaling challenges of 2D and 3D NAND flash memory and then provides a state-of-the-art hybrid memory solution with storage class memory and NAND flash memory for the big data solid-state storage system.

3:15 pm **BREAK**

3:30 pm 20-3 **A 28nm High Density 1R/1W 8T-SRAM Macro with Screening Circuitry against Read Disturb Failure,** *M. Yabuuchi, H. Fujiwara, Y. Tsukamoto. M. Tanaka, K. Nii, Renesas Electronics Corporation* **813**

We developed a high density 1R/1W SRAM macro based on 8T-SRAM with a novel scheme for Design for Testing. To achieve a smaller Macro area, a differential sense amplifier is introduced to read the data, where the reference voltage for reading 0/1 data is generated by unselected cell array. In addition, we proposed a screening test circuit for read disturb operation.

3:55 pm **A HKMG 28nm 1GHz Fully-Pipelined Tile-able 1MB Embedded SRAM IP with**

20-4 **1.39mm$^2$ per MB,** *M. Z. Kuo, O. Takahashi, P. L. Yang, C. C. Lin, M.J. Wang, P.W. Wang, S. H. Dhong, Taiwan Semiconductor Manufacturing Company* **817**

A fully-pipelined tile-able 1MB SRAM IP with a 0.127µm2 cell in a HKMG 28nmbulk technology has an area of 1.39mm2/MB with 79.2% array efficiency. It operates with 2-cycle latency up to 1GHz. The no-repair hardware has a circuit limited yield of 99.92 and 53% at 100 and 850MHz, respectively with 0.75V VDD.A Data Retention Voltage of 0.42V has been measured.

4:20 pm 20-5 **A Bit-by-Bit Re-Writable Eflash in a Generic Logic Process for Moderate-Density Embedded Non-Volatile Memory Applications,** *Seung-Hwan Song, Ki Chul Chun, Chris H. Kim, University of Minnesota* **821**

A bit-by-bit re-writable embedded flash memory is demonstrated in a generic65nm logic process for moderate-density embedded non-volatile memory applications. The proposed 6T embedded flash memory cell improves the overall cell endurance by eliminating redundant program/erase cycles without disturbing cells in the unselected wordlines. A multi-story high voltage switch utilizes four boosted supply levels generated by a compact voltage doubler based on-chip negative charge pump.

4:45 pm 20-6 **Tail-Bit Tracking Circuit with Degraded VGS Bit-Cell Mimic Array for a 50% Search-Time and 200mV Vmin Improvement in a Ternary Content Addressable Memory,** *Igor Arsovski, Travis Hebig, John Goss, Paul Grzymkowski, Josh Patch , IBM* **825**

A memory sense-timing circuit uses VGS degradation to emulate the behavior of weak memory tail-bits, improving Tail-Bit Tracking (TBT) across process, voltage and temperature. The TBT circuit generates timing for a TCAM search operation reducing Vmin by 200mV, and improving sense-time by 50%. Implemented in 32nm HKMG SOI process the 2Kx640b TCAM achieves 0.60V and 1G search/sec.

## Session 21 -- Oversampled ADC's

Wednesday, 9/25, 1:30 pm
Fir Ballroom
**Session Chair**: Eric Naviasky, Cadence
**Session Co-Chair**: Hasnain Lakdawala, Qualcomm

1:30 pm **Introduction**

This session has 4 papers on noise shaping ADC's. The first two papers take advantage of the noise shaping 1˜ inherent in a VCO. The last two offer novel solutions to feedback DAC imperfections.

1:35 pm 21-1 **A 1.8mW 2MHz-BW 66.5dB-SNDR Delta-Sigma ADC Using VCO-Based Integrators with Intrinsic CLA,** *Kyoungtae Lee, Yeonam Yoon, Nan Sun, The University of Texas at Austin* **829**

This paper presents a scaling-friendly continuous-time closed-loop VCO-based Delta-Sigma ADC. It uses the VCO as both quantizer and integrator, and thus, obviates the need for power-hungry scaling-unfriendly OTAs and precision comparators. It arranges two VCOs in a pseudo-differential manner, which cancels out even-order distortions. More importantly, it brings an intrinsic CLA capability that automatically addresses DAC mismatches. The prototype ADC in 130nm CMOS occupies a small area of 0.03mm^2 and achieves 66.5dB

SNDR over2MHz BW while sampling at 300MHz and consuming 1.8mW under a 1.2V power supply. It can also operate with a low analog supply of 0.7V and achieves 65.8dB SNDR while consuming 1.1mW. The corresponding FOMs for the two cases are 0.25pJ/step and 0.17pJ/step, respectively.

2:00 pm 21-2 **A 50MHz bandwidth, 10-b ENOB, 8.2mW VCO-based ADC enabled by filtered-dithering based linearization,** *Abhishek Ghosh, Sudhakar Pamarti, University of California, Los Angeles* **833**

A dithering technique for linearization of VCO-based ADCs is proposed. The proposed technique conditions the signal to the VCO input to appear as whitenoise thereby eliminating spurious signal content arising out of the VCO nonlinearity. The technique, thus obviates the need for power-hungry digital calibration techniques or expensive front-end loop-filters. A prototype implementation (in 65nm CMOS) based on the technique achieves 10-b ENOB in digitizing signals with 50MHz bandwidth consuming 8:2mW at an FoM of 90fJ/conv.step.

2:25 pm 21-3 **A Reconfigurable Delta-Sigma Modulator With Up To 100 MHz Bandwidth Using Flash Reference Shuffling,** *T. Caldwell, D. Alldred, Z. Li, Analog Devices, Inc* **837**

A reconfigurable 65 nm continuous-time low-pass delta-sigma modulator operates with a sampling frequency from 491 MHz to 1536 MHz, a signal bandwidth from 10MHz to 100 MHz, and a dynamic range of 75.4 dB to 62.8 dB, respectively. Reference shuffling in the flash ADC is used to improve the linearity of the flash and DAC, while also increasing the highest sampling rate and bandwidth of the modulator.

2:50 pm 21-4 **A 10-MHz Bandwidth 70-dB SNDR 640MS/s Continuous-Time Sigma-Delta ADC Using Gm-C Filter with Nonlinear Feedback DAC Calibration,** *J. Huang, S. Yang, J. Yuan, Hong Kong University of Science and Technology* **841**

Traditionally, wide-band (>10MHz) continuous-time sigma-delta ADCs with Gm-C filters have poor linearity. This paper introduces a novel on-chip calibration scheme to compensate the Gm-cell's nonlinearity. Measurements of the 640MS/s CTSD modulator show the best SNDR and power efficiency among Gm-C-based modulators. The FOM is also comparable to active-RC-based modulators.

3:15 pm **BREAK**

## Session 22 - AMS System Simulation Techniques

Wednesday, 9/25, 1:30 pm
Pine Ballroom
**Session Chair:** Larry Nagel, Omega Enterprises
**Session Co-Chair:** Colin McAndrew, Freescale

1:30 pm **Introduction**

This session presents new, innovative, and efficient techniques that extend the state of the art for analog mixed-signal (AMS) system-level simulations.

1:35 pm 22-1 **Algorithmic Nonlinear Macromodeling: Challenges, Solutions and Applications in Analog/Mixed-Signal Validation (Invited),** *C. Gu, Intel Corporation* **845**

Analog/Mixed-Signal validation at the system level is becoming increasingly important as more electrical bugs are caused by the interaction among various circuit blocks. While hand-crafted behavioral models and linear models are still most widely used among designers, there is an increasing need for automatic behavioral modeling tools which capture low-level nonlinear behaviors in the circuit. This paper discusses challenges and difficulties of algorithmic nonlinear macromodeling, and reviews a series of recently developed techniques. In particular, we study the behavioral modeling problem from the perspective of projection in the state space defined by voltages and currents. We review a few nonlinear macromodeling techniques from the projection perspective, and demonstrate the model accuracy and computational efficiency compared to transistor-level models and linear models.

2:25 pm 22-2 **Event-Driven Simulation of Volterra Series Models in System Verilog,** *J-E. Jang, S-J. Yang, J. Kim, Seoul National University* **853**

This paper presents a true event-driven methodology to simulate weakly-nonlinear analog circuits in System Verilog. We express a continuous-time signal as a linear combination of basis functions and reformulate a Volterra series model into a set of linear differential equations with an explicit notion on initial conditions. Two circuit examples showed 300~1000× speed-up compared to SPICE with the same accuracy.

2:50 pm 22-3 **A Verilog Piecewise-Linear Analog Behavior Model for Mixed-Signal Validation,** *S. Liao, M. Horowitz, Stanford University* **857**

Mixed-signal validation requires simulating the entire chip through a large number of test vectors, which makes pin-accurate and fast Verilog functional models of analog circuits with reasonable fidelity valuable. We describe an extensible approach to creating these models, by mapping continuous signals into discrete events and avoiding explicit time integration.

3:15 pm **BREAK**

3:30 pm 22-4 **Advancements in High-Speed Link Modeling and Simulation (Invited),** *Mike Peng Li, Masashi Shimanouchi, Hsinho Wu, Altera Corporation* **861**

This paper starts with reviewing the status of techniques and methods used in recent high-speed link simulation and modeling for signaling, integrated circuits, board circuits, and associated limitations and challenges, and then discusses new advancements that can overcome them.

4:20 pm 22-5 **Structure-Aware High-Dimensional Performance Modeling for Analog and Mixed-Signal Circuits,** *S. Sun, X. Li, C. Gu*, Carnegie Mellon University, *Intel Corp* **869**

Efficient high-dimensional performance modeling of nanoscale analog and mixed signal (AMS) circuits is challenging. In this paper, we propose a novel structure-aware modeling technique to accurately solve the model coefficients by exploiting the underlying structure of AMS circuits, and hence dramatically reduce the number of sampling points for performance modeling.

## Session 23 -- Analog Techniques II

Wednesday, 9/25, 3:25 pm
Fir Ballroom
**Session Chair:** Hasnain Lakdawala, Qualcomm

**Session Co-Chair**: Eric Naviasky, Cadence

3:25 pm **Introduction**

The session includes topics in time to digital converters, fast locking PLL's and double sampling sigma delta ADC's.

3:30 pm 23-1 **A 148fs$_{rms}$Integrated Noise 4MHz Bandwidth All-Digital Second-Order ΔΣ Time-to-Digital Converter Using Gated Switched-Ring Oscillator,** *W. Yu, K.S. Kim, S. Cho, KAIST* **873**

This paper presents an all-digital second-order ΔΣ time-to-digital converter(TDC) by using switched-ring oscillator (SRO) and gated switched-ring oscillator (GSRO). Unlike conventional multi-stage noise-shaping (MASH) TDC using the SRO, the proposed TDC does not require complex calibration to compensate for the error from frequency difference between the SROs. The prototype TDC achieves 148fsrms integrated noise and 80.4dB dynamic range in4MHz signal bandwidth at 400MS/s while consuming 6.55mW in a 65nm CMOS process.

3:55 pm 23-2 **A 0.84ps-LSB 2.47mW Time-to-Digital Converter Using a Charge Pump and a SAR-ADC,** *Zule Xu, Seungjong Lee, Masaya Miyahara, and Akira Matsuzawa, Tokyo Institute of Technology* **877**

We propose a 0.84ps-LSB, 2.47mW, 0.06mm² time-to-digital converter (TDC) using a charge pump and a SAR-ADC in 65nm CMOS. Sub-pico second time resolution is attainable by quantizing the time in charge domain. Low power consumption and small area are also feasible by using the SAR-ADC.

4:20 pm 23-3 **A double-sampling cross noise-coupled Sigma Delta modulator with a reduced amount of opamps,** *M. De Bock, P. Rombouts, UGhent* **881**

A second order double-sampling cross noise-coupled split-path Sigma Delta modulator is presented. The implementation of the noise-coupling is incorporated into the second integrator using a novel delaying feed-forward circuit. A prototype integrated in a 130nm CMOS technology achieves 77.8dBdynamic range and 71.4dB SNDR over a 5MHz bandwidth.

4:45 pm 23-4 **A Novel OTA-Based Fast Lock PLL,** *Mezyad Amourah, Sandeep Krishnegowda, Morgan Whately, Cypress Semiconductor* **885**

A novel fast lock scheme for phase-locked loops (PLLs). The proposed scheme uses a simple operational transconductance amplifier (OTA) to achieve significant reduction in PLL lock acquisition time without affecting PLL noise performance. The new fast lock schemes were implemented in multi-port SRAM chip to provide frequencies from 400MHz to 1.6GHz, The chip was fabricated using 65nm CMOS process. Silicon measurements across corner lots show significant reduction in PLL lock time, by a factor of 6.5X, over device operating conditions.

## Educational Session 7

Wednesday, 9/25, 1:30 pm
Cedar Ballroom
**Session Chair**: Mike Li, Altera
**Session Co-Chair:** Gerrit den Besten, NXP Semiconductors

E-7 **Trends, Possibilities and Limitations of Photonic Integrated Circuits and Lasers,**
1:30 pm – *John E. Bowers, University of California, Santa Barbara* **889**
3:00 pm

A number of important breakthroughs in the past decade have focused attention on Si as a photonic platform. We review here recent progress in this field, focusing on efforts to make lasers, amplifiers, modulators and photodetectors on or in silicon. We also describe progress in silicon photonic integrated circuits. The impact active silicon photonic integrated circuits could have on interconnects, telecommunications and on silicon electronics is reviewed.

3:00 pm **BREAK**

## Educational Session 8

Wednesday, 9/25, 3:30 pm
Cedar Ballroom
**Session Chair**: Jerry Jiang, Broadcom
**Session Co-Chair:** Eric Naviasky, Cadence

E-8 **A/D Converter Circuit and Architecture Design for High-Speed Data Communication,**
3:30 pm – *Boris Murmann, Stanford University* **934**
5:00 pm

A number of important breakthroughs in the past decade have focused attention on Si as a photonic platform. We review here recent progress in this field, focusing on efforts to make lasers, amplifiers, modulators and photodetectors on or in silicon. We also describe progress in silicon photonic integrated circuits. The impact active silicon photonic integrated circuits could have on interconnects, telecommunications and on silicon electronics is reviewed.