2013 European Conference on Circuit Theory and Design

(ECCTD 2013)

Dresden, Germany 8-12 September 2013



IEEE Catalog Number: ISBN: CFP13ECC-POD 978-1-4799-2857-6

Table of Contents

PAPER NUMBER PAPER TITLE

- 3 Jointly Optimal High-Order Error Feedback and Realization for Roundoff Noise Minimization in 2-D State-Space Digital Filters
- 4 Design of Sparse Lowpass Differentiator Using Iterative Hard Thresholding Method
- 5 Fractional Derivative Constrained Design of FIR Filter with Prescribed Magnitude and Phase Responses
- 8 Improved Single-Stage Kikback-Rejected Comparator for High Speed and Low Noise Flash ADCs
- 10 CMOS photodiode model and HDL implementation
- 12 A Construction Method of Optimum Integer-to-integer Transform based on an Error Propagation Model
- 13 A High Dynamic Range CMOS Image Sensor with a Digital Configurable Logarithmic Counter
- 15 Design and analysis of novel dynamic latched comparator with reduced kickback noise for high-speed ADCs
- 17 Efficiency Improvement of Partially Shaded Photovoltaic Panels
- 18 Throughput Enhancement for a New Time-delay Sampled-data System Based True Random Bit Generator
- 20 Power Savings in Digital Filters for Wireless Communication
- 21 Analysis of the mutual inductive and capacitive connections and tolerances of memristor's parameter's of a memristor memory matrix
- 23 Implementation of a Pulse-Holding Time-to-Digital Converter on an FPGA
- 24 An 8-b Cascaded Folding A/D Converter with a New Fully Differential Source Follower
- 27 Estimation of In-Cylinder Pressure Using Spark Plug Discharge Current Measurements
- 28 Finding All Solutions of Piecewise-Linear Resistive Circuits Using Separable Programming
- 29 Spatial Computing Architecture Using Randomness of Memory Cell Stability under Voltage Control
- 31 A Configurable Sampling Rate Converter for All-Digital 4G Transmitters
- 32 A 0.35µm CMOS 6-bit Current Steering DAC
- 33 Evaluating the influence of noise on the spectrum of an oscillator
- 34 The Spatial CAUCHY Problem for a Dissipative Infinite Quantum Waveguide Supporting a Single Propagating Mode
- 35 OpAmp Design for Lock-in Amplifiers in Portable Sensing Systems
- 36 Reliable and Efficient Phase Noise Simulation of Mixed-Mode Integer-N Phase-Locked Loops
- 38 Oscillators a simple introduction
- 39 Turn your baseband Matlab simulator into a fully functional, 2.4-GHz, operating FM-DCSK transceiver using SDE platform
- 40 A Low Noise Single-Ended to Differential Linear Charge Sampling SC-VGA for Second Harmonic Cardiac Ultrasound Imaging
- 41 A Low Noise Single-End to Differential Switched-Capacitor VGA for PZT Xducer Ultrasound Imaging
- 42 An LDO using stacked transistors on 65 nm CMOS
- 43 Design Tradeoffs in N-path GmC Integrators for Direct Delta-Sigma Receivers
- 44 A 65nm CMOS Front-end LNA for Medical Ultrasound Imaging with Feedback Employing Noise and Distortion Cancellation
- 45 A 176x120 Pixel CMOS Vision Chip for Gaussian Filtering with Massivelly Parallel CDS and A/D-Conversion
- 46 Realizable Reduction of Interconnect Models with Dense Coupling
- 47 An LC CMOS Injection-Locked Frequency Divider for Divide-by-Two and Divide-by-Three Operation
- 48 Low Power 2 Mbps Radio Telemetry System for Biomedical Applications
- 49 A Low Power Analog RAM Implementation for In-Probe Beamforming in Ultrasound Imaging
- 51 Effect of components relative tolerance in the magnitude response of a Gm-C biquad
- 53 Approximation of Almost Equiripple Low-pass FIR Filters
- 54 Syntheses of a PSpice Model of a Titanium-dioxide Memristor and Wien Memristor generator
- 55 A new driven memristive chaotic circuit
- 57 Sequential multiobjective optimization for large-scale passive filter synthesis
- 59 Memristor Macromodel and Its Application to Neuronal Spike Generation
- 61 Development of Antenna Deployment Circuit for Nano-Satellites
- 62 Lithography-Aware 1-Dimensional Cell Generation
- 64 Stabilization of coupled reaction-diffusion CNN
- 65 Trigger-Wave Propagation in Arbitrary Metrics in Asynchronous Cellular Logic Arrays
- 68 Admittance parameter formulation for realizable model-order reduction
- 69 A novel output transformer based highly linear RF-DAC architecture
- 70 Motion Picture Processing by Two-Layer Cellular Neural Networks with Switching Templates
- 71 Application of universal software defined PXI platform for the performance evaluation of FM-DCSK communications system
- 73 Optimized Frequency Compensation Topology for Low-Power Three-Stage OTAs
- A time-gated 4x128 SPAD array with a 512 channel flash 80 ps-TDC for pulsed Raman spectroscopy
- 76 Extended Constraint Management for Analog and Mixed-Signal IC Design

- 77 Comparison of Time-Domain and Frequency Domain Polynomial Fitting
- 78 Complex Adaptive Notch Filters for Frequency Estimation of Three-Phase Power Systems
- 79 Model Order Reduction by State Vector Selection (SVS) Approach
- 81 Modelling of a Charge Control Method for Capacitive MEMS
- 82 3-D Spatio-temporal Gabor-Type Filter Implementations with Time-Derivative Cellular Neural Networks
- 84 Power Grid Dispatch Policies and Robustness to Chain Failures
- 85 Low Power Secure CSSAL Bit-Parallel Multiplier over GF(2⁴) in 0.18um CMOS Technology
- 87 A Study on Random Bit Sequences with Prescribed Auto-Correlations by Post-Processing Using Linear Feedback Shift Registers
- 89 Observation of Spontaneous Bursting Spike Patterns in Simple Three Memristor Circuits
- 90 A Configurable IC to Contol, Readout, and Calibrate an Array of Biosensors
- 91 Steady-State Analysis of a Distributed Model of the Buck Converter
- 92 Strategies for Finding a Bandwidth-Optimal Topology for Impedance Matching
- 93 An Adaptive Approach to On-Chip CMOS Ramp Generation for High Resolution Single-Slope ADCs
- 94 Using ADZT for signal reconstruction
- 95 Simulation of Hybrid MTL Systems with Random Parameters based on Stochastic DAEs
- 97 Stabilizing Control based on Stability Transformation Method for Switching Power Converter
- 99 Filter-induced Bifurcation in Simple Spiking Circuits
- 100 A class of generalized orthonormal functions
- 101 A simple extraction procedure for determining the electrical parameters in Silicon Photomultipliers
- 102 State Space Analysis of Mixed Signal Systems with Switched Feedback and Delay
- 105 A High-Throughput Spur-Free Hybrid Nested Bus-Splitting/HK-MASH Digital Delta-Sigma Modulator
- 106 Experimental Validation of DAC with Nested Bus-Splitting EFM4 DDSM
- 107 STDP-Enabled Learning on a Reconfigurable Neuromorphic Platform
- 108 Insights on memristor modeling
- 109 Pulse Width Modulation Using a Recently Developed CMOS Core Circuit
- 110 NERO Mastering 300k CNN Cells
- 111 A Memory-Efficient Routing Method for Large-Scale Spiking Neural Networks
- 113 Folded-Cascode Transimpedance Amplifiers Employing a CMOS Inverter as Input Stage
- 114 A Study of RF Oscillator Reliability in Nanoscale CMOS
- 117 Coil shape design using the quasi-Newton algorithm
- 119 Frequency noise of CMOS LC tank oscillators operating in weak inversion
- 120 Critical Role of Initial Condition in the Dynamics of Memristive Systems: Orbital Narrowing Revisited
- 121 FPGA-implementation of a Holographic Pattern-matching Algorithm
- 122 Gain Estimation of a Digital-to-Time Converter for Phase-Prediction All-Digital PLL
- 123 Frequency Characterization of Memristive Devices
- 126 Automated synthesis of asynchronous event-based interfaces for neuromorphic systems
- 127 A Thermal Management System for Lithium-ion Battery in Mobile Systems
- 129 Double-Gate FinFET Process Variation Aware 10T SRAM Cell Topology Design and Analysis
- 130 Design Criteria for Loop Filters in Spectrum Balancing Technique-Based Adaptive Equalisers
- 131 An Energy-Efficient $\Delta\Sigma$ Modulator Using Dynamic-Common-Source Integrators
- 132 A Compact Low-voltage First-order Temperature-compensated CMOS Current Reference
- 134 Clustering Phenomena in Coupled Chaotic Circuits with Different Coupling Strength
- 135 Complex dynamics in neuromorphic memristor circuits
- 137 Exploration of Tradeoffs in the Design of Integer Cosine Transforms for Image Compression
- 138 Applying Cellular Neural Networks Dynamics for Image Representation
- 139 A 1.8 MHz MEMS-based oscillator with synchronous amplitude limiter.
- 141 Method of Modeling Analog Circuits in Verilog for Mixed-signal Design Simulations
- 142 A CMOS Quasi-digital Temperature Sensor for Battery Operated Systems
- 143 An Analog Dynamic Memory Array for Neuromorphic Hardware
- 145 A Modified Cross Coupled Rectifier based Charge Pump for Energy Harvesting using RF to DC conversion
- 147 A Wideband Lumped-Element Model for Arbitrarily Shaped Integrated Inductors
- 149 The Doppler Effect with Input Driven Autowaves
- 150 A High-Speed QR Decomposition Processor for Carrier-Aggregated LTE-A Downlink Systems
- 153 Realization of Preprocessing Blocks of CNN Based CASA System on FPGA
- 156 Application of Tool-Specific Simulation Algorithms to Memristor Models Written in Modelica
- 157 Design of 2D Parametric Filters for Directional Gaussian Smoothing
- 158 Novel Electronics for High-speed FM AFM in Life Science Applications
- 159 Discretization effects in single input delayed sliding mode control systems
- 160 Analysis of a Controlled 3-D Piecewise-Constant Circuit with time-delayed feedback
- 161 Study of peak and backoff efficiency of different power amplifier classes in outphasing systems
- 162 An Estimation Method for the 3 Port S-parameters with 1 Port Measurements
- 163 A neuromorphic approach to auditory pattern recognition in cricket phonotaxis

- 164 Oscillator Synthesis based on Nambu Mechanics with Canonical Dissipative Damping
- 165 A new oscillator scheme for analog modeling
- 166 Emulation of analog memristors using low yield digital switching memristors
- 167 Implementation trade-offs of the density matrix renormalization group algorithm on kilo-processor architectures
- 168 Behavioral Model of a Continuous Current Integrator with Time Discrete Feedback and Sampling
- 169 Autonomous detection of information patterns through hierarchical peeling
- 170 Analysis of myoelectric signals using a Field Programmable SoC
- 171 FPGA-based implementation of a real-time timing measuring device
- 174 A Chaos Based Integrated Jitter Booster Circuit for True Random Number Generators
- 175 Blocker and Image Reject Low-IF Frontend
- 176 Focused Calibration for Advanced RF Test with Embedded RF Detectors
- 177 A consideration on the condition number of extremely ill-conditioned matrices
- 178 Memristor Circuit Investigation through a new Tutorial Toolbox
- 179 Frameless computing for spatial-temporal events
- 180 Architectures for Nanoscale Hybrid Computing Systems
- 181 Multiple Metastable Rotating Waves and Long Transients in Cooperative CNN Rings
- 183 More on the Generalized Fisher Discriminant Based in 2 Neuron Cellular Neural Networks
- 184 Parameter properties of electronic and biological circuits and systems
- 6 Analysis of a Charge Redistribution SAR ADC with Partially Thermometer Coded DAC
- 14 Efficient Multistage Implementation of Rational Sampling Rate Converter
- 16 Design Strategies for Integrated High Voltage Charge Pumps
- 22 Mixed-Mode Simulations to Check Stability of an Adaptive Constant On-Time DC-DC Converter
- 26 A 1.25 Gb/s Fully Integrated Optical Receiver for SI-POF Applications
- 30 Inductively Coupled Wireless Power Transfer With Class-E² DC-DC Converter
- 52 Modeling and Optimization of a Dedicated FMCW Radar Frequency Synthesizer
- 56 Compact Implementation of a Three Stages Feedforward Operational Transconductance Amplifier with Miller Compensation
- 60 Low Power OTA-Less I-V-converter with Single-Ended To Differential Conversion for Capacitive Sensor Interfaces
- 88 Design and circuit implementation of approximate switched MPC
- 98 Reconstruction of conductances in resistive grids as an optimization problem
- 104 Live Demonstration: Ethernet Communication Linking Two Large-Scale Neuromorphic Systems
- 136 A Parallelized Distance Transformation Architecture for FPGAs
- 144 Live Demonstration: A 90GBit/s Serial NoC Link over 6mm in 65nm CMOS Technology
- 146 On Chaotic Behavior in Automatic Tuning Loops for Continuous–Time Filters
- 148 A 70 dBohm 2.3 GHz low noise Transimpedance Amplifier
- 199 Networks, Multipoles and Multiports (Tutorial Paper)